

3875081 G E SOLID STATE

01E 11044 D

7-37-25



J174-J177

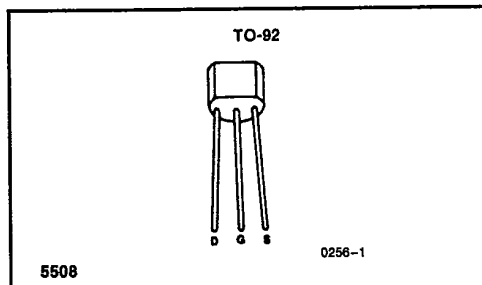
J174-J177

P-Channel JFET Switch

FEATURES

- Low Insertion Loss
- No Offset or Error Generated By Closed Switch
 - Purely Resistive
 - High Isolation Resistance From Driver
- Short Sample and Hold Aperture Time
- Fast Switching

PIN CONFIGURATION



APPLICATIONS

- Analog Switches
- Choppers
- Commutators

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage	30V
Gate Current	50mA
Storage Temperature Range	-55°C to +150°C
Operating Temperature Range	-55°C to +135°C
Lead Temperature (Soldering, 10sec)	300°C
Power Dissipation	350mW
Derate above 25°C	3.3mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-92

J17X

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	J174			J175			J176			J177			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{GSS}	Gate Reverse Current (Note 1)	V _{DS} = 0, V _{GS} = 20V			1			1			1			1	nA
V _{GS(off)}	Gate Source Cutoff Voltage	V _{DS} = -15V, I _D = -10nA	5		10	3		6	1		4	0.8		2.25	V
BV _{GSS}	Gate Source Breakdown Voltage	V _{DS} = 0, I _G = 1μA	30			30			30			30			
I _{DSS}	Drain Saturation Current (Note 2)	V _{DS} = -15V, V _{GS} = 0	-20		-135	-7		-70	-2		-35	-1.5		-20	mA
I _{D(off)}	Drain Cutoff Current (Note 1)	V _{DS} = -15V, V _{GS} = 10V			-1			-1			-1			-1	nA
r _{DS(on)}	Drain-Source ON Resistance	V _{GS} = 0, V _{DS} = -0.1V			85			125			250			300	Ω

INTERSIL'S SOLE AND EXCLUSIVE WARRANTY OBLIGATION WITH RESPECT TO THIS PRODUCT SHALL BE THAT STATED IN THE WARRANTY ARTICLE OF THE CONDITION OF SALE. THE WARRANTY SHALL BE EXCLUSIVE AND SHALL BE IN LIEU OF ALL OTHER WARRANTIES, EXPRESS, IMPLIED OR STATUTORY, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR USE.

NOTE: All typical values have been characterized but are not tested.

3875081 G E SOLID STATE

01E 11045 D

J174-J177**INTERSIL**

T-37-25

J174-J177

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions				J174			J175			J176			J177			Units
						Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
C _{dg(off)}	Drain-Gate OFF Capacitance	V _{DS} = 0,	f = 1MHz (Note 3)				5.5			5.5			5.5			5.5		pF
C _{sg(off)}	Source-Gate OFF Capacitance	V _{GS} = 10V					5.5			5.5			5.5			5.5		
C _{dg(on)} + C _{sg(on)}	Drain-Gate Plus Source Gate ON Capacitance	V _{DS} = V _{GS} = 0					32			32			32			32		
t _{d(on)}	Turn On Delay Time	Switching Time Test Conditions					2			5			15			20		ns
		(Note 3)	J174	J175	J176	J177												
t _r	Rise Time	V _{DD} = -10V	-10V	-6V	-6V	-6V		5		10			20			25		
t _{d(off)}	Turn Off Delay Time	V _{GS(off)} = 12V	8V	3V	3V	3V		5		10			15			20		
		R _L = 560Ω	12kΩ	5.6kΩ	10kΩ													
t _f	Fall Time	V _{GS(on)} = 0V	0V	0V	0V	0V		10		20			20			25		

NOTES: 1. Approximately doubles for every 10°C increase in T_A .
 2. Pulse test duration — 300 μs ; duty cycle $\leq 3\%$.
 3. For design reference only, not 100% tested.

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NOTE: All typical values have been characterized but are not tested.