

Quad, 1MHz, Operational Amplifiers for Commercial, Industrial, and Military Applications

The CA124, CA224, CA324, LM324, and LM2902 consist of four independent, high-gain operational amplifiers on a single monolithic substrate. An on-chip capacitor in each of the amplifiers provides frequency compensation for unity gain. These devices are designed specially to operate from either single or dual supplies, and the differential voltage range is equal to the power-supply voltage. Low power drain and an input common-mode voltage range from 0V to V+ -1.5V (single-supply operation) make these devices suitable for battery operation.

Part Number Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA0124E	-55 to 125	14 Ld PDIP	E14.3
CA0124M (124)	-55 to 125	14 Ld SOIC	M14.15
CA0124M96 (124)	-55 to 125	14 Ld SOIC Tape and Reel	M14.15
CA0224E	-40 to 85	14 Ld PDIP	E14.3
CA0224M (224)	-40 to 85	14 Ld SOIC	M14.15
CA0324E	0 to 70	14 Ld PDIP	E14.3
CA0324M (324)	0 to 70	14 Ld SOIC	M14.15
CA0324M96 (324)	0 to 70	14 Ld SOIC Tape and Reel	M14.15
LM324N	0 to 70	14 Ld PDIP	E14.3
LM2902N	-40 to 85	14 Ld PDIP	E14.3
LM2902M (2902)	-40 to 85	14 Ld SOIC	M14.15
LM2902M96 (2902)	-40 to 85	14 Ld SOIC Tape and Reel	M14.15

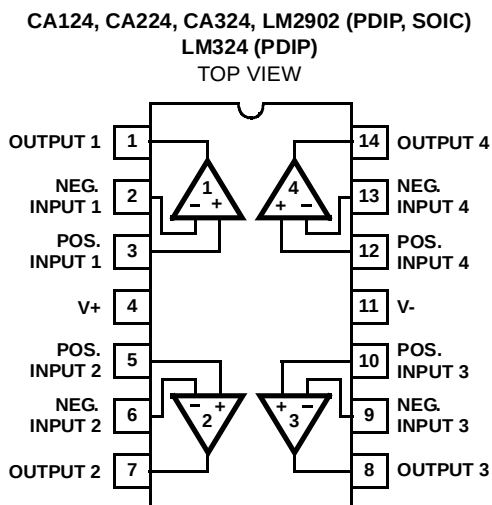
Features

- Operation from Single or Dual Supplies
- Unity-Gain Bandwidth 1MHz (Typ)
- DC Voltage Gain 100dB (Typ)
- Input Bias Current 45nA (Typ)
- Input Offset Voltage 2mV (Typ)
- Input Offset Current
 - CA224, CA324, LM324, LM2902 5nA (Typ)
 - CA124. 3nA (Typ)
- Replacement for Industry Types 124, 224, 324

Applications

- Summing Amplifiers
- Multivibrators
- Oscillators
- Transducer Amplifiers
- DC Gain Blocks

Pinout



CA124, CA224, CA324, LM324, LM2902

Absolute Maximum Ratings

Supply Voltage 32V or ± 16 V
 Differential Input Voltage 32V
 Input Voltage -0.3V to 32V
 Input Current ($V_I < -0.3$ V, Note 1) 50mA
 Output Short Circuit Duration ($V+ \leq 15$ V, Note 2) Continuous

Operating Conditions

Temperature Range
 CA124 -55°C to 125°C
 CA224, LM2902 -40°C to 85°C
 CA324, LM324 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (°C/W)
 PDIP Package 95
 SOIC Package 175
 Maximum Junction Temperature (Die) 175°C
 Maximum Junction Temperature (Plastic Package) 150°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C
 (SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. This input current will only exist when the voltage at any of the input leads is driven negative. This current is due to the collector base junction of the input p-n-p transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral n-p-n parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the $V+$ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This transistor action is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3V.
2. The maximum output current is approximately 40mA independent of the magnitude of $V+$. Continuous short circuits at $V+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to $V+$ can cause overheating and eventual destruction of the device.
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Values Apply for Each Operational Amplifier. Supply Voltage $V+ = 5$ V, $V- = 0$ V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	CA124			CA224, CA324, LM324			LM2902			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (Note 6)		25	-	2	5	-	2	7	-	-	-	mV
		Full	-	-	7	-	-	9	-	-	10	mV
Average Input Offset Voltage Drift	$R_S = 0\Omega$	Full	-	7	-	-	7	-	-	7	-	$\mu V/^\circ C$
Differential Input Voltage (Note 5)		Full	-	-	$V+$	-	-	$V+$	-	-	$V+$	V
Input Common Mode Voltage Range (Note 5)	$V+ = 30$ V	25	0	-	$V+ - 1.5$	0	-	$V+ - 1.5$	-	-	-	V
	$V+ = 30$ V	Full	0	-	$V+ - 2$	0	-	$V+ - 2$	-	-	-	V
	$V+ = 26$ V	Full	-	-	-	-	-	-	0	-	$V+ - 2$	V
Common Mode Rejection Ratio	DC	25	70	85	-	65	70	-	-	-	-	dB
Power Supply Rejection Ratio	DC	25	65	100	-	65	100	-	-	-	-	dB
Input Bias Current (Note 4)	I_{I+} or I_{I-}	25	-	45	150	-	45	250	-	-	-	nA
	I_{I+} or I_{I-}	Full	-	-	300	-	-	500	-	40	500	nA
Input Offset Current	$I_{I+} - I_{I-}$	25	-	3	30	-	5	50	-	-	-	nA
	$I_{I+} - I_{I-}$	Full	-	-	100	-	-	150	-	45	200	nA
Average Input Offset Current Drift		Full	-	10	-	-	10	-	-	10	-	$pA/^\circ C$
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V+ = 15$ V (For Large V_O Swing)	25	94	100	-	88	100	-	-	-	-	dB
	$R_L \geq 2k\Omega$, $V+ = 15$ V (For Large V_O Swing)	Full	88	-	-	83	-	-	83	-	-	dB

CA124, CA224, CA324, LM324, LM2902

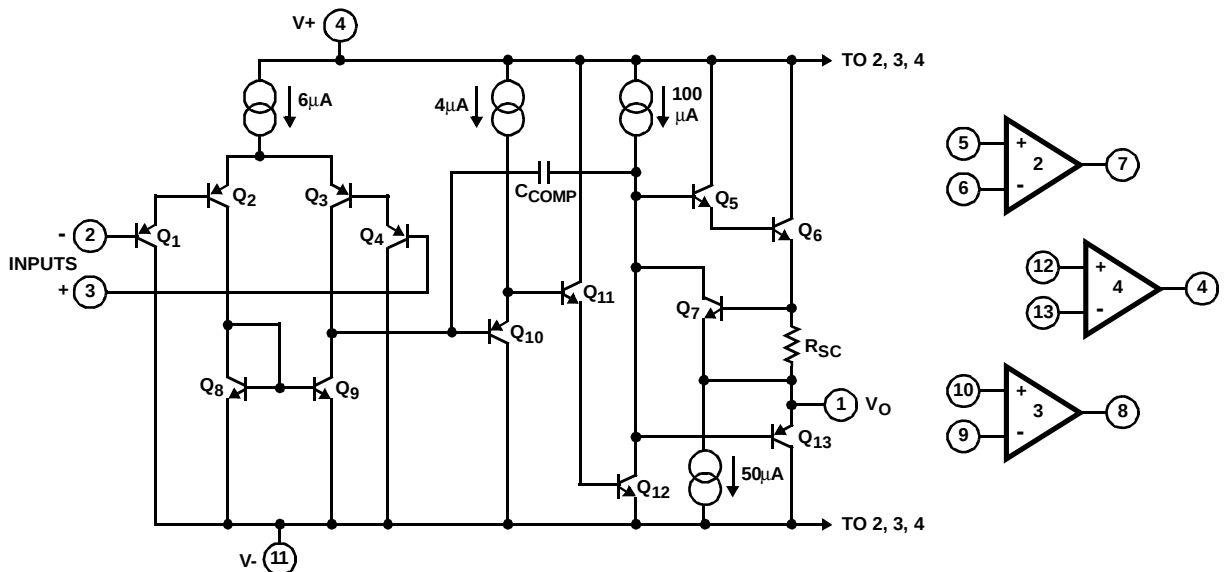
Electrical Specifications Values Apply for Each Operational Amplifier. Supply Voltage $V_+ = 5V$, $V_- = 0V$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	CA124			CA224, CA324, LM324			LM2902			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
Output Voltage Swing	High Level	R _L = 2kΩ	25	0	-	V+ -1.5	0	-	V+ -1.5	-	-	-	V
		R _L = 2kΩ, V+ = 30V	Full	26	-	-	26	-	-	-	-	-	V
		R _L = 2kΩ, V+ = 26V	Full	-	-	-	-	-	-	22	-	-	V
		R _L = 10kΩ, V+ = 30V	Full	27	28	-	27	28	-	23	28	-	V
	Low Level	R _L = 10kΩ	Full	-	5	20	-	5	20	-	5	100	mV
Output Current	Source	V _{I+} = +1V, V _{I-} = 0V, V+ = 15V	25	20	40	-	20	40	-	-	-	-	mA
		V _{I+} = 1V, V _{I-} = 0, V+ = 15V	Full	10	20	-	10	20	-	10	20	-	mA
	Sink	V _{I+} = 0V, V _{I-} = 1V, V+ = 15V	25	10	20	-	10	20	-	-	-	-	mA
		V _{I+} = 0V, V _{I-} = 1V, V _O = 200mV	25	12	50	-	12	50	-	-	-	-	μA
		V _{I-} = 1V, V _{I+} = 0, V+ = 15V	Full	5	8	-	5	8	-	5	8	-	mA
Crosstalk	f = 1 to 20kHz (Input Referred)	25	-	-120	-	-	-120	-	-	-	-	dB	
Total Supply Current	R _L = ∞	Full	-	0.8	2	-	0.8	2	-	0.7	1.2	mA	
	R _L = ∞, V+ = 26V	Full	-	-	-	-	-	-	-	1.5	3	mA	

NOTES:

- Due to the PNP input stage the direction of the input current is out of the IC. No loading change exists on the input lines because the current is essentially constant, independent of the state of the output.
- The input signal voltage and the input common mode voltage should not be allowed to go negative by more than 0.3V. The positive limit of the common mode voltage range is $V_+ - 1.5V$, but either or both inputs can go to $+32V$ without damage.
- $V_O = 1.4V$, $R_S = 0\Omega$ with V_+ from 5V to 30V, and over the full input common mode voltage range (0V to $V_+ - 1.5V$).

Schematic Diagram (One of Four Operational Amplifiers)



Typical Performance Curves

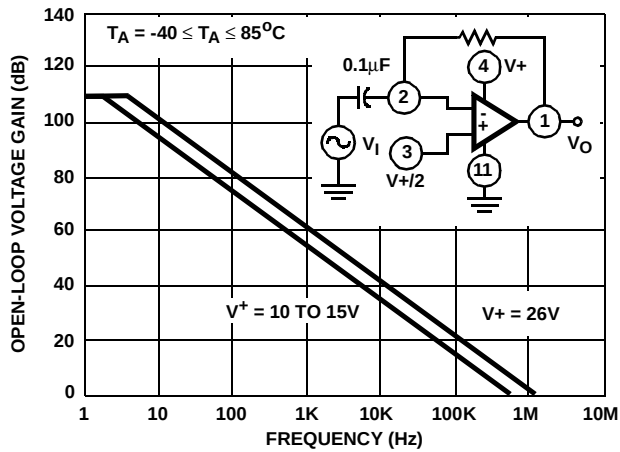


FIGURE 1. OPEN LOOP FREQUENCY RESPONSE

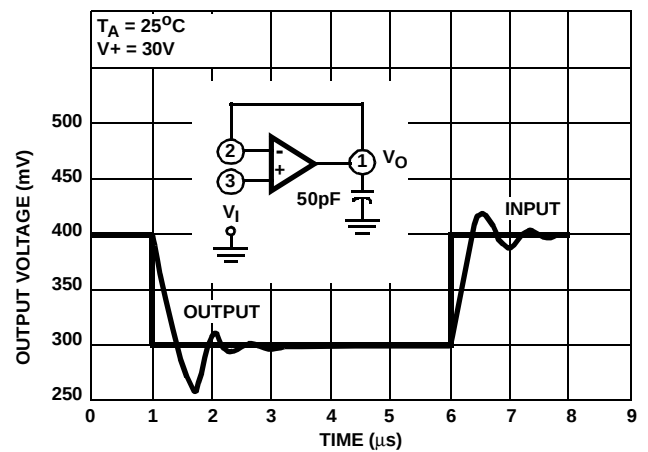


FIGURE 2. VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)

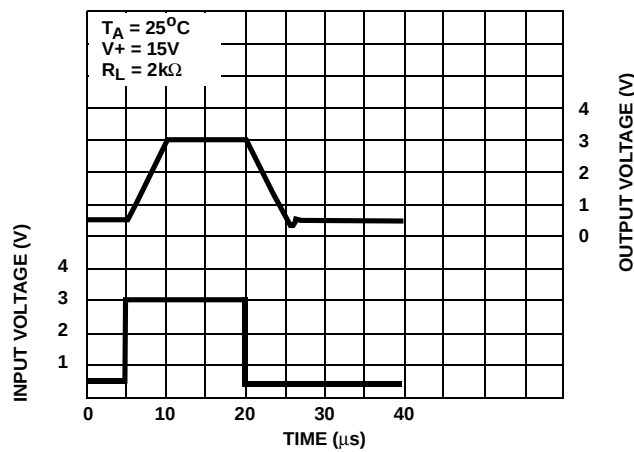


FIGURE 3. VOLTAGE FOLLOWER PULSE RESPONSE (LARGE SIGNAL)

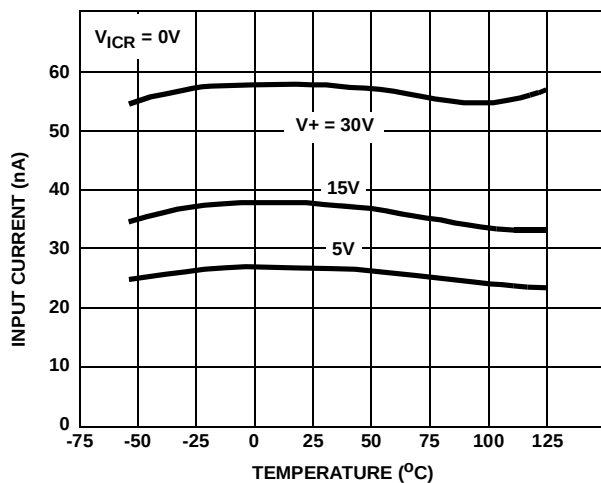


FIGURE 4. INPUT CURRENT vs AMBIENT TEMPERATURE

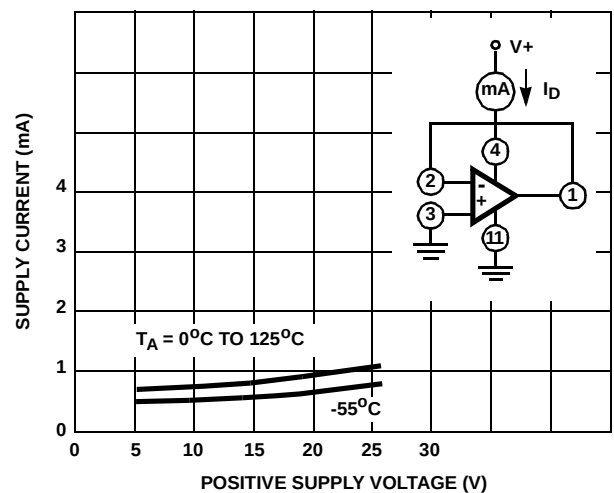


FIGURE 5. SUPPLY CURRENT vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

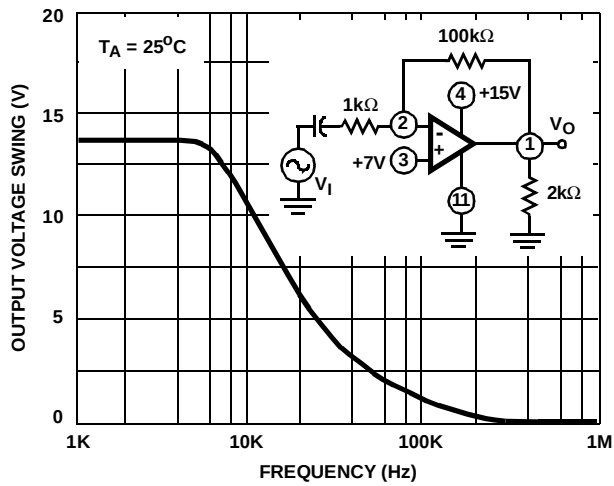


FIGURE 6. LARGE SIGNAL FREQUENCY RESPONSE

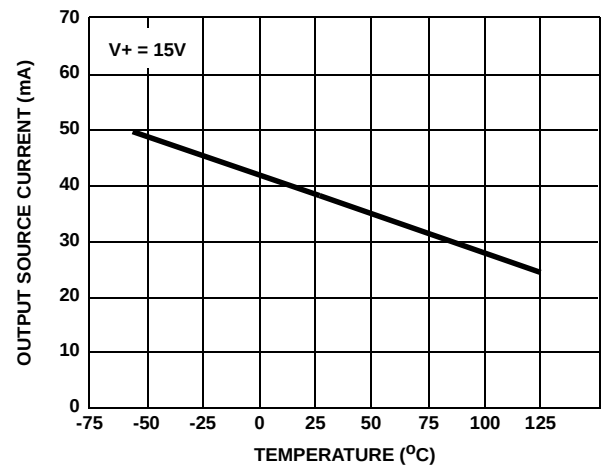


FIGURE 7. OUTPUT CURRENT vs AMBIENT TEMPERATURE

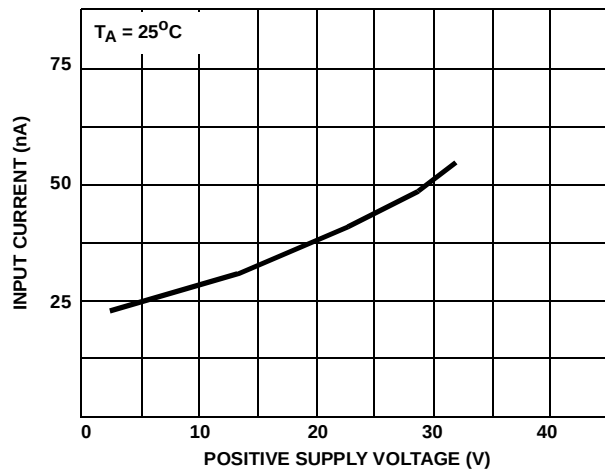


FIGURE 8. INPUT CURRENT vs SUPPLY VOLTAGE

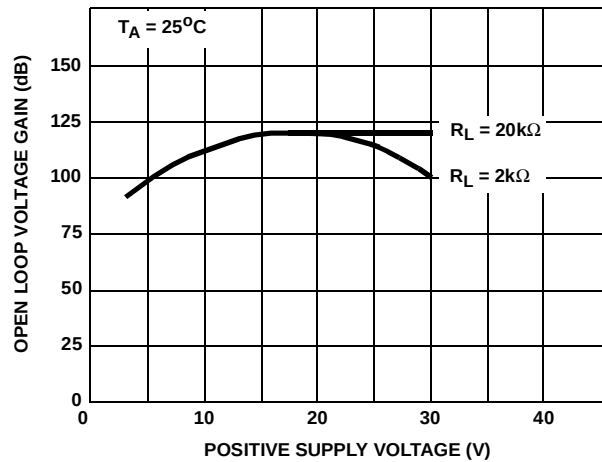
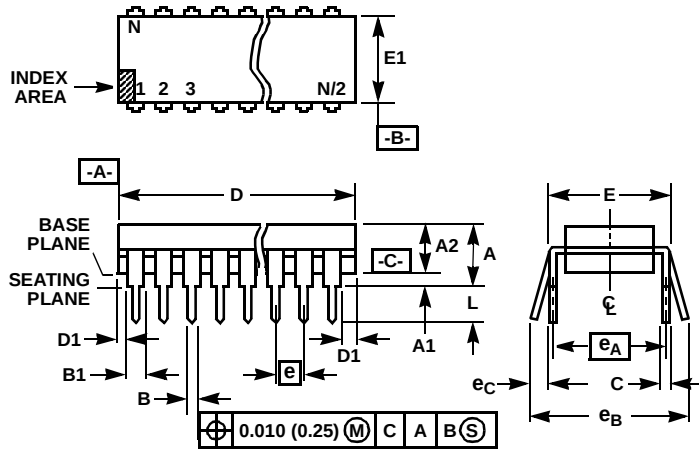


FIGURE 9. VOLTAGE GAIN vs SUPPLY VOLTAGE

Dual-In-Line Plastic Packages (PDIP)



NOTES:

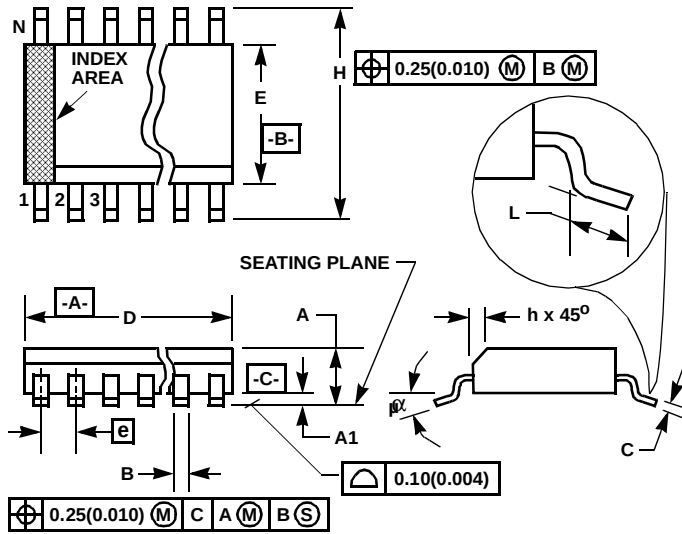
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum $-C-$.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E14.3 (JEDEC MS-001-AA ISSUE D) 14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

Rev. 0 12/93

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M14.15 (JEDEC MS-012-AB ISSUE C) 14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

All Intersil products are manufactured, assembled and tested utilizing ISO9000 quality systems.

Intersil Corporation's quality certifications can be viewed at website www.intersil.com/design/quality/iso.asp.

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site www.intersil.com

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
2401 Palm Bay Rd.
Palm Bay, FL 32905
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil Ltd.
8F-2, 96, Sec. 1, Chien-kuo North,
Taipei, Taiwan 104
Republic of China
TEL: 886-2-2515-8508
FAX: 886-2-2515-8369