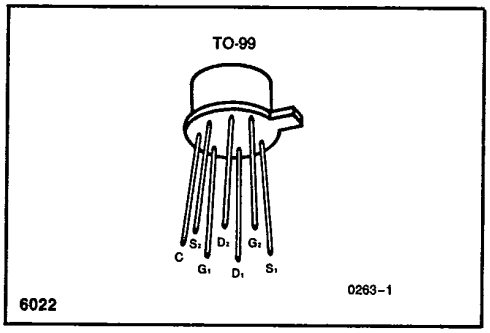
T-31-25

# U257
## Dual N-Channel JFET High Frequency Amplifier



### FEATURES
- $g_{fs} > 4500\mu s$ From DC to 100MHz
- Matched $V_{GS}$, $g_{fs}$ and $g_{os}$

### PIN CONFIGURATION




### ABSOLUTE MAXIMUM RATINGS
($T_A$ = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage (Note 1) ..... −25V
Gate Current (Note 1) ..... 50mA
Storage Temperature Range ..... −65°C to +200°C
Operating Temperature Range ..... −55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

| | One Side | Both Sides |
|---|---|---|
| Power Dissipation ($T_A$ = 85°C) ..... | 250mW | 500mW |
| Derate above 25°C | 3.8mW/°C | 7.7mW/°C |

**NOTE:** *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

### ORDERING INFORMATION

| TO-99 |
|---|
| U257 |

### ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C unless otherwise specified)

| Symbol | Parameter | Test Conditions | | Min | Max | Units |
|---|---|---|---|---|---|---|
| $I_{GSS}$ | Gate Reverse Current | $V_{GS}$ = 15V, $V_{DS}$ = 0 | | | −100 | pA |
| | | | $T_A$ = 150°C | | −250 | nA |
| $BV_{GSS}$ | Gate-Source Breakdown Voltage | $I_G$ = −1μA, $V_{DS}$ = 0 | | −25 | | V |
| VGS(off) | Gate-Source Cutoff Voltage | $V_{DS}$ = 10V, $I_D$ = 1nA | | −1 | −5 | V |
| $I_{DSS}$ | Saturation Drain Current (Note 2) | $V_{DS}$ = 10V, $V_{GS}$ = 0 | | 5 | 40 | mA |
| $g_{fs}$ | Common-Source Forward Transconductance | $V_{DS}$ = 10V, $I_D$ = 5mA | f = 1kHz | 4500 | 10,000 | μs |
| $g_{fs}$ | Common-Source Forward Transconductance | $V_{DG}$ = 10V, $I_D$ = 5mA | f = 100MHz (Note 3) | 4500 | 10,000 | |
| $g_{os}$ | Common-Source Output Conductance | $V_{DS}$ = 10V, $I_D$ = 5mA | f = 1kHz | | 200 | |
| $g_{oss}$ | Common-Source Output Conductance | $V_{DG}$ = 10V, $I_D$ = 5mA | f = 100MHz | | 200 | |
| $C_{iss}$ | Common-Source Input Capacitance | | f = 1MHz | | 5 | pF |
| $C_{rss}$ | Common-Source Reverse Transfer Capacitance | | | | 1.2 | |
| $\overline{e_n}$ | Equivalent Input Noise Voltage | (Note 3) | f = 10kHz | | 30 | $\frac{nV}{\sqrt{Hz}}$ |
| $\frac{I_{DSS1}}{I_{DSS2}}$ | Drain Current Ratio at Zero Gate Voltage (Note 2) | $V_{DS}$ = 10V, $V_{GS}$ = 0 | | 0.85 | 1 | |
| $\lvert V_{GS1} - V_{GS2} \rvert$ | Differential Gate-Source Voltage | $V_{DG}$ = 10V, $I_D$ = 5mA | | | 100 | mV |
| $\frac{g_{fs1}}{g_{fs2}}$ | Transconductance Ratio | | f = 1kHz | 0.85 | 1 | |
| $\lvert g_{os1} - g_{os2} \rvert$ | Differential Output Conductance | | | | 20 | μs |

**NOTES:** 1. Per transistor.
2. Pulse test required, pulse width = 300μs, duty cycle ≤ 3%.
3. For design reference only, not 100% tested.

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*NOTE: All typical values have been characterized but are not tested.*