Dual/Quad Low Power Precision, Picoamp Input Op Amps

FEATURES

- S8 Package – Standard Pinout
- Offset Voltage – Prime Grade: 60μV Max
- Offset Voltage – Low Cost Grade (Including Surface Mount Dual/Quad): 75μV Max
- Offset Voltage Drift: 0.5μV/°C Max
- Input Bias Current: 250pA Max
- 0.1Hz to 10Hz Noise: 0.3μV_{P-P}, 2.2pA_{P-P}
- Supply Current per Amplifier: 400μA Max
- CMRR: 120dB Min
- Voltage Gain: 1 Million Min
- Guaranteed Specs with ±1.0V Supplies
- Guaranteed Matching Specifications
- LT1114 in Narrow Surface Mount Package

APPLICATIONS

- Picoampere/Microvolt Instrumentation
- Two and Three Op Amp Instrumentation Amplifers
- Thermocouple and Bridge Amplifiers
- Low Frequency Active Filters
- Photo Current Amplifiers
- Battery-Powered Systems

DESCRIPTION

The LT1112 dual and LT1114 quad op amps achieve a new standard in combining low cost and outstanding precision specifications.

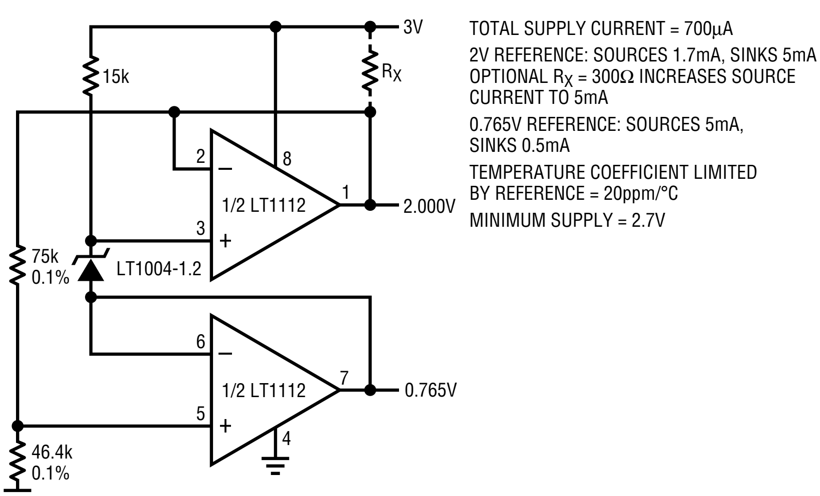
The performance of the selected prime grades matches or exceeds competitive devices. In the design of the LT1112/ LT1114 however, particular emphasis has been placed on optimizing performance in the low cost plastic and SO packages. For example, the 75μV maximum offset voltage in these low cost packages is the lowest on any dual or quad non-chopper op amp.

The LT1112/LT1114 also provide a full set of matching specifications, facilitating their use in such matching dependent applications as two and three op amp instrumentation amplifiers.

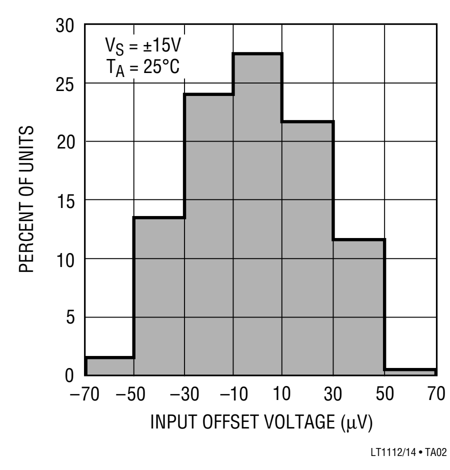
Another set of specifications is furnished at ±1V supplies. This, combined with the low 320μA supply current per amplifier, allows the LT1112/LT1114 to be powered by two nearly discharged AA cells.

Protected by U.S. Patents 4,575,685; 4,775,884 and 4,837,496

Dual Output, Buffered Reference (On Single 3V Supply)



Distribution of Input Offset Voltage (In All Packages)



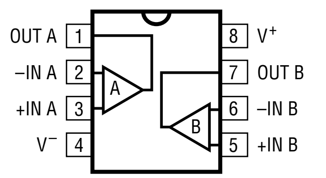
ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ±20V
Differential Input Current (Note 1) .... ±10mA
Input Voltage (Equal to Supply Voltage) .... ±20V
Output Short-Circuit Duration .... Indefinite
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec)................ 300°C

Operating Temperature Range
LT1112AM/LT1112M
LT1114AM/LT1114M .... −55°C to 125°C
LT1112AC/LT1112C/LT1112S8
LT1114AC/LT1114C/LT1114S .... −40°C to 85°C

PACKAGE/ORDER INFORMATION

TOP VIEW

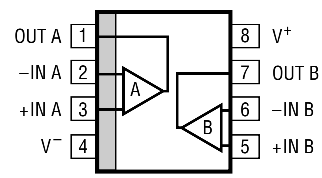


J8 PACKAGE 8-LEAD CERAMIC DIP
N8 PACKAGE 8-LEAD PLASTIC DIP

T_{JMAX} = 160°C, θ_{JA} = 100°C/W (J8)
T_{JMAX} = 140°C, θ_{JA} = 130°C/W (N8)

ORDER PART NUMBER
LT1112AMJ8
LT1112MJ8
LT1112ACN8
LT1112CN8

TOP VIEW

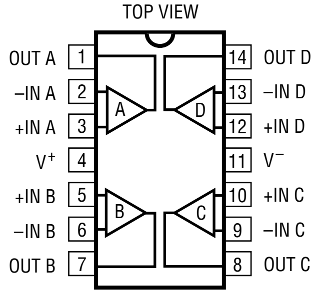


S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 140°C, θ_{JA} = 190°C/W

ORDER PART NUMBER
LT1112S8
PART MARKING
1112

TOP VIEW

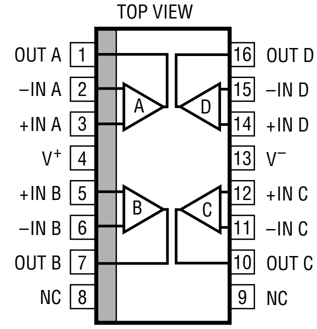


J PACKAGE 14-LEAD CERAMIC DIP
N PACKAGE 14-LEAD PLASTIC DIP

T_{JMAX} = 160°C, θ_{JA} = 80°C/W (J)
T_{JMAX} = 140°C, θ_{JA} = 110°C/W (N)

ORDER PART NUMBER
LT1114AMJ
LT1114MJ
LT1114ACN
LT1114CN

TOP VIEW



S PACKAGE
16-LEAD PLASTIC SO (NARROW)

T_{JMAX} = 140°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LT1114S

ELECTRICAL CHARACTERISTICS

V_S = ±15V, V_{CM} = 0V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 2)	LT1112AM/AC LT1114AM/AC MIN	TYP	MAX	LT1112M/C/S8 LT1114M/C/S MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage			20	60		25	75	µV
		V_S = ±1.0V		40	110		45	130	µV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability			0.3			0.3		µV/Mo
I_{OS}	Input Offset Current			50	180		60	230	pA
		LT1114S					75	330	pA
I_B	Input Bias Current			±70	±250		±80	±280	pA
		LT1114S					±100	±450	pA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 9)		0.3	0.9		0.3	0.9	μV_{P-P}

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $V_{CM} = 0V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 2)	LT1112AM/AC LT1114AM/AC MIN	TYP	MAX	LT1112M/C/S8 LT1114M/C/S MIN	TYP	MAX	UNITS
	Input Noise Voltage Density	f_O = 10Hz (Note 9) f_O = 1000Hz (Note 9)		16 14	28 18		16 14	28 18	nV/√Hz nV/√Hz
i_n	Input Noise Current	0.1Hz to 10Hz		2.2			2.2		pA_{P-P}
	Input Noise Current Density	f_O = 10Hz f_O = 1000Hz		0.030 0.008			0.030 0.008		pA/√Hz pA/√Hz
V_{CM}	Input Voltage Range		±13.5	±14.3		±13.5	±14.3		V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±13.5V	120	136		115	136		dB
PSRR	Power Supply Rejection Ratio	V_S = ±1.0V to ±20V	116	126		114	126		dB
	Minimum Supply Voltage	(Note 4)	±1.0			±1.0			V
R_{IN}	Input Resistance Differential Mode Common Mode	 (Note 3)	 20	 50 800		 15	 40 700		 MΩ GΩ
A_{VOL}	Large-Signal Voltage Gain	V_O = ±12V, R_L = 10kΩ V_O = ±10V, R_L = 2kΩ	1000 800	5000 1500		800 600	5000 1300		V/mV V/mV
V_{OUT}	Output Voltage Swing	R_L = 10kΩ R_L = 2kΩ	±13.0 ±11.0	±14.0 ±12.4		±13.0 ±11.0	±14.0 ±12.4		V V
SR	Slew Rate		0.16	0.30		0.16	0.30		V/µs
GBW	Gain-Bandwidth Product	f_O = 10kHz	450	750		450	750		kHz
I_S	Supply Current per Amplifier	 V_S = ±1.0V		350 320	400 370		350 320	450 420	µA µA
	Channel Separation	f_O = 10Hz		150			150		dB
ΔV_{OS}	Offset Voltage Match	(Note 5)		35	100		40	130	µV
ΔI_B^+	Noninverting Bias Current Match (Notes 5, 6)	 LT1114S		100	450		100 120	500 680	pA pA
ΔCMRR	Common-Mode Rejection Match	(Notes 5, 7)	117	136		113	136		dB
ΔPSRR	Power Supply Rejection Match	(Notes 5, 7)	114	130		112	130		dB

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $-55°C \le T_A \le 125°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 2)		LT1112AMJ8 LT1114AMJ MIN	TYP	MAX	LT1112MJ8 LT1114MJ MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	 V_S = ±1.2V	● ●		35 60	120 220		45 70	150 260	µV µV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 8)	●		0.15	0.5		0.20	0.75	µV/°C
I_{OS}	Input Offset Current		●		80	400		100	500	pA
I_B	Input Bias Current		●		±150	±600		±170	±700	pA
V_{CM}	Input Voltage Range		●	±13.5	±14.1		±13.5	±14.1		V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±13.5V	●	116	130		111	130		dB
PSRR	Power Supply Rejection Ratio	V_S = ±1.2V to ±20V	●	112	124		110	124		dB
A_{VOL}	Large-Signal Voltage Gain	V_O = ±12V, R_L = 10kΩ V_O = ±10V, R_L = 2kΩ	● ●	500 200	2500 600		400 170	2500 500		V/mV V/mV

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $-55°C \le T_A \le 125°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 2)		LT1112AMJ8 LT1114AMJ MIN	TYP	MAX	LT1112MJ8 LT1114MJ MIN	TYP	MAX	UNITS
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	●	±13.0	±13.85		±13.0	±13.85		V
SR	Slew Rate		●	0.12	0.22		0.12	0.22		V/µs
I_S	Supply Current per Amplifier		●		380	460		380	530	µA
ΔV_{OS}	Offset Voltage Match	(Note 5)	●		55	200		70	240	µV
	Offset Voltage Match Drift	(Notes 5, 8)	●		0.2	0.7		0.3	1.0	µV/°C
ΔI_B^+	Noninverting Bias Current Match	(Notes 5, 6)	●		150	750		170	850	pA
ΔCMRR	Common-Mode Rejection Ratio	(Notes 5, 7)	●	112	130		106	130		dB
ΔPSRR	Power Supply Rejection Ratio	(Notes 5, 7)	●	109	126		106	126		dB

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 2)		LT1112ACN8 LT1114ACN MIN	TYP	MAX	LT1112N8/S8 LT1114CN/S MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT1112N8	●		27	100		30	125	µV
		LT1112S8, LT1114N/S	●		35	125		45	150	µV
		$V_S = \pm1.2V$	●		50	175		65	210	µV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift (Note 8)	LT1112N8	●		0.15	0.5		0.2	0.75	µV/°C
		LT1112S8, LT1114N/S	●		0.3	1.1		0.4	1.3	µV/°C
I_{OS}	Input Offset Current		●		60	220		70	290	pA
		LT1114S	●					90	420	pA
I_B	Input Bias Current		●		±80	±300		±90	±350	pA
		LT1114S	●					±115	±550	pA
V_{CM}	Input Voltage Range		●	±13.5	±14.2		±13.5	±14.2		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm13.5V$	●	118	133		113	133		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm1.2V$ to $\pm20V$	●	114	125		112	125		dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm12V$, $R_L = 10k\Omega$	●	800	4000		650	4000		V/mV
		$V_O = \pm10V$, $R_L = 2k\Omega$	●	500	1300		400	1000		V/mV
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	●	±13.0	±13.9		±13.0	±13.9		V
SR	Slew Rate		●	0.14	0.27		0.14	0.27		V/µs
I_S	Supply Current per Amplifier		●		370	440		370	500	µA
ΔV_{OS}	Offset Voltage Match (Note 5)	LT1112N8	●		45	170		55	210	µV
		LT1112S8, LT1114N/S	●		55	220		70	270	µV
	Offset Voltage Match Drift (Notes 5, 8)	LT1112N8	●		0.2	0.7		0.3	1.0	µV/°C
		LT1112S8, LT1114N/S	●		0.4	1.6		0.5	1.9	µV/°C
ΔI_B^+	Noninverting Bias Current Match (Notes 5, 6)		●		120	530		135	620	pA
		LT1114S	●					160	880	pA
ΔCMRR	Common-Mode Rejection Ratio	(Notes 5, 7)	●	114	134		109	134		dB
ΔPSRR	Power Supply Rejection Ratio	(Notes 5, 7)	●	110	128		108	128		dB

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $-40°C \le T_A \le 85°C$, (Note 10)

SYMBOL	PARAMETER	CONDITIONS (Note 2)		LT1112ACN8 LT1114ACN MIN	TYP	MAX	LT1112N8/S8 LT1114CN/S MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT1112N8	●		30	110		35	135	µV
		LT1112S8, LT1114N/S	●		40	135		45	160	µV
		$V_S = \pm1.2V$	●		55	200		60	240	µV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	LT1112N8	●		0.15	0.50		0.20	0.75	µV/°C
		LT1112S8, LT1114N/S	●		0.30	1.10		0.40	1.30	µV/°C
I_{OS}	Input Offset Current		●		70	330		85	400	pA
		LT1114S	●					110	600	pA
I_B	Input Bias Current		●		±110	±500		±120	±550	pA
		LT1114S	●					±150	±800	pA
V_{CM}	Input Voltage Range		●	±13.5	±14.1		±13.5	±14.1		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm13.5V$	●	117	132		112	132		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm1.2V$ to $\pm20V$	●	113	125		111	125		dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm12V$, $R_L = 10k\Omega$	●	700	3300		600	3300		V/mV
		$V_O = \pm10V$, $R_L = 2k\Omega$	●	400	1100		300	900		V/mV
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	●	±13.0	±13.85		±13.0	±13.85		V
SR	Slew Rate		●	0.13	0.24		0.13	0.24		V/µs
I_S	Supply Current per Amplifier		●		370	450		370	510	µA
ΔV_{OS}	Offset Voltage Match (Note 5)	LT1112N8	●		50	180		60	225	µV
		LT1112S8, LT1114N/S	●		60	230		70	270	µV
	Offset Voltage Match Drift (Notes 5)	LT1112N8	●		0.2	0.7		0.3	1.0	µV/°C
		LT1112S8, LT1114N/S	●		0.4	1.6		0.5	1.9	µV/°C
ΔI_B^+	Noninverting Bias Current Match (Notes 5, 6)		●		140	660		155	770	pA
		LT1114S	●					190	1300	pA
ΔCMRR	Common-Mode Rejection Ratio	(Notes 5, 7)	●	113	133		109	133		dB
ΔPSRR	Power Supply Rejection Ratio	(Notes 5, 7)	●	110	127		107	127		dB

The ● denotes specifications which apply over the operating temperature range.

Note 1: Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless limiting resistance is used.

Note 2: Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers; i.e., out of 100 LT1114s (or 100 LT1112s) typically 240 op amps (or 120) will be better than the indicated specification.

Note 3: This parameter is guaranteed by design and is not tested.

Note 4: Offset voltage, supply current and power supply rejection ratio are measured at the minimum supply voltage.

Note 5: Matching parameters are the difference between amplifiers A and D and between B and C on the LT1114; between the two amplifiers on the LT1112.

Note 6: This parameter is the difference between two noninverting input bias currents.

Note 7: ΔCMRR and ΔPSRR are defined as follows: (1) CMRR and PSRR are measured in µV/V on the individual amplifiers. (2) The difference is calculated between the matching sides in µV/V. (3) The result is converted to dB.

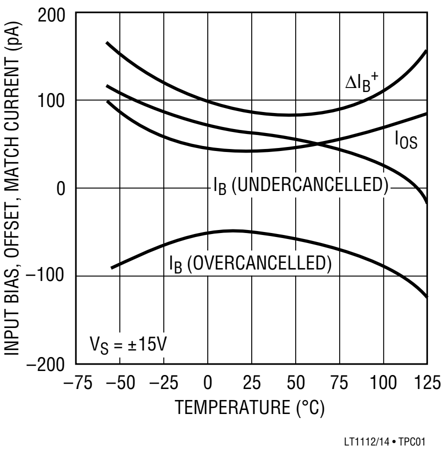
Note 8: This parameter is not 100% tested.

Note 9: These parameters are not tested. More than 99% of the op amps tested during product characterization have passed the maximum limits. 100% passed at 1kHz.

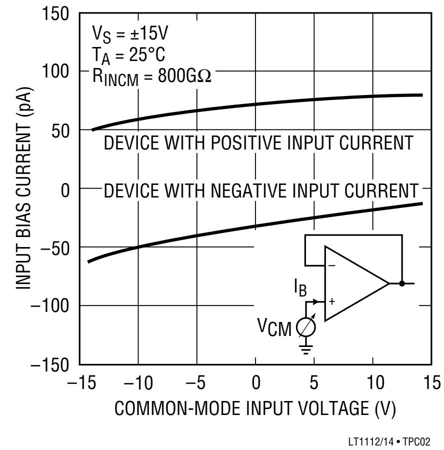
Note 10: The LT1112/LT1114 are not tested and are not quality assurance sampled at –40°C and at 85°C. These specifications are guaranteed by design, correlation and/or inference from –55°C, 0°C, 25°C, 70°C and/or 125°C tests.

TYPICAL PERFORMANCE CHARACTERISTICS

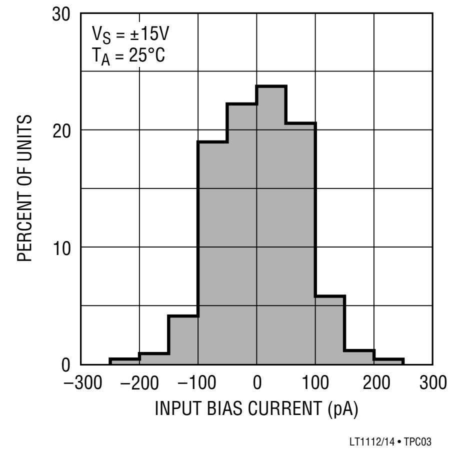
Input Bias and Offset Current, Noninverting Bias Current Match vs Temperature



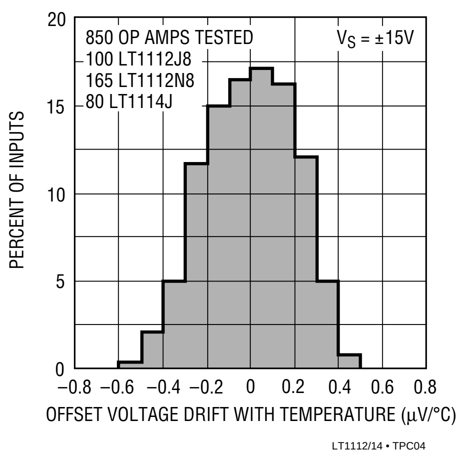
Input Bias Current Over Common-Mode Range



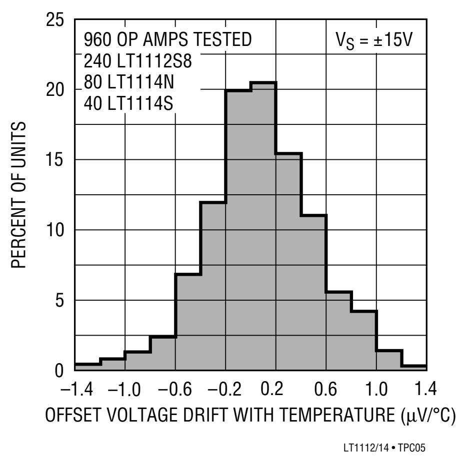
Distribution of Input Bias Current (In All Packages Except LT1114S)



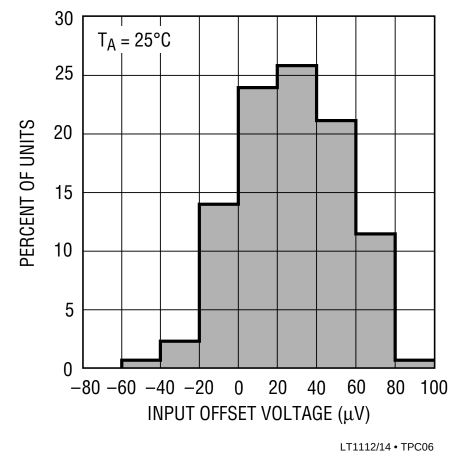
Drift with Temperature LT1112N8/J8, LT1114J



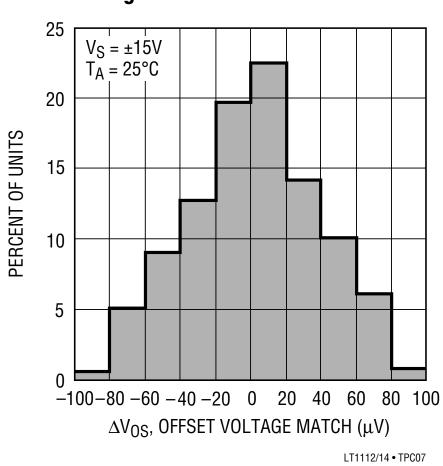
Drift with Temperature LT1112S8, LT1114N/S



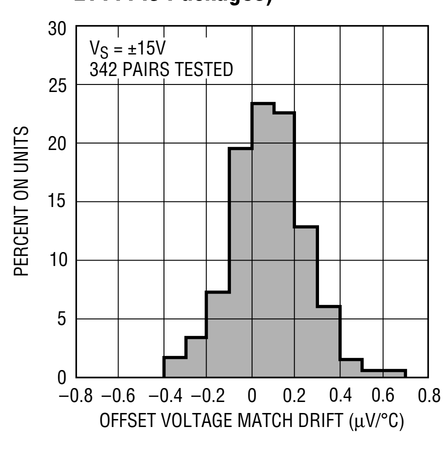
Distribution of Offset Voltage at $V_S = \pm 1.0V$ (In All Packages)



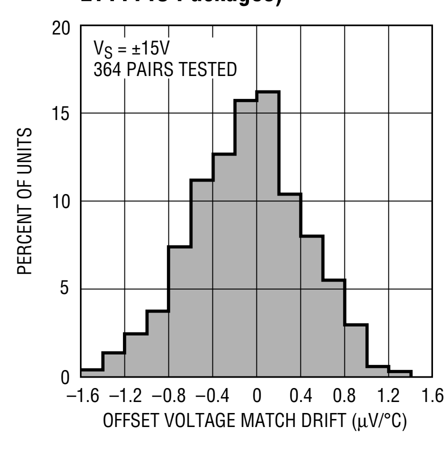
Distribution of Offset Voltage Match



Distribution of Offset Voltage Match Drift (LT1112J8, LT1112N8, LT1114J Packages)

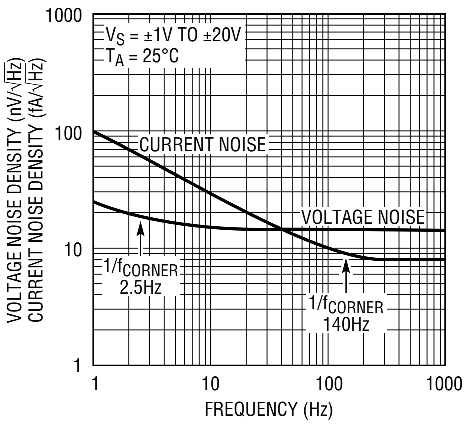


Distribution of Offset Voltage Match Drift (LT1112S8, LT1114N, LT1114S Packages)



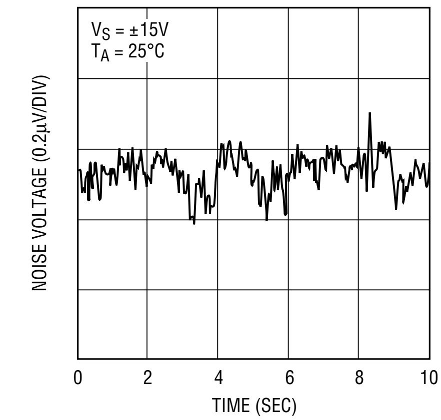
TYPICAL PERFORMANCE CHARACTERISTICS

Noise Spectrum



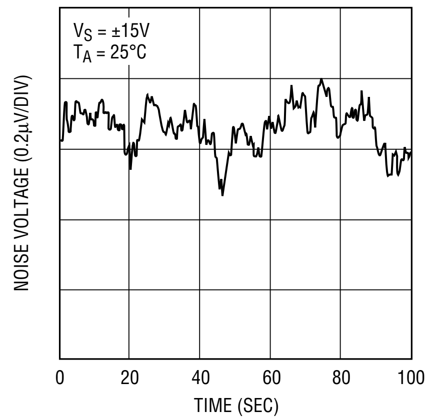
LT1112/14 • TPC10

0.1Hz to 10Hz Noise



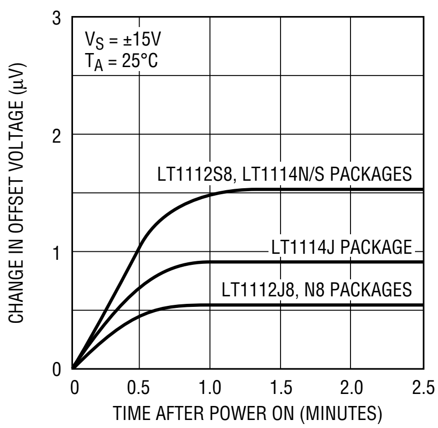
LT1112/14 • TPC11

0.01Hz to 1Hz Noise



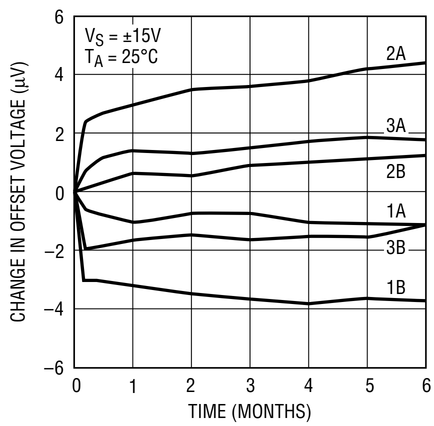
LT1112/14 • TPC12

Warm-Up Drift



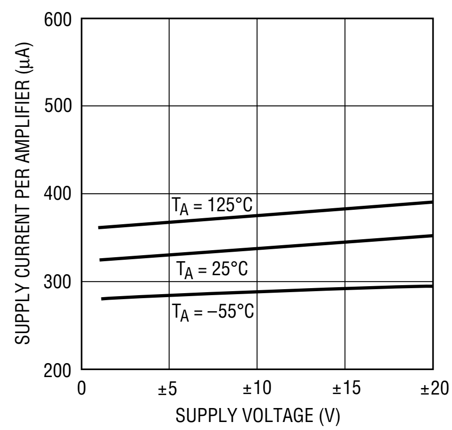
LT1112/14 • TPC13

Long Term Stability of Three Representative Units



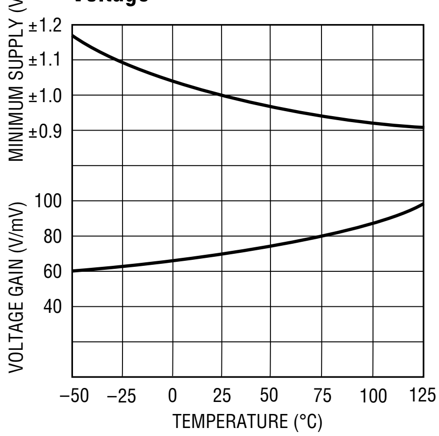
LT1112/14 • TPC14

Supply Current per Amplifier vs Supply Voltage



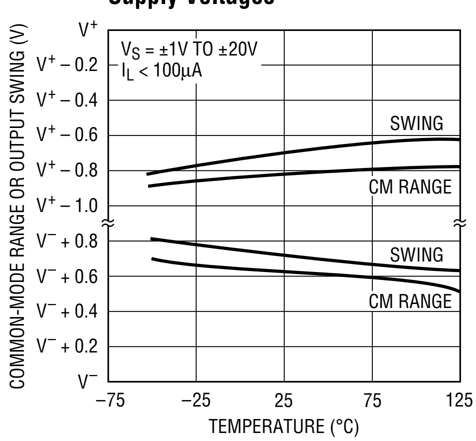
LT1112/14 • TPC15

Minimum Supply Voltage vs Temp Voltage Gain at Minimum Supply Voltage



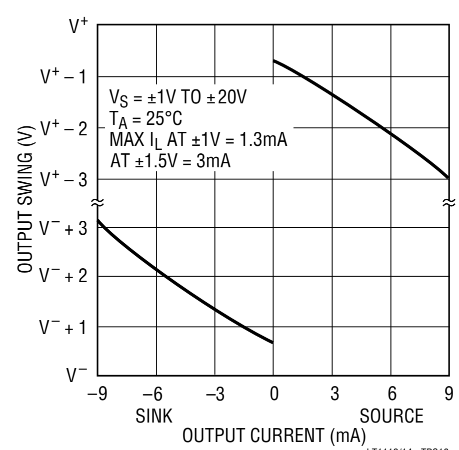
LT1112/14 • TPC16

Common-Mode Range and Voltage Swing with Respect to Supply Voltages



LT1112/14 • TPC17

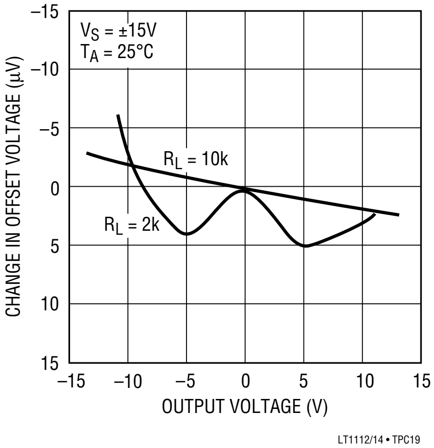
Output Voltage Swing vs Load Current



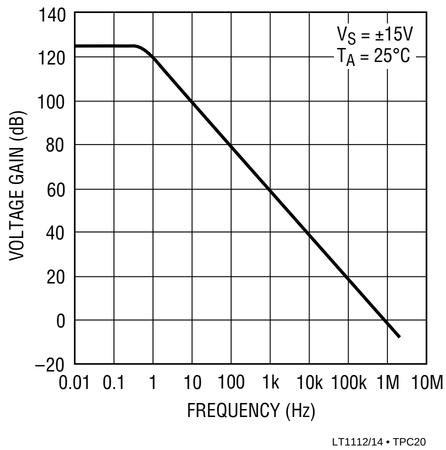
LT1112/14 • TPC18

TYPICAL PERFORMANCE CHARACTERISTICS

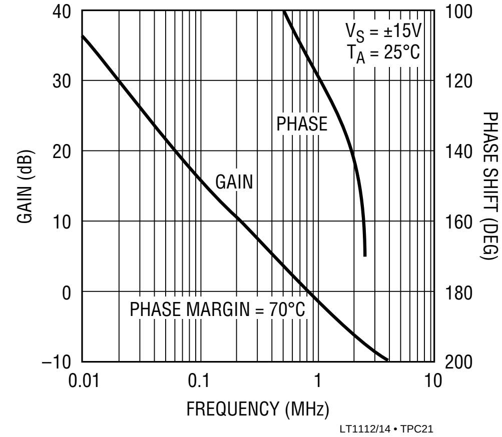
Voltage Gain



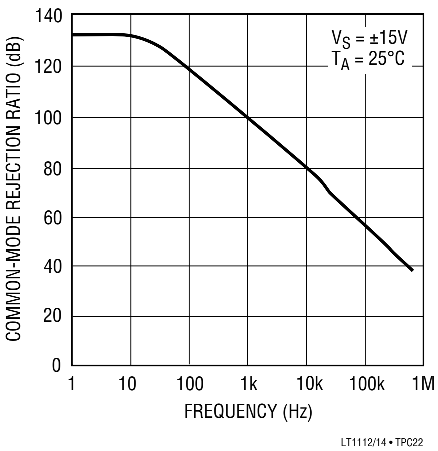
Voltage Gain vs Frequency



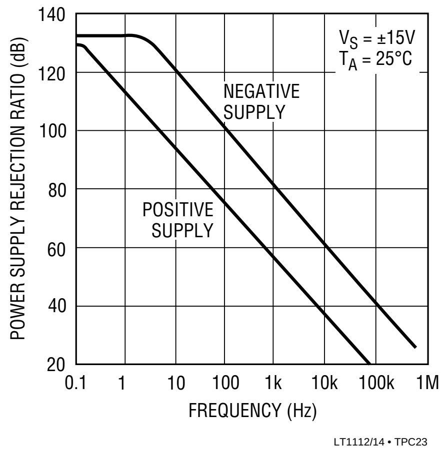
Gain, Phase Shift vs Frequency



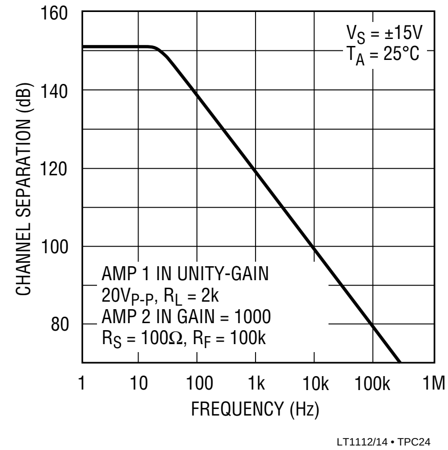
Common-Mode Rejection vs Frequency



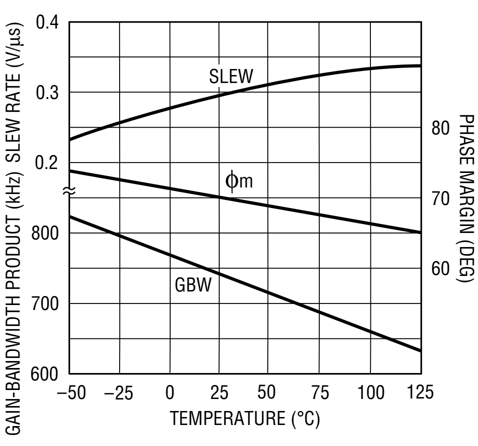
Power Supply Rejection vs Frequency



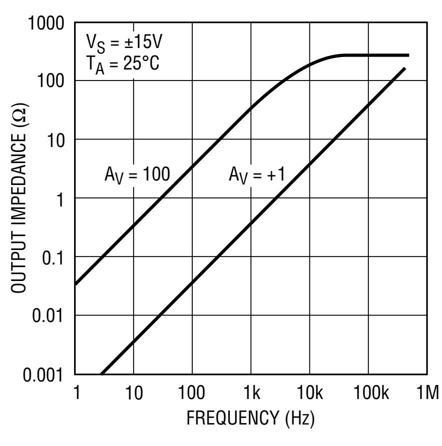
Channel Separation vs Frequency



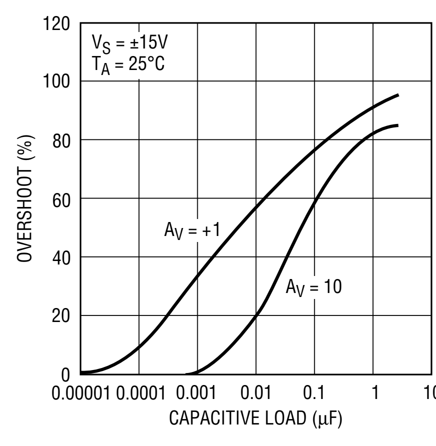
Slew Rate, Gain-Bandwidth Product and Phase Margin vs Temperature



Closed-Loop Output Impedance

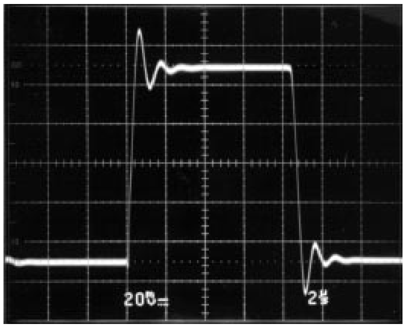


Capacitive Loading Handling



TYPICAL PERFORMANCE CHARACTERISTICS

Small-Signal Transient Response

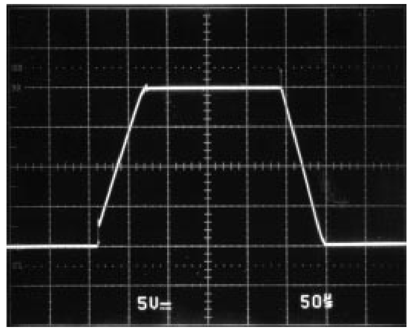


20mV/DIV

2μs/DIV

$A_V = +1$
$C_L = 500pF$
$V_S = \pm15V$

Large-Signal Transient Response

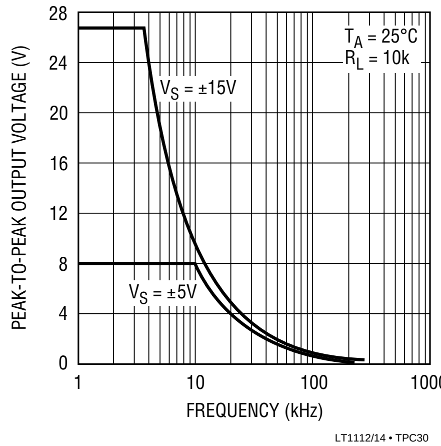


5V/DIV

50μs/DIV

$A_V = +1$
$R_F = 10k$
$C_F = 100pF$
$V_S = \pm15V$

Undistorted Output Voltage vs Frequency



APPLICATIONS INFORMATION

The LT1112 dual and LT1114 quad in the plastic and ceramic DIP packages are pin compatible to and directly replace such precision op amps as the OP-200, OP-297, AD706 duals and OP-400, OP-497, AD704 quads with improved price/performance.

The LT1112 in the S8 surface mount package has the standard pin configuration, i.e., the same configuration as the plastic and ceramic DIP packages.

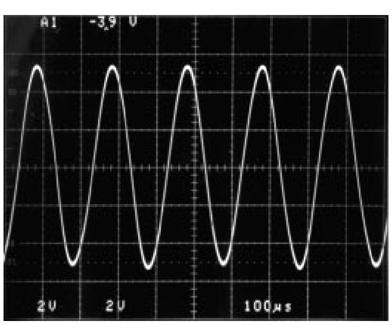
The LT1114 quad is offered in the narrow 16-pin surface mount package. All competitors are in the wide 16-pin package which occupies 1.8 times the area of the narrow package. The wide package is also 1.8 times thicker than the narrow package.

The inputs of the LT1112/1114 are protected with back-to-back diodes. In the voltage follower configuration, when the input is driven by a fast large-signal pulse (>1V), the input protection diodes effectively short the output to the input during slewing, and a current, limited only by the output short-circuit protection, will flow through the diodes.

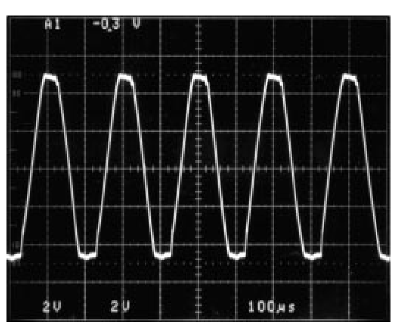
The use of a feedback resistor is recommended because this resistor keeps the current below the short-circuit limit, resulting in faster recovery and settling of the output.

The input voltage of the LT1112/1114 should never exceed the supply voltages by more than a diode drop. However, the example below shows that as the input voltage exceeds the common-mode range, the LT1112's output clips cleanly, without any glitches or phase reversal. The OP-297 exhibits phase reversal. The photos also illustrate that both the input and output ranges of the LT1112 are within

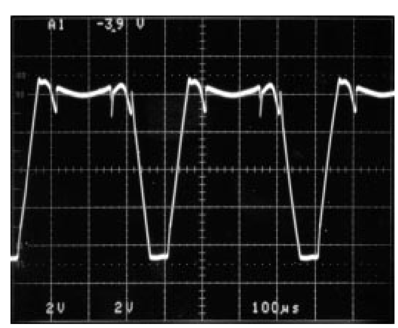
Voltage Follower with Input Exceeding the Common-Mode Range ($V_S = \pm5V$)



INPUT: ±5.2V Sine Wave



LT1112 Output



OP-297 Output

APPLICATIONS INFORMATION

800mV of the supplies. The effect of input and output overdrive on the other amplifiers in the LT1112 or LT1114 packages is negligible, as each amplifier is biased independently.

Advantages of Matched Dual and Quad Op Amps

In many applications the performance of a system depends on the matching between two operational amplifiers rather than the individual characteristics of the two op amps. Two or three op amp instrumentation amplifiers, tracking voltage references and low drift active filters are some of the circuits requiring matching between two op amps.

The well-known triple op amp configuration illustrates these concepts. Output offset is a function of the difference between the offsets of the two halves of the LT1112. This error cancellation principle holds for a considerable number of input referred parameters in addition to offset voltage and its drift with temperature. Input bias current will be the average of the two noninverting input currents (I_B^+). The difference between these two currents (ΔI_B^+) is the offset current of the instrumentation amplifier. Common-mode and power supply rejections will be dependent only on the match between the two amplifiers (assuming perfect resistor matching).

The concepts of common-mode and power supply rejection ratio match (ΔCMRR and ΔPSRR) are best demonstrated with a numerical example:

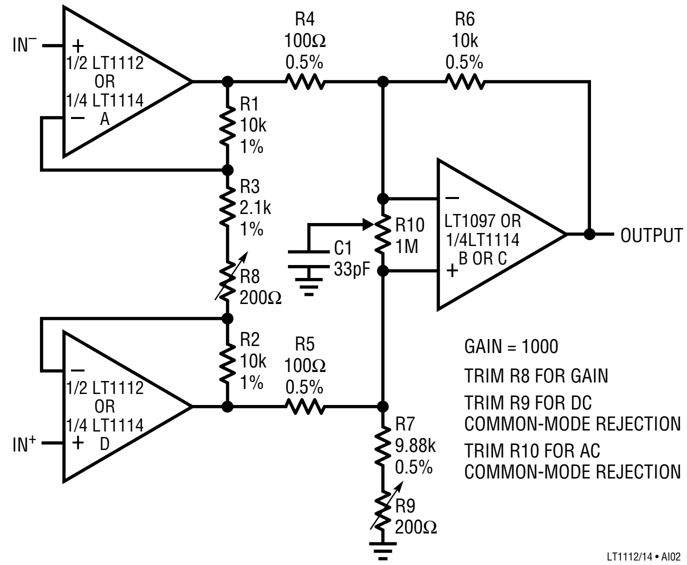
Assume $CMRR_A$ = +1µV/V or 120dB,
and $CMRR_B$ = +0.75µV/V or 122.5dB,
then ΔCMRR = 0.25µV/V or 132dB;
if $CMRR_B$ = –0.75µV/V which is still 122.5dB,
then ΔCMRR = 1.75µV/V or 115dB.

Clearly the LT1112/LT1114, by specifying and guaranteeing all of these matching parameters, can significantly improve the performance of matching-dependent circuits.

Typical performance of the instrumentation amplifier:

Input offset voltage = 35µV
Offset voltage drift = 0.3µV/°C
Input bias current = 80pA
Input offset current = 100pA
Input resistance = 800GΩ
Input noise = 0.42µV_{P-P}

Three Op Amp Instrumentation Amplifier



When the instrumentation amplifier is used with high impedance sources, the LT1114 is recommended because its CMRR vs frequency performance is better than the LT1112's. For example, with two matched 1MΩ source resistors, CMRR at 100Hz is 100dB with the LT1114, 76dB with the LT1112.

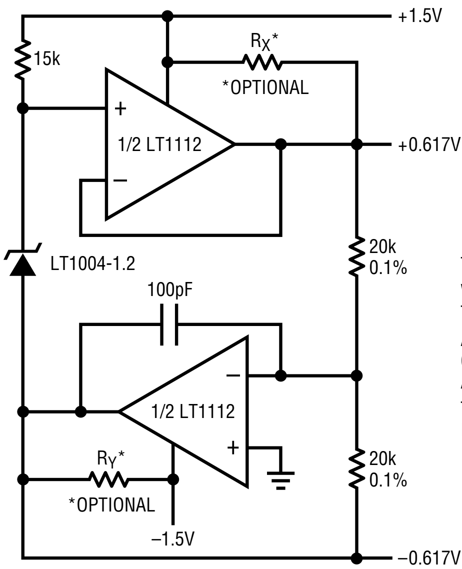
This difference is explained by the fact that capacitance between adjacent pins on an IC package is about 0.25pF (including package, socket and PC board trace capacitances).

On the dual op amp package, positive input A is next to the V^- pin (AC ground), while positive input B has no AC ground pin adjacent to it, resulting in a 0.25pF input capacitance mismatch. At 100Hz, 0.25pF represents a 6.4×10^9 input impedance mismatch, which is only 76dB higher than the 1MΩ source resistors.

On the quad package, all four inputs are adjacent to a power supply terminal–therefore, there is no mismatch.

TYPICAL APPLICATION

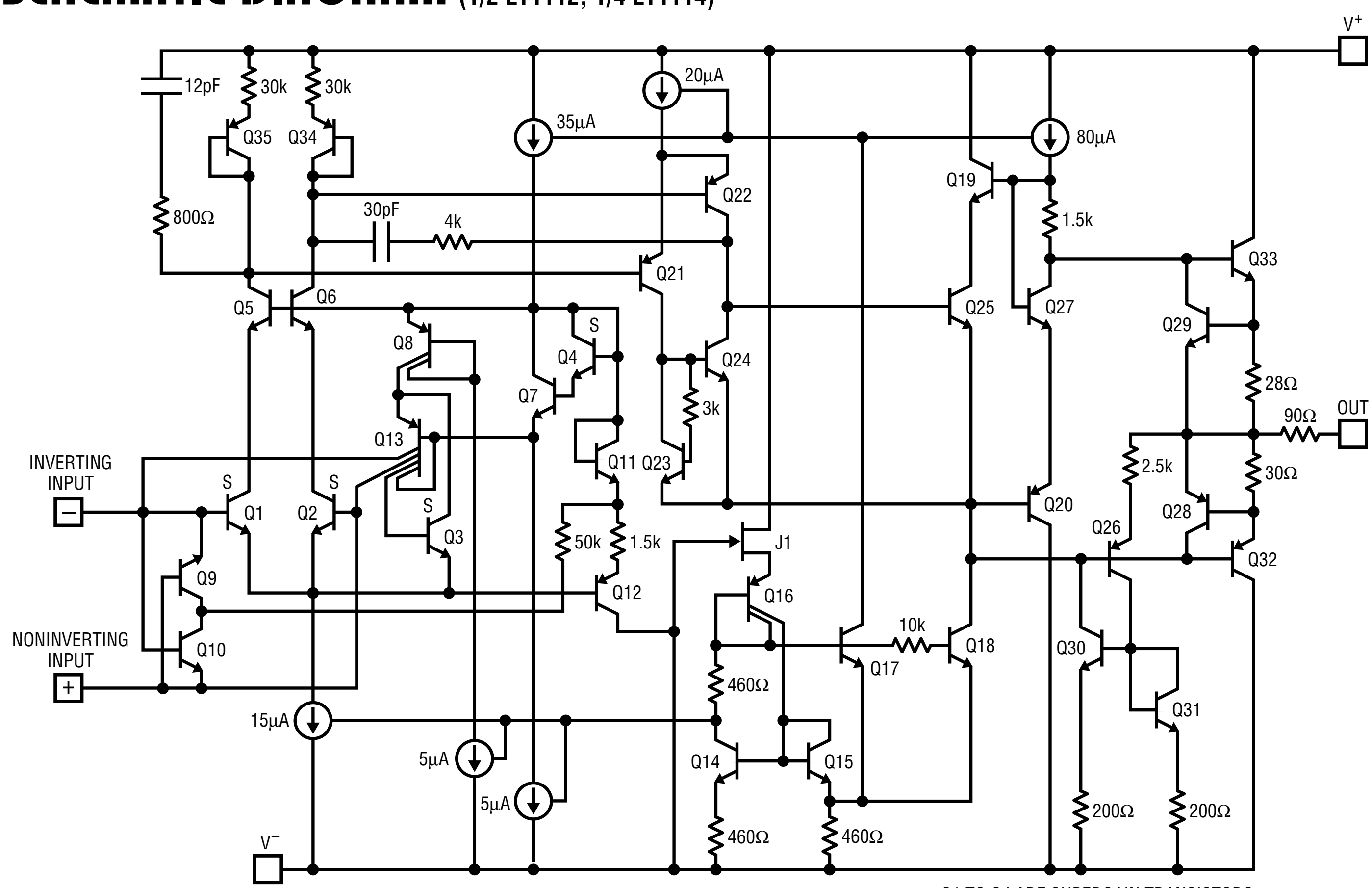
Dual Buffered ±0.617V Reference Powered by Two AA Batteries



TOTAL SUPPLY CURRENT = 700µA
WORKS WITH BATTERIES DISCHARGED TO ±1.3V
AT ±1.5V: MAXIMUM LOAD CURRENT = 800µA; CAN BE INCREASED WITH OPTIONAL R_X, R_Y; AT R_X = R_Y = 750Ω LOAD CURRENT = 2mA
TEMPERATURE COEFFICIENT LIMITED BY REFERENCE = 20ppm/°C

LT1112/14 • TA03

SCHEMATIC DIAGRAM (1/2 LT1112, 1/4 LT1114)

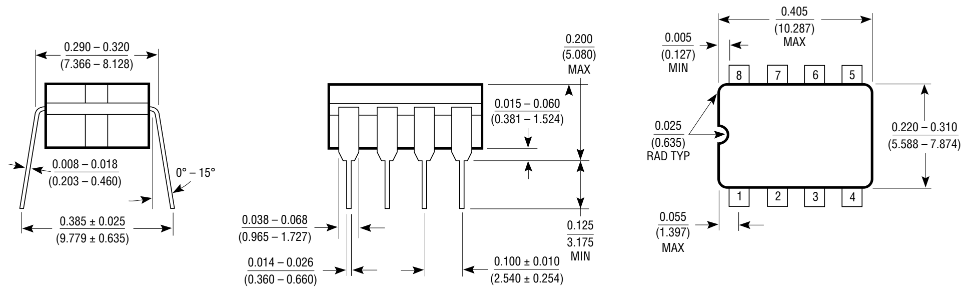


Q1 TO Q4 ARE SUPERGAIN TRANSISTORS

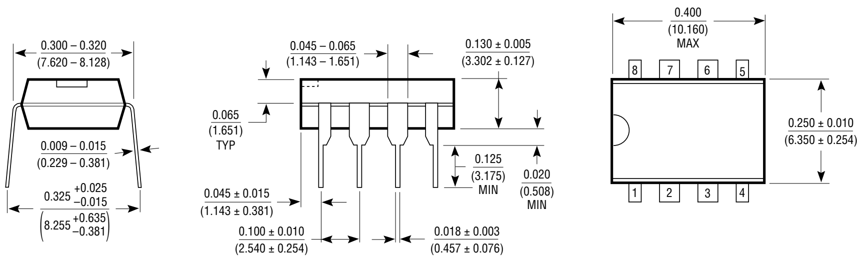
LT1112/14 • SD01

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

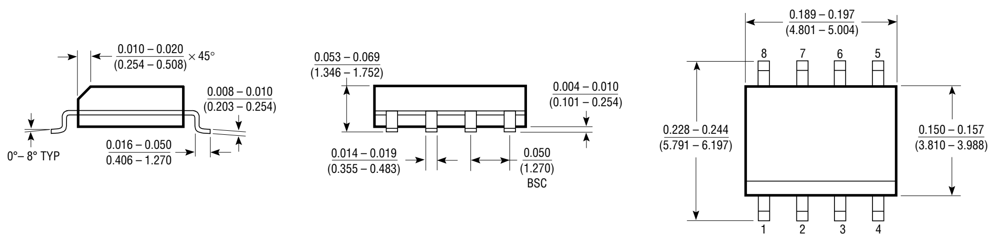
J8 Package
8-Lead Ceramic DIP



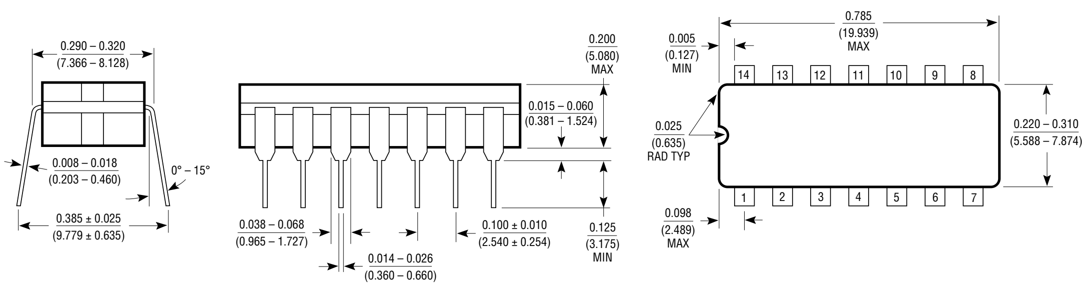
N8 Package
8-Lead Plastic DIP



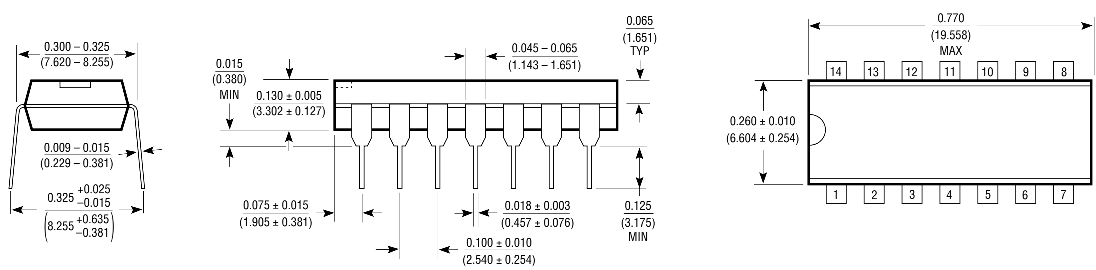
S8 Package
8-Lead Plastic SOIC



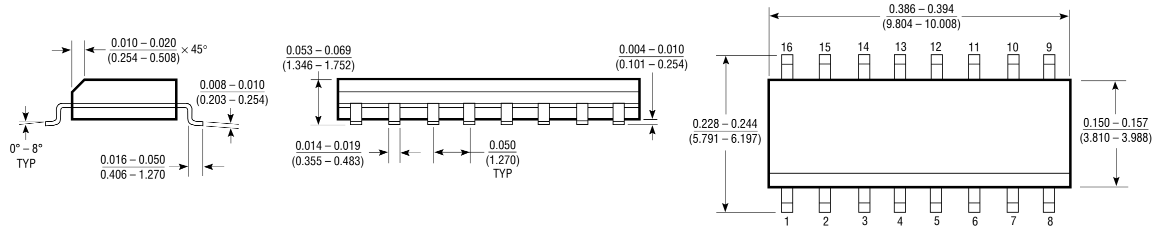
J Package
14-Lead Ceramic DIP



N Package
14-Lead Plastic DIP



S Package
16-Lead Plastic SOIC



Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7487
(408) 432-1900 • FAX: (408) 434-0507 • TELEX: 499-3977

LT/GP 1292 10K REV 0