

Dual and Quad Precision Rail-to-Rail Input and Output Op Amps

FEATURES

- Input Common Mode Range Includes Both Rails
- Output Swings Rail-to-Rail
- Low Input Offset Voltage: 150 μ V
- High Common Mode Rejection Ratio: 90dB
- High A_{VOL} : >1V/ μ V Driving 10k Ω Load
- Low Input Bias Current: 10nA
- Wide Supply Range: 1.8V to \pm 15V
- Low Supply Current: 375 μ A per Amplifier
- High Output Drive: 30mA
- 400kHz Gain-Bandwidth Product
- Slew Rate: 0.13V/ μ s
- Stable for Capacitive Loads up to 1000pF

APPLICATIONS


- Rail-to-Rail Buffer Amplifiers
- Low Voltage Signal Processing
- Supply Current Sensing at Either Rail
- Driving A/D Converters

DESCRIPTION

The LT[®]1366/LT1367/LT1368/LT1369 are dual and quad bipolar op amps which combine rail-to-rail input and output operation with precision specifications. These op amps maintain their characteristics over a supply range of 1.8V to 36V. Operation is specified for 3V, 5V and \pm 15V supplies. Input offset voltage is typically 150 μ V, with an open-loop gain A_{VOL} of 1 million while driving a 10k load. Common mode rejection is typically 90dB over the full rail-to-rail input range, and supply rejection is 110dB.

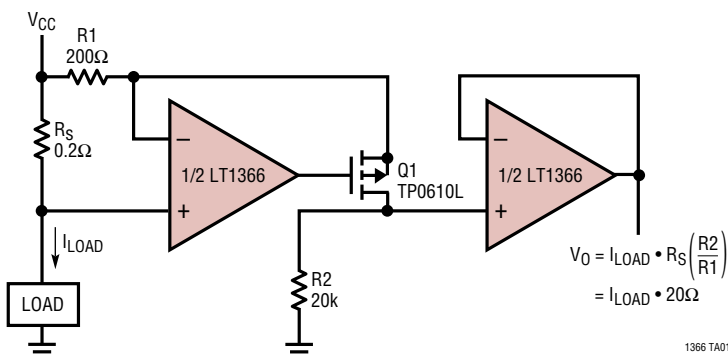
The LT1366/LT1367 have conventional compensation which assures stability for capacitive loads of 1000pF or less. The LT1368/LT1369 have compensation that requires a 0.1 μ F output capacitor, which improves the amplifier's supply rejection and reduces output impedance at high frequencies. The output capacitor's filtering action reduces high frequency noise, which is beneficial when driving A/D converters.

The LT1366/LT1368 are available in plastic 8-pin PDIP and 8-lead SO packages with the standard dual op amp pinout. The LT1367/LT1369 feature the standard quad pinout, which is available in a plastic 14-lead SO package. These devices can be used as plug-in replacements for many standard op amps to improve input/output range and precision.

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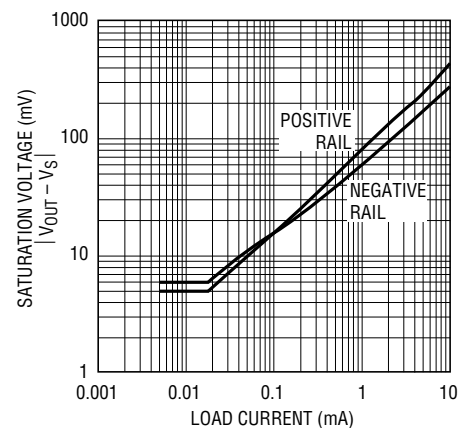
TYPICAL APPLICATION

Positive Supply Rail Current Sense



1366 TA01

Output Saturation Voltage vs Load Current



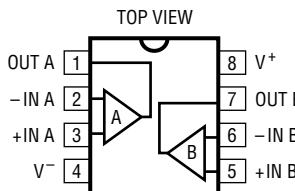
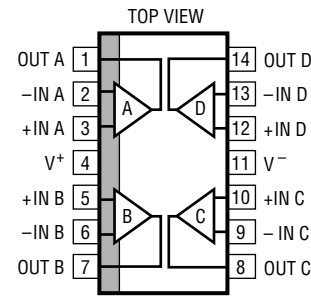
1366 TA02

LT1366/LT1367 LT1368/LT1369

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-)	36V	Junction Temperature	150°C
Input Current	$\pm 15\text{mA}$	Storage Temperature Range	-65°C to 150°C
Output Short-Circuit Duration (Note 1)	Continuous	Lead Temperature (Soldering, 10 sec)	300°C
Operating Temperature Range	-40°C to 85°C		

PACKAGE/ORDER INFORMATION

 <p>N8 PACKAGE 8-LEAD PDIP</p> <p>S8 PACKAGE 8-LEAD PLASTIC SO</p> <p>$T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 130^\circ\text{C/W}$ (N8) $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 190^\circ\text{C/W}$ (S8)</p>	ORDER PART NUMBER	 <p>S PACKAGE 14-LEAD PLASTIC SO</p> <p>$T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 150^\circ\text{C/W}$</p>	ORDER PART NUMBER
	LT1366CN8 LT1366CS8 LT1368CN8 LT1368CS8		LT1367CS LT1369CS
	S8 PART MARKING		
	1366		
	1368		

AVAILABLE OPTIONS

PRODUCT NUMBER	NUMBER OF OP AMPS	LOAD CAPACITANCE	MAX V_{OS} (25°C) AT $V_S = 5\text{V}$, 0V	ORDER PART NUMBER	
				PLASTIC (N)	SURFACE MOUNT(S)
LT1366	2	$0\text{pF} < C_L < 1000\text{pF}$	475 μV	LT1366CN8	LT1366CS8
LT1367	4	$0\text{pF} < C_L < 1000\text{pF}$	800 μV		LT1367CS
LT1368	2	$C_L = 0.1\mu\text{F}$	475 μV	LT1368CN8	LT1368CS8
LT1369	4	$C_L = 0.1\mu\text{F}$	800 μV		LT1369CS

ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, 0V, $V_{CM} = 2.5\text{V}$, $V_O = 2.5\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (LT1366/LT1368)	$V_{CM} = V_{CC}$ $V_{CM} = V_{EE}$		150	475	μV
	Input Offset Voltage (LT1367/LT1369)	$V_{CM} = V_{CC}$ $V_{CM} = V_{EE}$		150	800	μV
ΔV_{OS}	Input Offset Voltage Shift (LT1366/LT1368)	$V_{CM} = V_{EE}$ to V_{CC}		150	400	μV
	Input Offset Voltage Match (Channel to Channel)	$V_{CM} = V_{EE}$, V_{CC} (Notes 3, 4)		250	700	μV
I_B	Input Bias Current	$V_{CM} = V_{CC}$ $V_{CM} = V_{EE}$	0 -35	10 -10	35 0	nA
	Input Bias Current Shift	$V_{CM} = V_{EE}$ to V_{CC}		20	70	nA

ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, 0V , $V_{CM} = 2.5\text{V}$, $V_O = 2.5\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{OS}	Input Offset Current	$V_{CM} = V_{CC}$		1	12	nA
		$V_{CM} = V_{EE}$		0.3	12	nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V_{EE}$ to V_{CC}		1	12	nA
	Input Bias Current Match (Channel to Channel)	$V_{CM} = V_{CC}$ (Note 3) $V_{CM} = V_{EE}$ (Note 3)	0 0	1 1	12 12	nA nA
e_n	Input Noise Voltage Density	$f = 1\text{kHz}$		29		nV/ $\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 1\text{kHz}$		0.07		pA/ $\sqrt{\text{Hz}}$
C_{IN}	Input Capacitance			12		pF
A_{VOL}	Large-Signal Voltage Gain	$V_O = 50\text{mV}$ to 4.8V , $R_L = 10\text{k}$	250	2000		V/mV
CMRR	Common Mode Rejection Ratio (LT1366/LT1368) CMRR Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC} $V_{CM} = V_{EE}$ to V_{CC} (Note 3)	81 75	90 90		dB dB
	Common Mode Rejection Ratio (LT1367/LT1369) CMRR Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC} $V_{CM} = V_{EE}$ to V_{CC} (Note 3)	77 71	90 90		dB dB
PSRR	Power Supply Rejection Ratio	$V_S = 2.0\text{V}$ to 12V , $V_{CM} = V_O = 0.5\text{V}$	90	105		dB
	PSRR Match (Channel to Channel) (Note 3)	$V_S = 2.0\text{V}$ to 12V , $V_{CM} = V_O = 0.5\text{V}$	84	100		dB
V_{OL}	Output Voltage Swing LOW	No Load		6	12	mV
		$I_{SINK} = 0.5\text{mA}$		40	70	mV
		$I_{SINK} = 2.5\text{mA}$		110	200	mV
V_{OH}	Output Voltage Swing HIGH	No Load	$V_{CC} - 0.012$	$V_{CC} - 0.004$		V
		$I_{SOURCE} = 0.5\text{mA}$	$V_{CC} - 0.100$	$V_{CC} - 0.050$		V
		$I_{SOURCE} = 2.5\text{mA}$	$V_{CC} - 0.250$	$V_{CC} - 0.150$		V
I_{SC}	Short-Circuit Current	(Note 1)	± 15	± 30		mA
I_S	Supply Current per Amplifier			340	520	μA
GBW	Gain-Bandwidth Product (LT1366/LT1367)	$A_V = 1000$		0.4		MHz
	Gain-Bandwidth Product (LT1368/LT1369)	$A_V = 1000$		0.16		MHz
t_S	Settling Time (LT1366/LT1367)	$A_V = 1$, $V_{STEP} = 4\text{V}$ to 0.1%		30		μs

$0^\circ\text{C} < T_A < 70^\circ\text{C}$, $V_S = 5\text{V}$, 0V , $V_{CM} = 2.5\text{V}$, $V_O = 2.5\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (LT1366/LT1368)	$V_{CM} = V_{CC}$	●	200	575	μV
		$V_{CM} = V_{EE}$	●	200	575	μV
V_{OS}	Input Offset Voltage (LT1367/LT1369)	$V_{CM} = V_{CC}$	●	200	950	μV
		$V_{CM} = V_{EE}$	●	200	900	μV
$V_{OS\ TC}$	Input Offset Voltage Drift	(Note 2)	●	2	6	$\mu\text{V}/^\circ\text{C}$
ΔV_{OS}	Input Offset Voltage Shift (LT1366/LT1368)	$V_{CM} = V_{EE}$ to V_{CC}	●	200	425	μV
	Input Offset Voltage Match (Channel to Channel)	$V_{CM} = V_{EE}$, V_{CC} (Notes 3, 4)	●	250	900	μV
ΔV_{OS}	Input Offset Voltage Shift (LT1367/LT1369)	$V_{CM} = V_{EE}$ to V_{CC}	●	200	675	μV
	Input Offset Voltage Match (Channel to Channel)	$V_{CM} = V_{EE}$, V_{CC} (Notes 3, 4)	●	250	1900	μV
I_B	Input Bias Current	$V_{CM} = V_{CC}$	●	0	15	nA
		$V_{CM} = V_{EE}$	●	-45	-10	0
ΔI_B	Input Bias Current Shift	$V_{CM} = V_{EE}$ to V_{CC}	●	25	90	nA
I_{OS}	Input Offset Current	$V_{CM} = V_{CC}$	●	2	15	nA
		$V_{CM} = V_{EE}$	●	1	15	nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V_{EE}$ to V_{CC}	●	2	15	nA
	Input Bias Current Match (Channel to Channel)	$V_{CM} = V_{CC}$ (Note 3) $V_{CM} = V_{EE}$ (Note 3)	● ●	0 0	2 1	15 15

ELECTRICAL CHARACTERISTICS

0°C < T_A < 70°C, V_S = 5V, 0V, V_{CM} = 2.5V, V_O = 2.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
A _{VOL}	Large-Signal Voltage Gain	V _O = 50mV to 4.8V, R _L = 10k	●	250	2000	V/mV	
CMRR	Common Mode Rejection Ratio (LT1366/LT1368) CMRR Match (Channel to Channel)	V _{CM} = V _{EE} to V _{CC}	●	80	87	dB	
		V _{CM} = V _{EE} to V _{CC} (Note 3)	●	74	87	dB	
	Common Mode Rejection Ratio (LT1367/LT1369) CMRR Match (Channel to Channel)	V _{CM} = V _{EE} to V _{CC}	●	77	87	dB	
		V _{CM} = V _{EE} to V _{CC} (Note 3)	●	71	87	dB	
PSRR	Power Supply Rejection Ratio PSRR Match (Channel to Channel) (Note 3)	V _S = 2.3V to 12V, V _{CM} = V _O = 0.5V	●	88	105	dB	
		V _S = 2.3V to 12V, V _{CM} = V _O = 0.5V	●	82	100	dB	
V _{OL}	Output Voltage Swing LOW	No Load	●		9	14	mV
		I _{SINK} = 0.5mA	●		45	80	mV
		I _{SINK} = 2.5mA	●		120	230	mV
V _{OH}	Output Voltage Swing HIGH	No Load	●	V _{CC} - 0.014	V _{CC} - 0.005	V	
		I _{SOURCE} = 0.5mA	●	V _{CC} - 0.110	V _{CC} - 0.055	V	
		I _{SOURCE} = 2.5mA	●	V _{CC} - 0.300	V _{CC} - 0.180	V	
I _{SC}	Short-Circuit Current	(Note 1)	●	±12.5		mA	
I _S	Supply Current per Amplifier		●		385	540	μA

T_A = 25°C, V_S = 3V, 0V, V_{CM} = 1.5V, V_O = 1.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
V _{OS}	Input Offset Voltage (LT1366/LT1368)	V _{CM} = V _{CC}		150	475	μV	
		V _{CM} = V _{EE}		150	475	μV	
	Input Offset Voltage (LT1367/LT1369)	V _{CM} = V _{CC}		150	850	μV	
		V _{CM} = V _{EE}		150	750	μV	
ΔV _{OS}	Input Offset Voltage Shift (LT1366/LT1368) Input Offset Voltage Match (Channel to Channel)	V _{CM} = V _{EE} to V _{CC}		150	400	μV	
		V _{CM} = V _{EE} , V _{CC} (Notes 3, 4)		250	700	μV	
	Input Offset Voltage Shift (LT1367/LT1369) Input Offset Voltage Match (Channel to Channel)	V _{CM} = V _{EE} to V _{CC}		150	650	μV	
		V _{CM} = V _{EE} , V _{CC} (Notes 3, 4)		250	1700	μV	
I _B	Input Bias Current	V _{CM} = V _{CC}	0	10	35	nA	
		V _{CM} = V _{EE}	-35	-10	0	nA	
ΔI _B	Input Bias Current Shift	V _{CM} = V _{EE} to V _{CC}		20	70	nA	
I _{OS}	Input Offset Current	V _{CM} = V _{CC}		1.0	12	nA	
		V _{CM} = V _{EE}		0.3	12	nA	
ΔI _{OS}	Input Offset Current Shift Input Bias Current Match (Channel to Channel)	V _{CM} = V _{EE} to V _{CC}		1	12	nA	
		V _{CM} = V _{CC} (Note 3) V _{CM} = V _{EE} (Note 3)	0	1	12	nA	
			0	1	12	nA	
A _{VOL}	Large-Signal Voltage Gain	V _O = 50mV to 2.8V, R _L = 10k		250	1500	V/mV	
CMRR	Common Mode Rejection Ratio (LT1366/LT1368) CMRR Match (Channel to Channel)	V _{CM} = V _{EE} to V _{CC}		77	86	dB	
		V _{CM} = V _{EE} to V _{CC} (Note 3)		71	86	dB	
	Common Mode Rejection Ratio (LT1367/LT1369) CMRR Match (Channel to Channel)	V _{CM} = V _{EE} to V _{CC}		73	86	dB	
		V _{CM} = V _{EE} to V _{CC} (Note 3)		67	86	dB	
V _{OL}	Output Voltage Swing LOW	No Load		6	12	mV	
		I _{SINK} = 0.5mA		40	70	mV	
		I _{SINK} = 2.5mA		110	200	mV	
V _{OH}	Output Voltage Swing HIGH	No Load		V _{CC} - 0.012	V _{CC} - 0.004	V	
		I _{SOURCE} = 0.5mA		V _{CC} - 0.100	V _{CC} - 0.050	V	
		I _{SOURCE} = 2.5mA		V _{CC} - 0.250	V _{CC} - 0.150	V	
I _{SC}	Short-Circuit Current	(Note 1)		±10	±20	mA	
I _S	Supply Current per Amplifier				330	500	μA

ELECTRICAL CHARACTERISTICS

0°C < T_A < 70°C, V_S = 3V, 0V, V_{CM} = 1.5V, V_O = 1.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{OS}	Input Offset Voltage (LT1366/LT1368)	V _{CM} = V _{CC}	●	200	575	μV
		V _{CM} = V _{EE}	●	200	575	μV
	Input Offset Voltage (LT1367/LT1369)	V _{CM} = V _{CC}	●	200	950	μV
		V _{CM} = V _{EE}	●	200	900	μV
ΔV _{OS}	Input Offset Voltage Shift (LT1366/LT1368) Input Offset Voltage Match (Channel to Channel)	V _{CM} = V _{EE} to V _{CC}	●	200	425	μV
		V _{CM} = V _{EE} , V _{CC} (Notes 3, 4)	●	250	900	μV
	Input Offset Voltage Shift (LT1367/LT1369) Input Offset Voltage Match (Channel to Channel)	V _{CM} = V _{EE} to V _{CC}	●	200	675	μV
		V _{CM} = V _{EE} , V _{CC} (Notes 3, 4)	●	250	1900	μV
V _{OS} TC	Input Offset Voltage Drift	(Note 2)	●	2	6	μV/°C
I _B	Input Bias Current	V _{CM} = V _{CC}	●	0	15	nA
		V _{CM} = V _{EE}	●	-45	-10	0
ΔI _B	Input Bias Current Shift	V _{CM} = V _{EE} to V _{CC}	●	25	90	nA
I _{OS}	Input Offset Current	V _{CM} = V _{CC}	●	2	15	nA
		V _{CM} = V _{EE}	●	1	15	nA
ΔI _{OS}	Input Offset Current Shift Input Bias Current Match (Channel to Channel)	V _{CM} = V _{EE} to V _{CC}	●	2	15	nA
		V _{CM} = V _{CC} (Note 3) V _{CM} = V _{EE} (Note 3)	● ●	0 0	2 1	15 15
A _{VOL}	Large-Signal Voltage Gain	V _O = 50mV to 2.8V, R _L = 10k	●	150	1500	V/mV
CMRR	Common Mode Rejection Ratio (LT1366/LT1368) CMRR Match (Channel to Channel)	V _{CM} = V _{EE} to V _{CC}	●	76	83	dB
		V _{CM} = V _{EE} to V _{CC} (Note 3)	●	70	83	dB
	Common Mode Rejection Ratio (LT1367 /LT1369) CMRR Match (Channel to Channel)	V _{CM} = V _{EE} to V _{CC} V _{CM} = V _{EE} to V _{CC} (Note 3)	● ●	72 66	83 83	dB dB
V _{OL}	Output Voltage Swing LOW	No Load	●	9	14	mV
		I _{SINK} = 0.5mA	●	45	80	mV
		I _{SINK} = 2.5mA	●	120	230	mV
V _{OH}	Output Voltage Swing HIGH	No Load	●	V _{CC} - 0.014	V _{CC} - 0.005	V
		I _{SOURCE} = 0.5mA	●	V _{CC} - 0.110	V _{CC} - 0.055	V
		I _{SOURCE} = 2.5mA	●	V _{CC} - 0.300	V _{CC} - 0.180	V
I _{SC}	Short-Circuit Current	(Note 1)	●	±10		mA
I _S	Supply Current per Amplifier		●	375	520	μA

ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, $V_O = 0\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (LT1366/LT1368)	$V_{CM} = V_{CC}$ $V_{CM} = V_{EE}$		200 200	700 700	μV μV
	Input Offset Voltage (LT1367/LT1369)	$V_{CM} = V_{CC}$ $V_{CM} = V_{EE}$		200 200	1000 900	μV μV
ΔV_{OS}	Input Offset Voltage Shift (LT1366/LT1368)	$V_{CM} = V_{EE}$ to V_{CC}		150	500	μV
	Input Offset Voltage Match (Channel to Channel)	$V_{CM} = V_{EE}$, V_{CC} (Notes 3, 4)		300	1300	μV
	Input Offset Voltage Shift (LT1367/LT1369)	$V_{CM} = V_{EE}$ to V_{CC}		150	650	μV
	Input Offset Voltage Match (Channel to Channel)	$V_{CM} = V_{EE}$, V_{CC} (Notes 3, 4)		300	2000	μV
I_B	Input Bias Current	$V_{CM} = V_{CC}$	0	10	35	nA
		$V_{CM} = V_{EE}$	-35	-10	0	nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V_{EE}$ to V_{CC}		20	70	nA
I_{OS}	Input Offset Current	$V_{CM} = V_{CC}$		1.0	12	nA
		$V_{CM} = V_{EE}$		0.3	12	nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V_{EE}$ to V_{CC}		1	12	nA
	Input Bias Current Match (Channel to Channel)	$V_{CM} = V_{CC}$ (Note 3) $V_{CM} = V_{EE}$ (Note 3)	0 0	1 1	12 12	nA nA
C_{IN}	Input Capacitance			7.1		pF
A_{VOL}	Large-Signal Voltage Gain	$V_O = -14.7\text{V}$ to 14.7V , $R_L = 10\text{k}$ $V_O = -10\text{V}$ to 10V , $R_L = 2\text{k}$	1000 500	10000 10000		V/mV V/mV
	Channel Separation	$V_O = -10\text{V}$ to 10V , $R_L = 2\text{k}$	120	135		dB
SR	Slew Rate (LT1366/LT1367)	$A_V = -1$, $R_L = \text{Open}$, $V_O = \pm 10\text{V}$, Measured at $V_O = \pm 5\text{V}$		0.13		V/ μs
	Slew Rate (LT1368/LT1369)	$A_V = -1$, $R_L = \text{Open}$, $V_O = \pm 10\text{V}$, Measured at $V_O = \pm 5\text{V}$		0.065		V/ μs
CMRR	Common Mode Rejection Ratio (LT1366/LT1368)	$V_{CM} = V_{EE}$ to V_{CC}	95	106		dB
	CMRR Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC} (Note 3)	89	106		dB
	Common Mode Rejection Ratio (LT1367/LT1369)	$V_{CM} = V_{EE}$ to V_{CC}	93	106		dB
	CMRR Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC} (Note 3)	87	106		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 5\text{V}$ to $\pm 15\text{V}$	90	110		dB
	PSRR Match (Channel to Channel)	$V_S = \pm 5\text{V}$ to $\pm 15\text{V}$ (Note 3)	84	105		dB
V_{OL}	Output Voltage Swing LOW	No Load		$V_{EE} + 0.006$	$V_{EE} + 0.012$	V
		$I_{SINK} = 0.5\text{mA}$		$V_{EE} + 0.040$	$V_{EE} + 0.070$	V
		$I_{SINK} = 10\text{mA}$		$V_{EE} + 0.240$	$V_{EE} + 0.500$	V
V_{OH}	Output Voltage Swing HIGH	No Load	$V_{CC} - 0.012$	$V_{CC} - 0.004$		V
		$I_{SOURCE} = 0.5\text{mA}$	$V_{CC} - 0.100$	$V_{CC} - 0.050$		V
		$I_{SOURCE} = 10\text{mA}$	$V_{CC} - 0.800$	$V_{CC} - 0.400$		V
I_{SC}	Short-Circuit Current	(Note 1)	± 30	± 75		mA
I_S	Supply Current per Amplifier			370	550	μA

ELECTRICAL CHARACTERISTICS

$0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, $V_O = 0\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (LT1366/LT1368)	$V_{CM} = V_{CC}$	●	250	850	μV
		$V_{CM} = V_{EE}$	●	250	850	μV
	Input Offset Voltage (LT1367/LT1369)	$V_{CM} = V_{CC}$	●	250	1150	μV
		$V_{CM} = V_{EE}$	●	250	1000	μV
ΔV_{OS}	Input Offset Voltage Shift (LT1366/LT1368) Input Offset Voltage Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC}	●	200	525	μV
		$V_{CM} = V_{EE}$, V_{CC} (Notes 3, 4)	●	300	1500	μV
	Input Offset Voltage Shift (LT1367/LT1369) Input Offset Voltage Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC}	●	200	750	μV
		$V_{CM} = V_{EE}$, V_{CC} (Notes 3, 4)	●	300	2300	μV
$V_{OS\ TC}$	Input Offset Voltage Drift	(Note 2)	●	2	8	$\mu\text{V}/^{\circ}\text{C}$
I_B	Input Bias Current	$V_{CM} = V_{CC}$	●	0	15	nA
		$V_{CM} = V_{EE}$	●	-45	-10	0
ΔI_B	Input Bias Current Shift	$V_{CM} = V_{EE}$ to V_{CC}	●	25	90	nA
I_{OS}	Input Offset Current	$V_{CM} = V_{CC}$	●	2	15	nA
		$V_{CM} = V_{EE}$	●	1	15	nA
ΔI_{OS}	Input Offset Current Shift Input Bias Current Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC}	●	2	15	nA
		$V_{CM} = V_{CC}$ (Note 3) $V_{CM} = V_{EE}$ (Note 3)	● ●	0 0	2 1	15 15
A_{VOL}	Large-Signal Voltage Gain Channel Separation	$V_O = -14.7\text{V}$ to 14.7V , $R_L = 10\text{k}$	●	750	6000	V/mV
		$V_O = -10\text{V}$ to 10V , $R_L = 2\text{k}$	●	500	6000	V/mV
CMRR	Common Mode Rejection Ratio (LT1366/LT1368) CMRR Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC}	●	95	103	dB
		$V_{CM} = V_{EE}$ to V_{CC} (Note 3)	●	89	103	dB
	Common Mode Rejection Ratio (LT1367/LT1369) CMRR Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC}	●	92	103	dB
		$V_{CM} = V_{EE}$ to V_{CC} (Note 3)	●	86	103	dB
PSRR	Power Supply Rejection Ratio PSRR Match (Channel to Channel)	$V_S = \pm 5\text{V}$ to $\pm 15\text{V}$	●	80	105	dB
		$V_S = \pm 5\text{V}$ to $\pm 15\text{V}$ (Note 3)	●	75	100	dB
V_{OL}	Output Voltage Swing LOW	No Load	●	$V_{EE} + 0.009$	$V_{EE} + 0.014$	V
		$I_{SINK} = 0.5\text{mA}$	●	$V_{EE} + 0.045$	$V_{EE} + 0.080$	V
		$I_{SINK} = 10\text{mA}$	●	$V_{EE} + 0.300$	$V_{EE} + 0.600$	V
V_{OH}	Output Voltage Swing HIGH	No Load	●	$V_{CC} - 0.014$	$V_{CC} - 0.005$	V
		$I_{SOURCE} = 0.5\text{mA}$	●	$V_{CC} - 0.11$	$V_{CC} - 0.055$	V
		$I_{SOURCE} = 10\text{mA}$	●	$V_{CC} - 0.95$	$V_{CC} - 0.500$	V
I_{SC}	Short-Circuit Current	(Note 1)	●	± 30		mA
I_S	Supply Current per Amplifier		●	415	575	μA

The ● denotes specifications that apply over the full operating temperature range.

Note 1: Applies to short circuits to ground for all split supplies and for single supplies less than 20V. Short circuits to either supply for supplies greater than 20V total may permanently damage the part. A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 2: This parameter is not 100% tested.

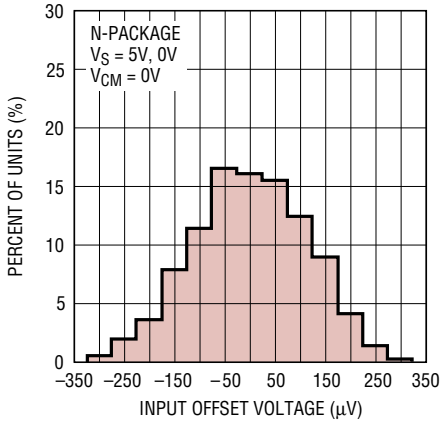
Note 3: Matching parameters are the difference between amplifiers A and D and between B and C on the LT1367/LT1369; between the two amplifiers on the LT1366/LT1368.

Note 4: Input offset voltage match is the difference in offset voltage between amplifiers measured at both $V_{CM} = V_{EE}$ and $V_{CM} = V_{CC}$.

TYPICAL PERFORMANCE CHARACTERISTICS

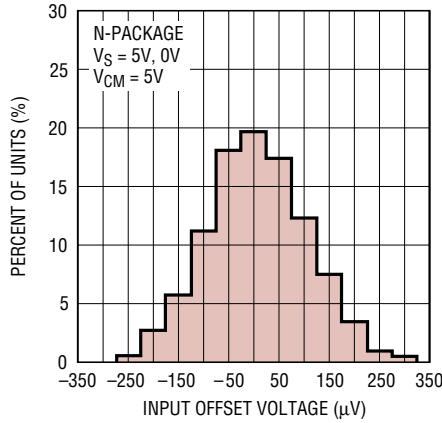
(The data presented here applies to the LT1366/LT1367/LT1368/LT1369 unless otherwise noted.)

PNP Stage V_{OS} Distribution (LT1366/LT1368)



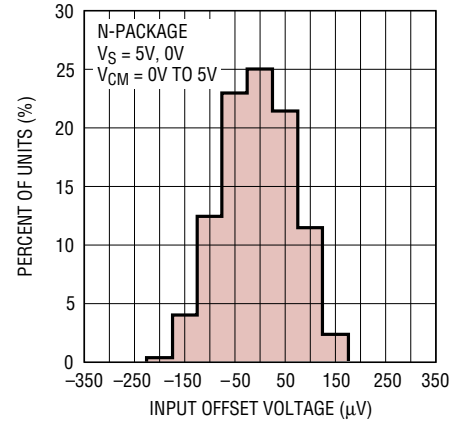
LT1366 TPC03

NPN Stage V_{OS} Distribution (LT1366/LT1368)



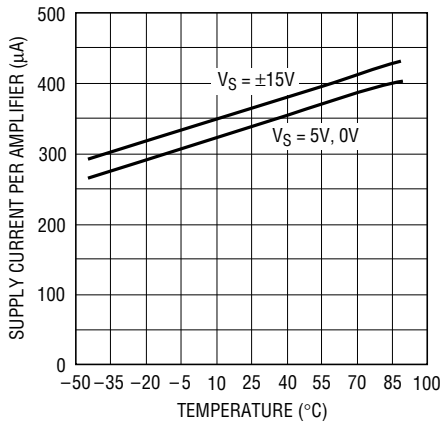
LT1366 TPC02

ΔV_{OS} -Shift Between PNP and NPN Stages (LT1366/LT1368)



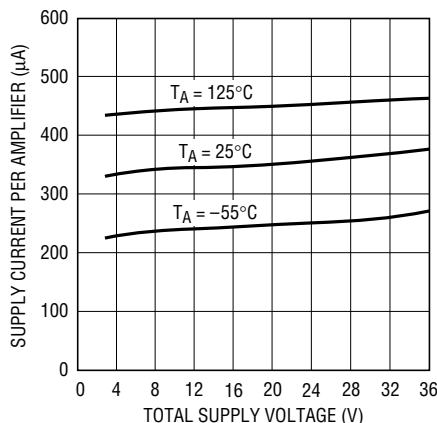
LT1366 TPC01

Supply Current vs Temperature



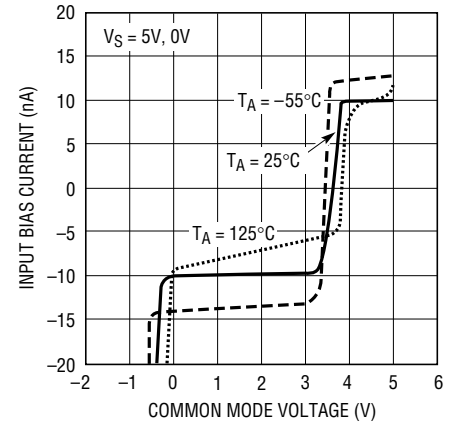
LT1366 TPC04

Supply Current vs Supply Voltage



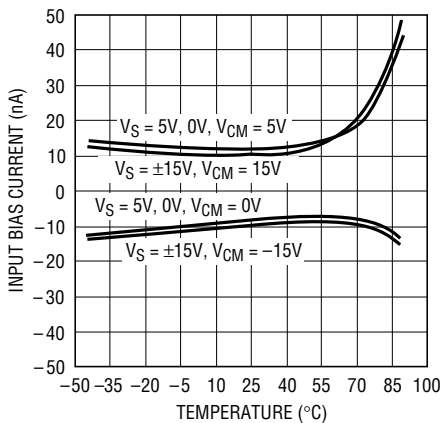
LT1366 TPC05

Input Bias Current vs Common Mode Voltage



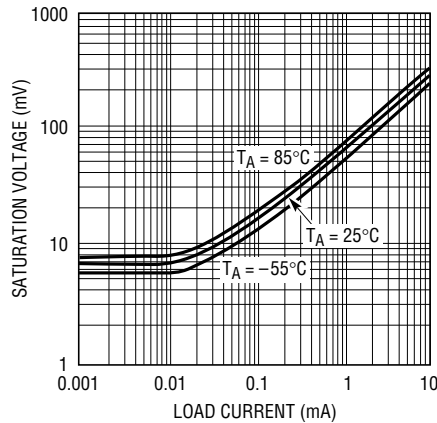
LT1366 TPC06

Input Bias Current vs Temperature



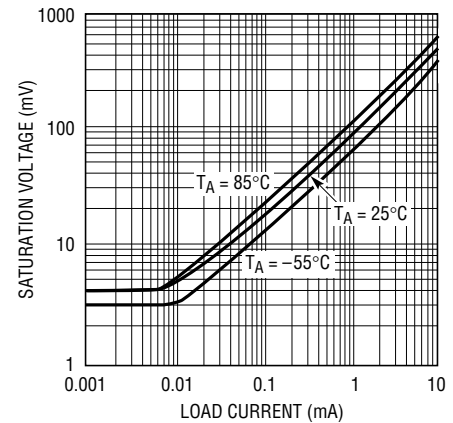
LT1366 TPC07

Output Saturation Voltage vs Load Current (Output HIGH)



LT1366 TPC08

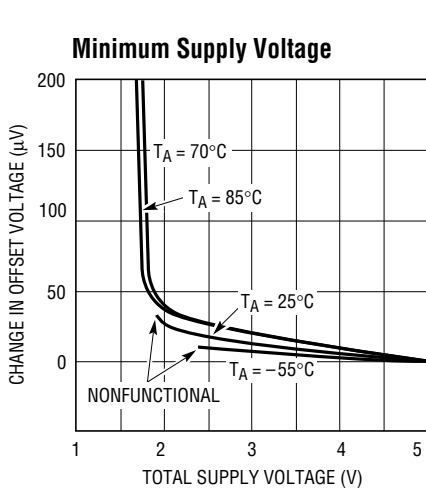
Output Saturation Voltage vs Load Current (Output LOW)



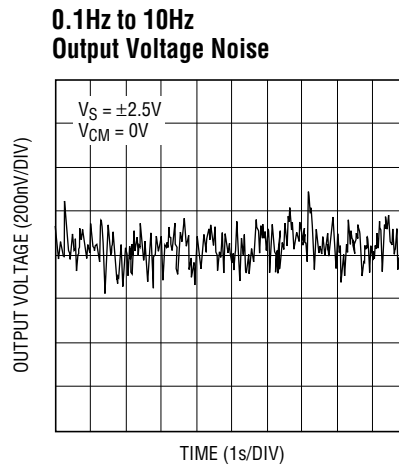
LT1366 TPC09

TYPICAL PERFORMANCE CHARACTERISTICS

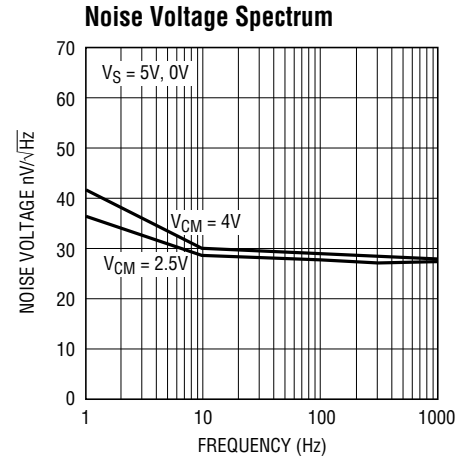
(The data presented here applies to the LT1366/LT1367/LT1368/LT1369 unless otherwise noted.)



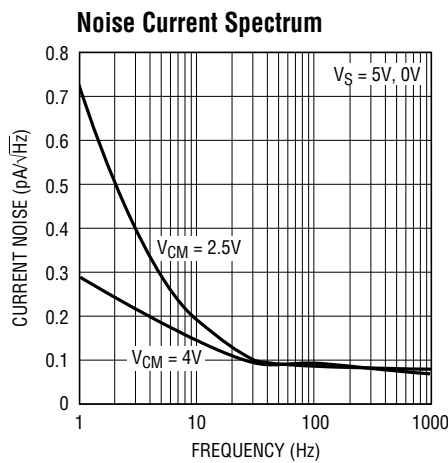
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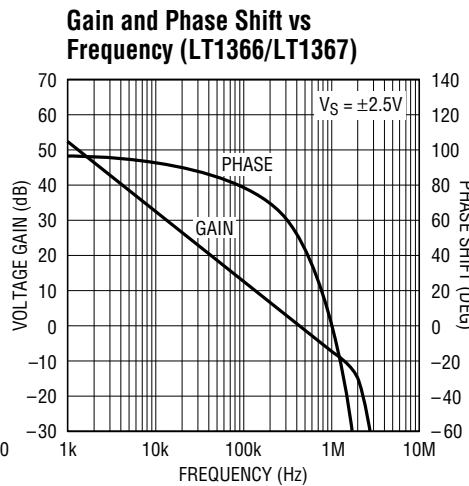
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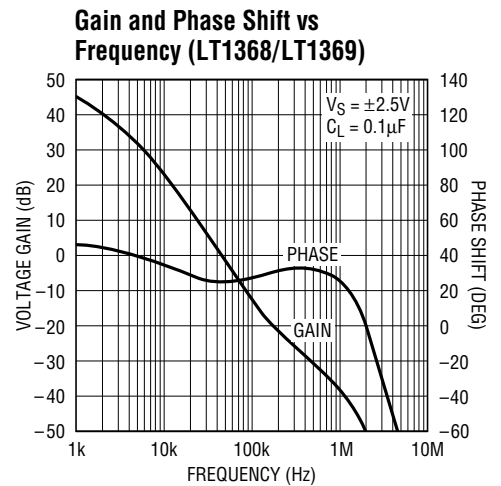
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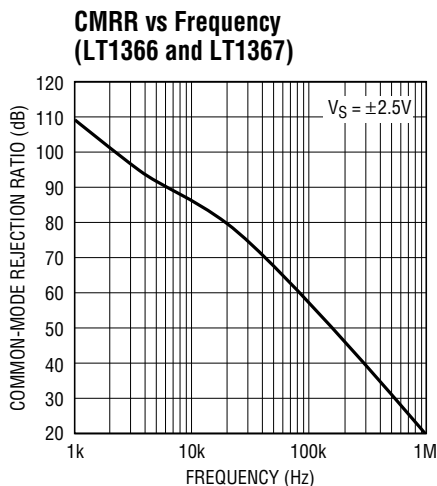
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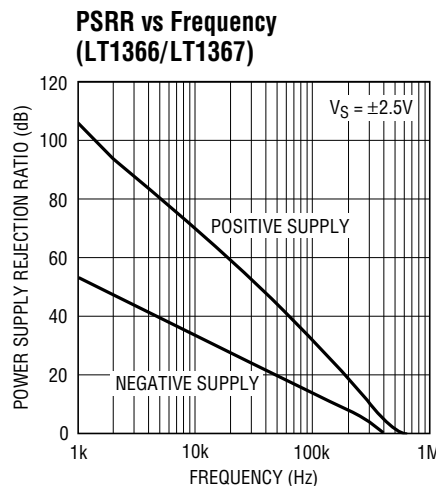
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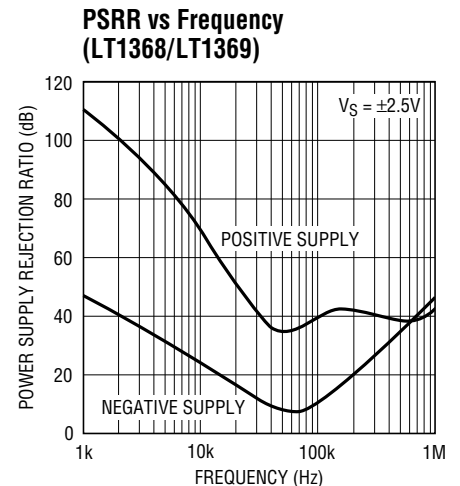
LT1366 TPC15



LT1366 TPC16



LT1366 TPC17

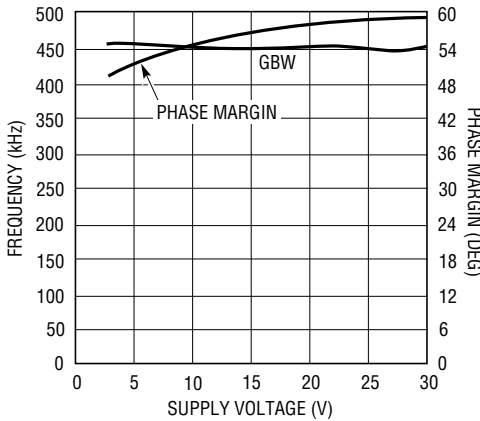


LT1366 TPC18

TYPICAL PERFORMANCE CHARACTERISTICS

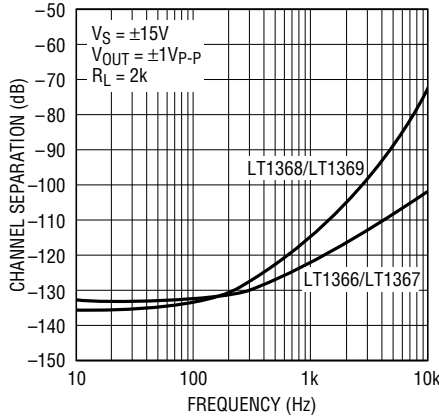
(The data presented here applies to the LT1366/LT1367/LT1368/LT1369 unless otherwise noted.)

Gain-Bandwidth and Phase Margin vs Supply Voltage (LT1366/LT1367)



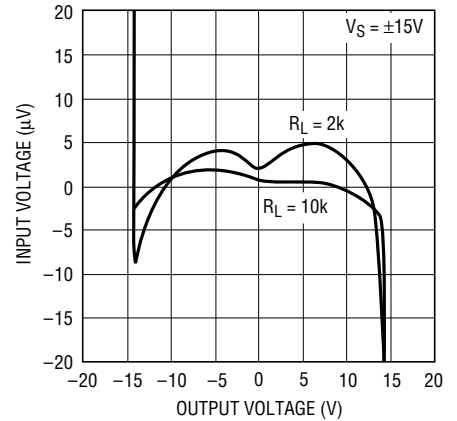
LT1366 TPC19

Channel Separation vs Frequency



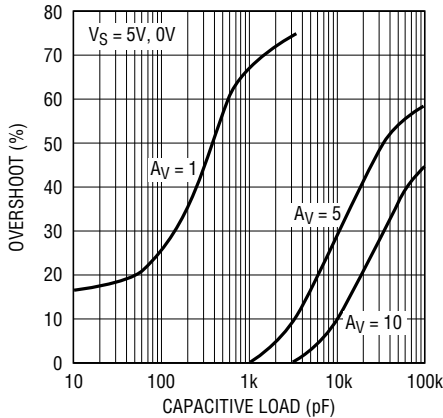
LT1366 TPC20

Open-Loop Gain



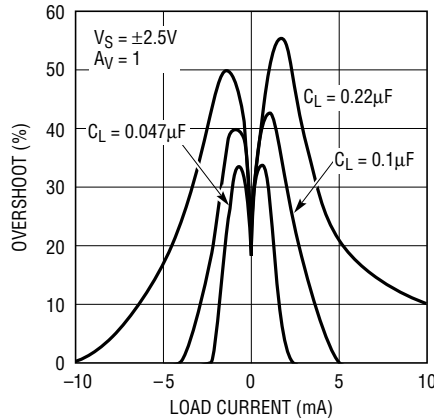
LT1366 TPC21

Capacitive Load Handling (LT1366/LT1367)



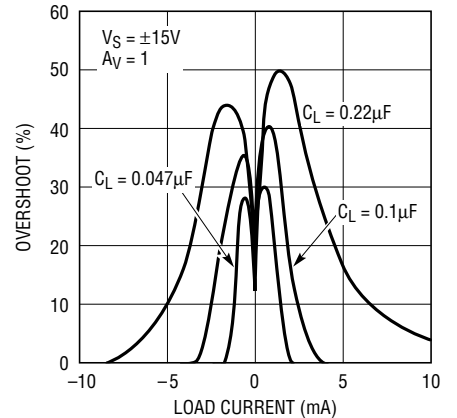
LT1366 TPC22

Overshoot vs Load Current (LT1368/LT1369)



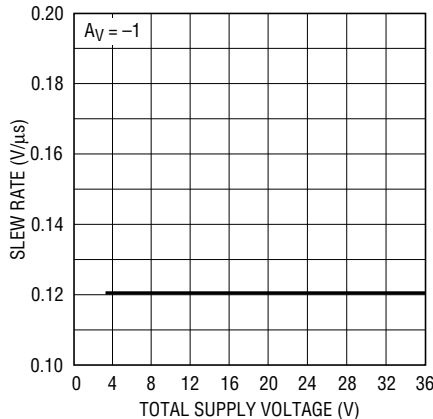
LT1366 TPC23

Overshoot vs Load Current (LT1368/LT1369)



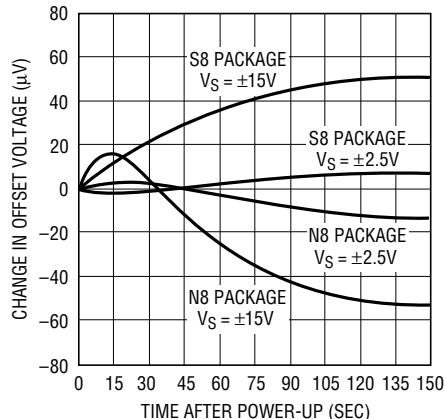
LT1366 TPC24

Slew Rate vs Supply Voltage



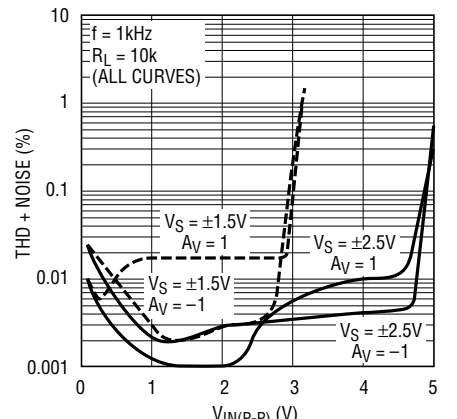
LT1366 TPC25

Warm-Up Drift vs Time



LT1366 TPC26

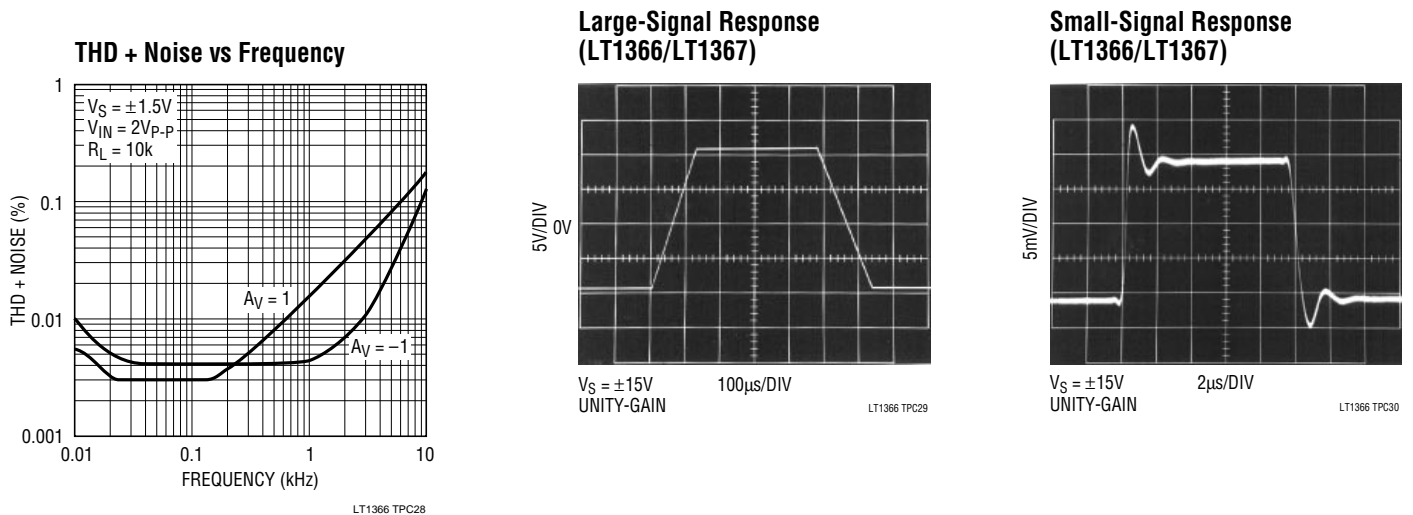
THD + Noise vs Peak-to-Peak Voltage



LT1366 TPC27

TYPICAL PERFORMANCE CHARACTERISTICS

(The data presented here applies to the LT1366/LT1367/LT1368/LT1369 unless otherwise noted.)



APPLICATIONS INFORMATION

Rail-to-Rail Operation

The LT1366 family differs from conventional op amps in the design of both the input and output stages. Figure 1 shows a simplified schematic of the amplifier. The input stage consists of two differential amplifiers, a PNP stage Q1/Q2 and an NPN stage Q3/Q4, which are active over

different portions of the input common mode range. Lateral devices are used in both input stages, eliminating the need for clamps across the input pins. Each input stage is trimmed for offset voltage. A complementary output configuration (Q23 through Q26) is employed to create an output stage with rail-to-rail swing. The amplifier is fabri-

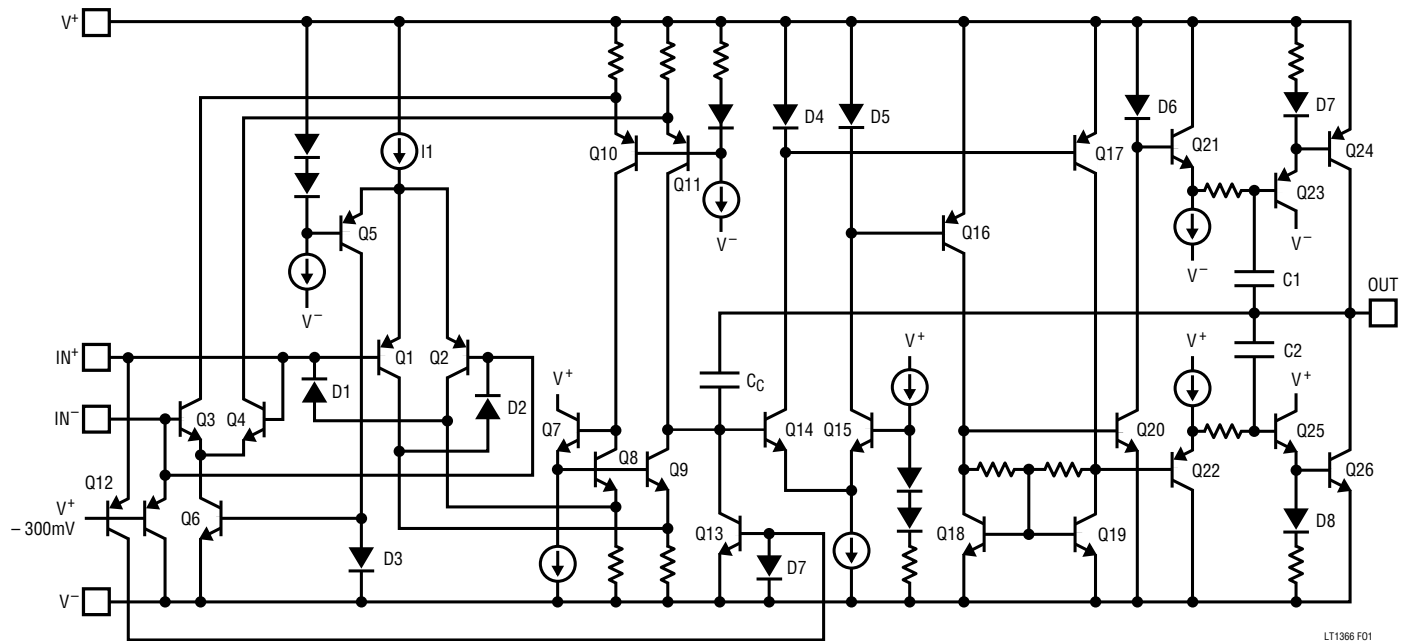


Figure 1. LT1366 Simplified Schematic Diagram

APPLICATIONS INFORMATION

cated on Linear Technology's proprietary complementary bipolar process, which ensures very similar DC and AC characteristics for the output devices Q24 and Q26.

A simple comparator Q5 steers current from current source I1 between the two input stages. When the input common mode voltage V_{CM} is near the negative supply, Q5 is reverse biased, and I1 becomes the tail current for the PNP differential pair Q1/Q2. At the other extreme, when V_{CM} is within about 1.3V from the positive supply, Q5 diverts I1 to the current mirror D3/Q6, which furnishes the tail current for the NPN differential pair Q3/Q4.

The collector currents of the two input pairs are combined in the second stage, consisting of Q7 through Q11. Most of the voltage gain in the amplifier is contained in this stage. Differential amplifier Q14/Q15 buffers the output of the second stage, converting the output voltage to differential currents. The differential currents pass through current mirrors D4/Q17 and D5/Q16, and are converted to differential voltages by Q18 and Q19. These voltages are also buffered and applied to the output Darlington pairs Q23/Q24 and Q25/Q26. Capacitors C1 and C2 form local feedback loops around the output devices, lowering the output impedance at high frequencies.

Input Offset Voltage

Since the amplifier has two input stages, the input offset voltage changes depending upon which stage is active. The input offsets are random, but bounded voltages. When the amplifier switches between stages, offset voltages may go up, down, or remain flat; but will not exceed the guaranteed limits. This behavior is illustrated in three distribution plots of input offset voltage in the Typical Performance Characteristics section.

Overdrive Protection

Two circuits prevent the output from reversing polarity when the input voltage exceeds the common mode range. When the noninverting input exceeds the positive supply by approximately 300mV, the clamp transistor Q12 (Figure 1) turns on, pulling the output of the second stage low, which forces the output high. For inputs below the negative supply, diodes D1 and D2 turn on, overcoming the saturation of the input pair Q1/Q2.

When overdriven, the amplifier draws input current that exceeds the normal input bias current. Figures 2 and 3 show some typical overdrive currents as a function of input voltage. The input current must be less than 1mA of positive overdrive or less than 7mA of negative overdrive, for the phase reversal protection to work properly. When the amplifier is severely overdriven, an external resistor should be used to limit the overdrive current. In addition to overdrive protection, the amplifier is protected against ESD strokes up to 4kV on all pins.

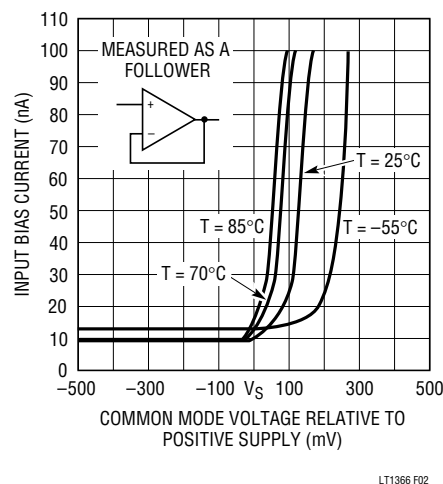


Figure 2. Input Bias Current vs Common Mode Voltage

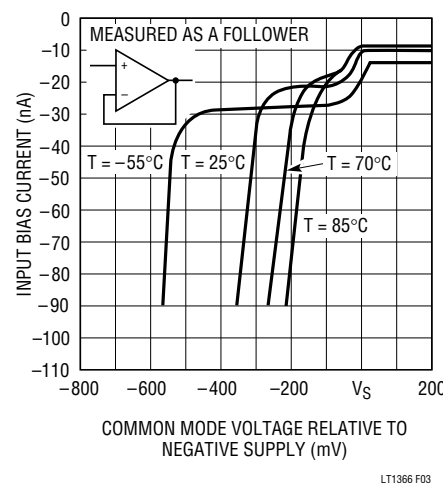


Figure 3. Input Bias Current vs Common Mode Voltage

APPLICATIONS INFORMATION

Improved Supply Rejection in the LT1368/LT1369

The LT1368/LT1369 are variations of the LT1366/LT1367 offering greater supply rejection and lower high frequency output impedance. The LT1368/LT1369 require a $0.1\mu\text{F}$ load capacitance for compensation. The output capacitance forms a filter, which reduces pickup from the supply and lowers the output impedance. This additional filtering is helpful in mixed analog/digital systems with common supplies, or systems employing switching supplies. Filtering also reduces high frequency noise, which may be beneficial when driving A/D converters.

Figure 4 shows the outputs of the LT1366/LT1368 perturbed by a $200\text{mV}_{\text{P-P}}$ 50kHz square wave added to the positive supply. The LT1368's power supply rejection is about ten times greater than that of the LT1366 at 50kHz . Note the 5-to-1 scale change in the output voltage traces.

The tolerance of the external compensation capacitor is not critical. The plots of Overshoot vs Load Current in the Typical Performance Characteristics section illustrate the effect of a capacitive load.

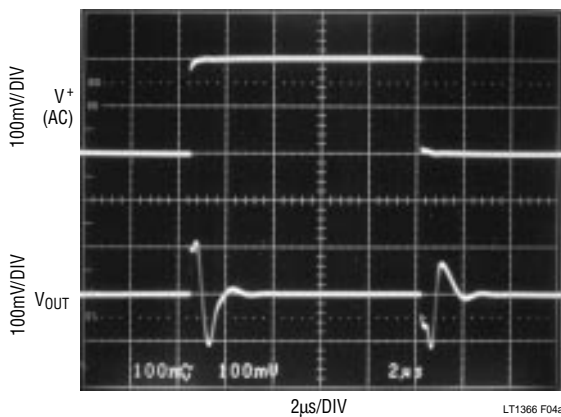


Figure 4a. LT1366 Power Supply Rejection Test

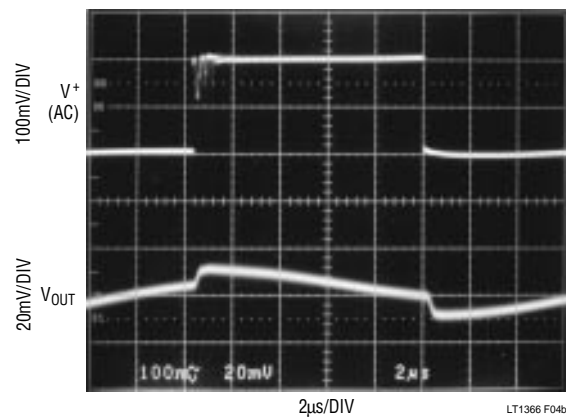


Figure 4b. LT1368 Power Supply Rejection Test

TYPICAL APPLICATIONS

Buffering A/D Converters

Figure 5 shows the LT1368 driving an LTC[®]1288 2-channel micropower A/D Converter (ADC). The LTC1288 can accommodate voltage references and input signals equal to the supply rails. The sampling nature of this ADC eliminates the need for an external sample-and-hold, but may call for a drive amplifier because of the ADC's $12\mu\text{s}$ settling requirement. The LT1368's rail-to-rail operation and low input offset voltage make it well-suited for low power, low frequency A/D applications. Either the LT1366 or LT1368 could be used for this application. However, for low frequencies ($f < 1\text{kHz}$) the LT1368 provides better supply rejection.

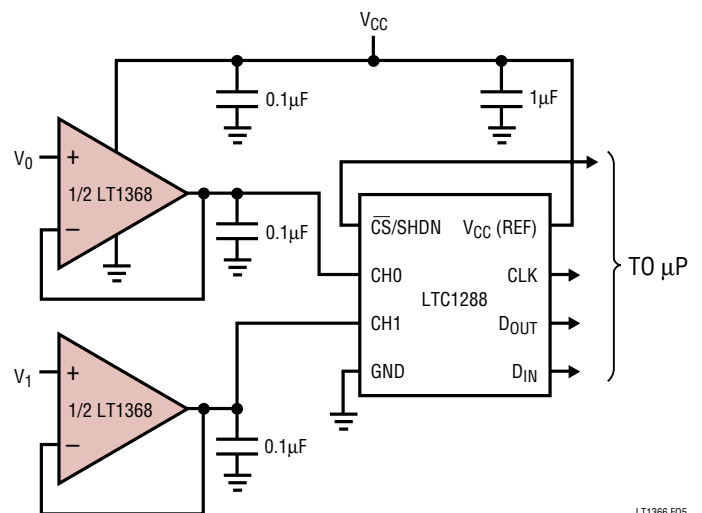


Figure 5. 2-Channel Low Power A/D Converter

TYPICAL APPLICATIONS

Precision Low Dropout Regulator

Microprocessors and complex digital circuits frequently specify tight control of power supply characteristics. The circuit shown in Figure 6 provides a precise 3.6V, 1A output from a minimum 3.8V input voltage. The circuit's nominal operating voltage is $4.75V \pm 5\%$. The voltage reference and resistor ratios determine output voltage accuracy, while the LT1366's high gain enforces 0.2% line and load regulation. Quiescent current is about 1mA and does not change appreciably with supply or load. All components are available in surface mount packages.

The regulator's main loop consists of A1 and a logic level FET, Q1. The output is fed back to the op amp's positive input because of the phase inversion through Q1. The regulator's frequency response is limited by Q1's roll-off and the phase lead introduced by the output capacitor's effective series resistance (ESR). Two pole-zero networks compensate for these effects. The pole formed with R5 and C2 rolls off the gain set with the feedback network, while the pole formed with R7 and C3 rolls off A1's gain directly, which is the dominant influence on settling time. The zeros formed with R6 and C2, and R8 and C3 provide phase boost near the unity-gain crossover, which in-

creases the regulator's phase margin. Although not directly part of the compensation, R9 decouples the op amp's output from Q1's large gate capacitance.

A second loop provides a foldback current limit. A2 compares the sense voltage across R1 with 50mV referenced to the positive rail. When the sense voltage exceeds the reference, A2's output drives Q1's gate positive via A1. In current limit, the output voltage collapses and the current limit LED (D1) turns on causing about 30mV to drop across R3. A2 regulates Q1's drain current so that the deficit between the 50mV reference and the voltage across R3 is made up across the sense resistor. The reduced sense voltage is 20mV, which sets the current limit to about 400mA. As the supply voltage increases, the voltage across R3 increases, and the current limit folds back to a lower level. The current limit loop deactivates when the load current drops below the regulated output current. When the supply turns on rapidly, C1 bypasses the fold back circuit allowing the regulator to start-up into a heavy load.

Q1 does not require a heat sink. When mounted on a type FR4 PC board, Q1 has a thermal resistance of $50^{\circ}\text{C}/\text{W}$. At 1.4W worst case dissipation, Q1 can operate up to 80°C .

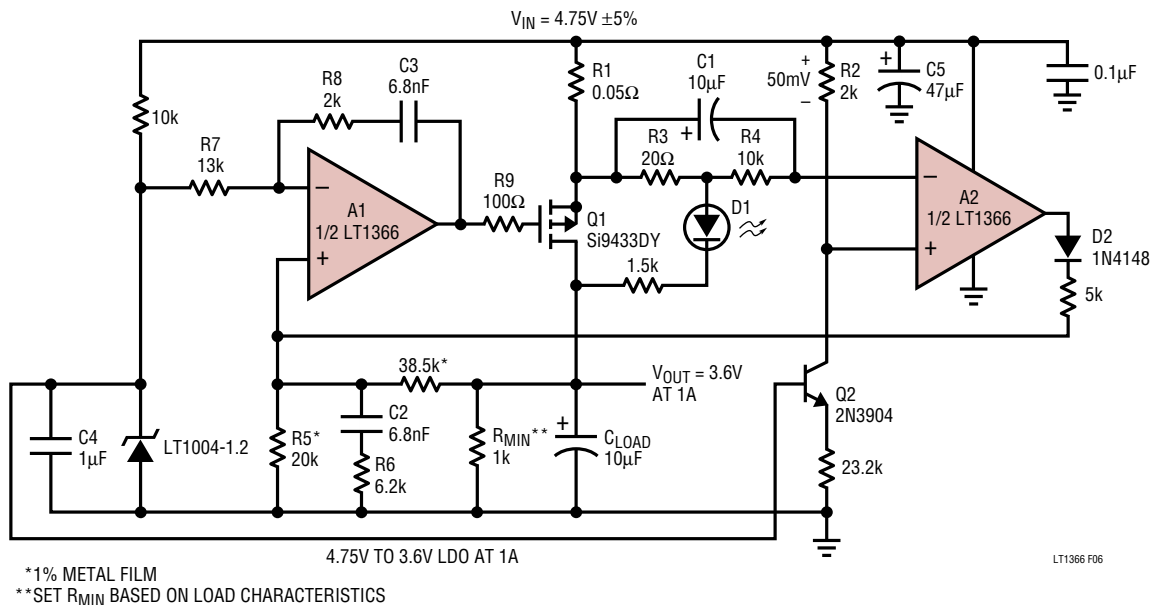


Figure 6. Precision 3.6V, 1A Low Dropout Regulator

TYPICAL APPLICATIONS

High-Side Current Source

The wide-compliance current source shown in Figure 7 takes advantage of the LT1366's ability to measure small signals near the positive supply rail. The LT1366 adjusts Q1's gate voltage to force the voltage across the sense resistor (R_{SENSE}) to equal the voltage from the supply to the potentiometer's wiper. A rail-to-rail op amp is needed because the voltage across the sense resistor must drop to zero when the divided reference voltage is set to zero. Q2 acts as a constant current sink to minimize error in the reference voltage when the supply voltage varies.

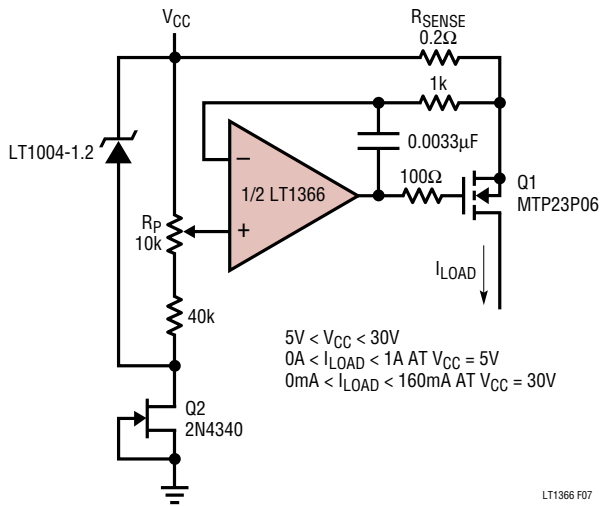


Figure 7. High-Side Current Source

The circuit can operate over a wide supply range ($5V < V_{CC} < 30V$). At low input voltage, circuit operation is limited by the MOSFET's gate drive requirements. At high

input voltage, circuit operation is limited by the LT1366's absolute maximum ratings and the output power requirements.

The circuit delivers 1A at 200mV of sense voltage. With a 5V input supply, the power dissipation is 5W. For operation at 70°C ambient temperature, the MOSFET's heat sink must have a thermal resistance of:

$$\begin{aligned} \theta_{HS} &= \theta_{JA \text{ SYSTEM}} - \theta_{JC \text{ FET}} \\ &= (125^{\circ}\text{C} - 70^{\circ}\text{C})/5\text{W} - 1.25^{\circ}\text{C/W} \\ &= 11^{\circ}\text{C/W} - 1.25^{\circ}\text{C/W} \\ &= 9.75^{\circ}\text{C/W} \end{aligned}$$

which is easily achievable with a small heat sink. Input voltages greater than 5V require the use of a larger heat sink or a reduction of the output current.

The circuit's supply regulation is about 0.03%/V. The output impedance is equal to the MOSFET's output impedance multiplied by the op amp's open-loop gain. Degrada-tions in current-source compliance occur when the voltage across the MOSFET's on-resistance and the sense resistor drops below the voltage required to maintain the desired output current. This condition occurs when $[V_{CC} - V_{OUT}] < [I_{LOAD} \cdot (R_{SENSE} + R_{ON})]$.

Single Supply, 1kHz, 4th Order Butterworth Filter

An LT1367 is used in Figure 8 to form a 4th order Butterworth filter. The filter is a simplified state variable architecture consisting of two cascaded 2nd order sections. Each section uses the 360 degree phase shift around

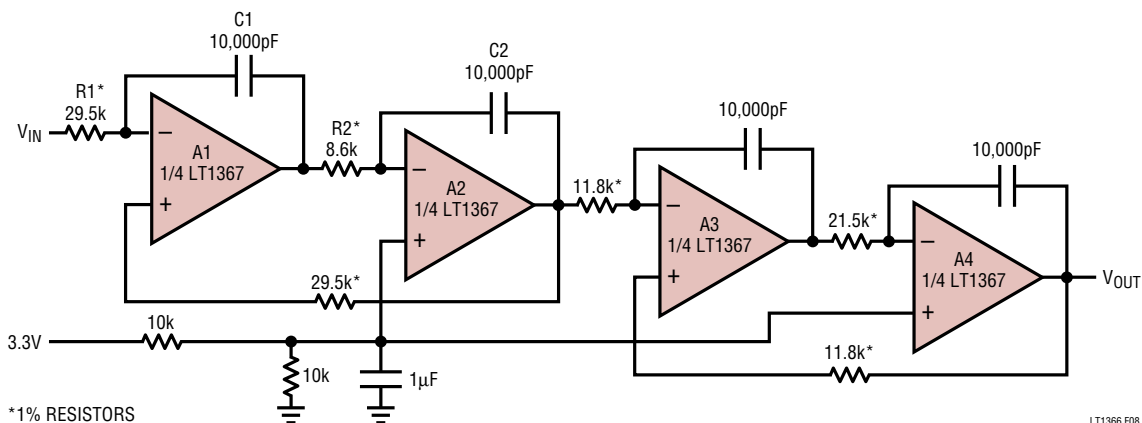


Figure 8. 4-Pole 1kHz, 3.3V Single Supply, State Variable Filter Using the LT1367

TYPICAL APPLICATIONS

the 2 op amp loop to create a negative summing junction at A1's positive input¹. The circuit has low sensitivities for center frequency and Q, which are set with the following equations:

$$\omega_0^2 = 1/(R1 \cdot C1 \cdot R2 \cdot C2)$$

where,

$$R1 = 1/(\omega_0 \cdot Q \cdot C1) \text{ and } R2 = Q/(\omega_0 \cdot C2).$$

The DC bias applied to A2 and A4, half supply, is not needed when split supplies are available. The circuit swings rail-to-rail in the passband making it an excellent anti-aliasing filter for ADCs. The amplitude response is flat to 1kHz then rolls off at 80dB/decade.

¹James Hahn, "State Variable Filter Trims Predecessor's Component Count," *Electronics*, April 21, 1982.

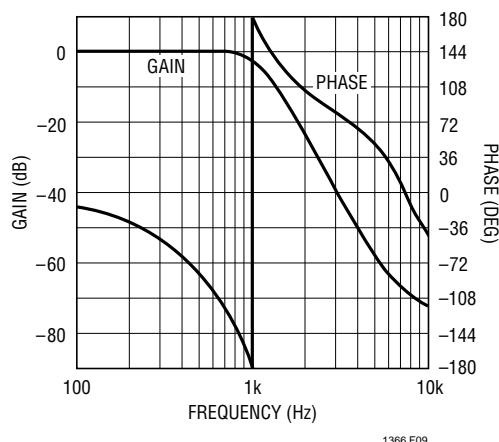


Figure 9. Frequency Response of 4th Order Butterworth Filter

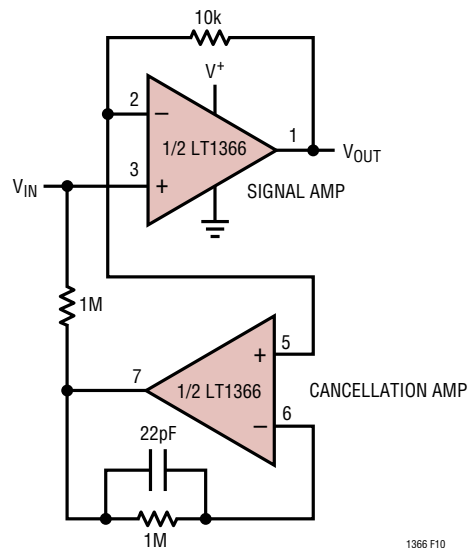


Figure 10. Input Bias Current Cancellation

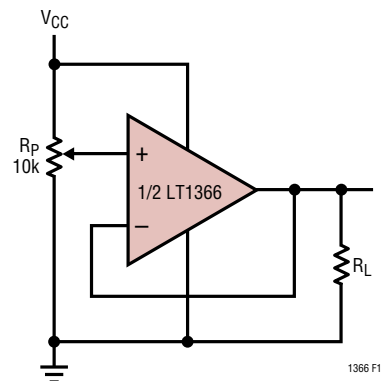
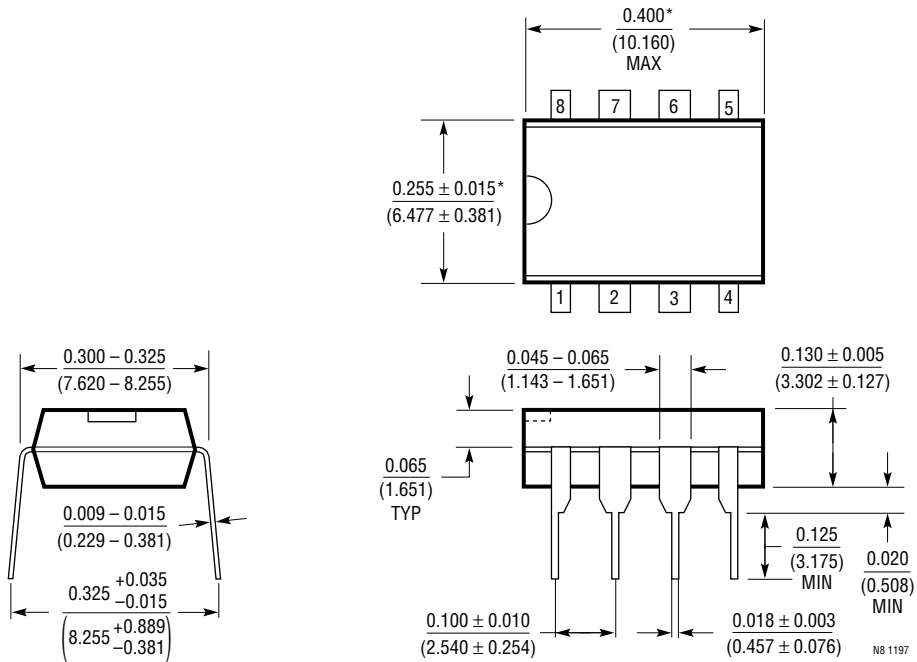


Figure 11. Rail-to-Rail Potentiometer Buffer

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

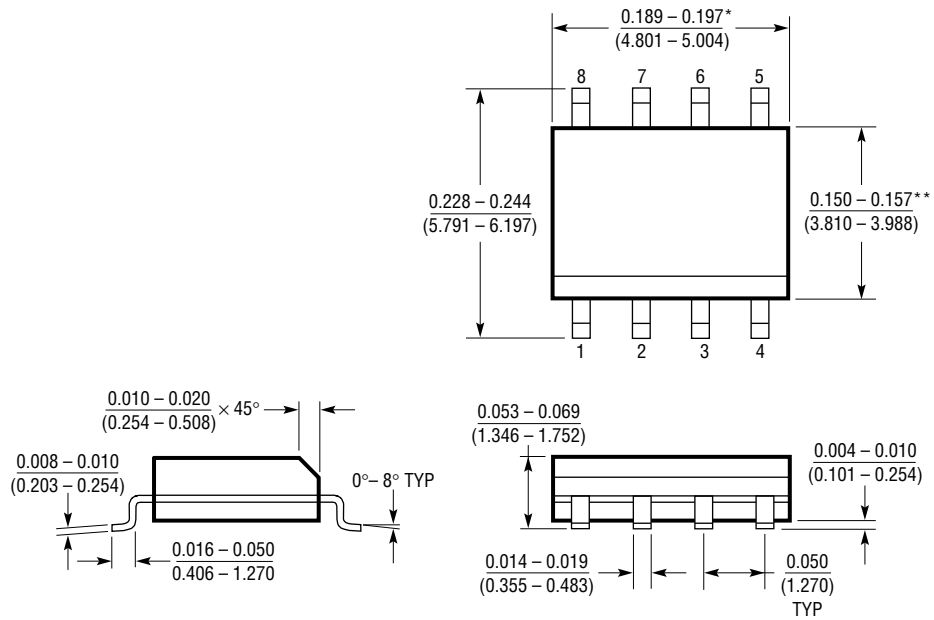
N8 Package
8-Lead PDIP (Narrow 0.300)
 (LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
 (LTC DWG # 05-08-1610)

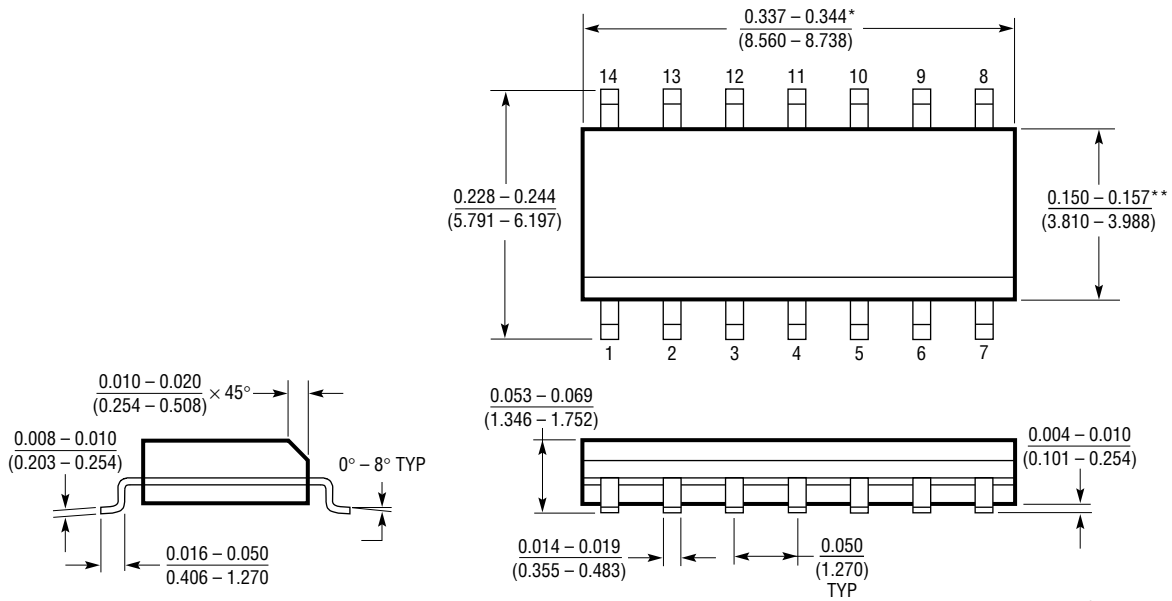


*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
 **DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S08 0996

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

S Package
14-Lead Plastic Small Outline (Narrow 0.150)
 (LTC DWG # 05-08-1610)

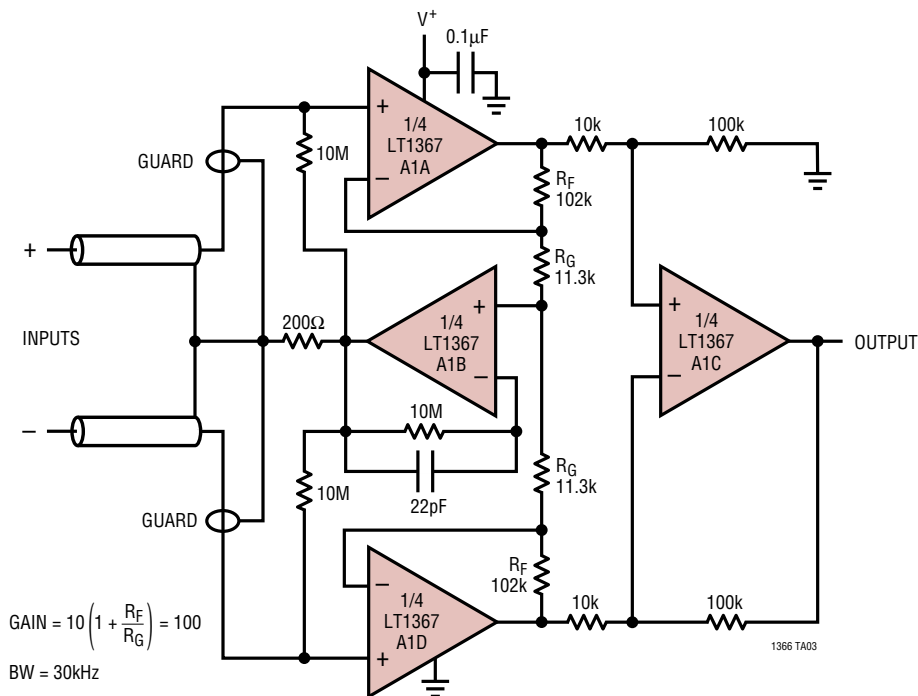


* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
 ** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S14 0695

TYPICAL APPLICATION

Instrumentation Amplifier



RELATED PARTS

PART	DESCRIPTION	COMMENTS
LT1078/LT1079	Dual/Quad 55μA Max, Single Supply, Precision Op Amps	Input/Output Common Mode Includes Ground, 70μV $V_{OS(MAX)}$ and 2.5μV/°C Drift (Max), 200kHz GBW, 0.07V/μs Slew Rate
LTC1152	Rail-to-Rail Input, Rail-to-Rail Output, Zero-Drift Amplifier	High DC Accuracy, 10μV $V_{OS(MAX)}$, 100nV/°C Drift, 1MHz GBW, 1V/μs Slew Rate, Supply Current 2.2mA (Max), Single Supply, Can Be Configured for C-Load™ Operation
LT1178/LT1179	Dual/Quad 17μA Max, Single Supply, Precision Op Amps	Input/Output Common Mode Includes Ground, 70μV $V_{OS(MAX)}$ and 4μV/°C Drift (Max), 85kHz GBW, 0.04V/μs Slew Rate
LT1211/LT1212	Dual/Quad 14MHz, 7V/μs, Single Supply, Precision Op Amps	Input Common Mode Includes Ground, 275μV $V_{OS(MAX)}$ and 6μV/°C Drift (Max), Supply Current 1.8mA per Op Amp (Max)
LT1495/LT1496	1.5μA, Rail-to-Rail Input/Output Dual/Quad	375μV $V_{OS(MAX)}$, 2μV/°C Drift (Max), "Over-the-Top" Input

C-Load is a trademark of Linear Technology Corporation