

FEATURES

- Trimmed to High Accuracy: 0.075% Max
- Low Drift: 10ppm/°C Max
- Industrial Temperature Range S0 Package
- Temperature Coefficient Guaranteed to 125°C
- Low Supply Current: 130μA Max
- Minimum Output Current: 20mA
- No Output Capacitor Required
- Reverse Battery Protection
- Minimum Input/Output Differential: 0.9V
- Available in Small MSOP Package

APPLICATIONS

- Handheld Instruments
- Precision Regulators
- A/D and D/A Converters
- Power Supplies
- Hard Disk Drives

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DESCRIPTION

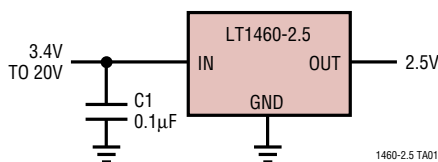
The LT[®]1460-2.5 is a micropower bandgap reference that combines very high accuracy and low drift with low power dissipation and small package size. This series reference uses curvature compensation to obtain low temperature coefficient and trimmed precision thin-film resistors to achieve high output accuracy. The reference will supply up to 20mA, making it ideal for precision regulator applications, yet it is almost totally immune to input voltage variations.

This series reference provides supply current and power dissipation advantages over shunt references that must idle the entire load current to operate. Additionally, the LT1460-2.5 does not require an output compensation capacitor, but it is stable with capacitive loads. This feature is important in critical applications where PC board space is a premium or fast settling is demanded. Reverse battery protection keeps the reference from conducting current and being damaged.

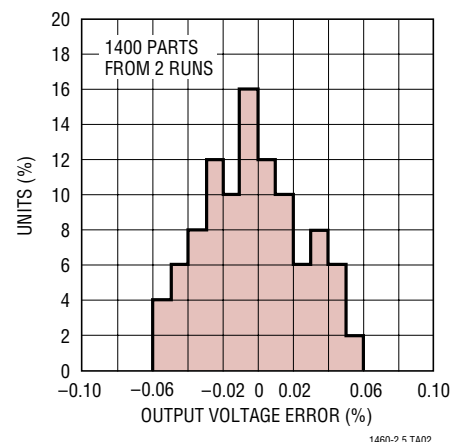
The LT1460-2.5 is available in the 8-lead MSOP, SO, PDIP and the 3-lead TO-92 packages. It is also available in the SOT-23 package (see separate data sheet LT1460S3-2.5).

TYPICAL APPLICATION

Basic Connection



Typical Distribution of Output Voltage
 S8 Package



ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage	30V	Specified Temperature Range	
Reverse Voltage	−15V	Commercial	0°C to 70°C
Output Short-Circuit Duration, $T_A = 25^\circ\text{C}$		Industrial	−40°C to 85°C
$V_{IN} > 10\text{V}$	5 sec	Storage Temperature Range (Note 2) ...	−65°C to 150°C
$V_{IN} \leq 10\text{V}$	Indefinite	Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW MS8 PACKAGE 8-LEAD PLASTIC MSOP *CONNECTED INTERNALLY. DO NOT CONNECT EXTERNAL CIRCUITRY TO THESE PINS TJMAX = 125°C, θJA = 250°C/W	TOP VIEW N8 PACKAGE 8-LEAD PDIP S8 PACKAGE 8-LEAD PLASTIC SO * CONNECTED INTERNALLY. DO NOT CONNECT EXTERNAL CIRCUITRY TO THESE PINS TJMAX = 125°C, θJA = 130°C/W (N8) TJMAX = 125°C, θJA = 190°C/W (S8)	BOTTOM VIEW Z PACKAGE 3-LEAD TO-92 PLASTIC TJMAX = 125°C, θJA = 160°C/W	
ORDER PART NUMBER	ORDER PART NUMBER		ORDER PART NUMBER
LT1460CCMS8-2.5 LT1460FCMS8-2.5	LT1460ACN8-2.5 LT1460BIN8-2.5 LT1460DCN8-2.5 LT1460EIN8-2.5	LT1460ACS8-2.5 LT1460BIS8-2.5 LT1460DCS8-2.5 LT1460EIS8-2.5	LT1460LHS8-2.5 LT1460MHS8-2.5
MS8 PART MARKING	S8 PART MARKING		
LTAA LTAB	1460A2 460BI2	1460D2 460EI2	460LH2 460MH2

Consult factory for Military grade parts.

Available Options

TEMPERATURE	ACCURACY (%)	TEMPERATURE COEFFICIENT (ppm/°C)	PACKAGE TYPE			
			N8	S8	MS8	Z
0°C to 70°C	0.075	10	LT1460ACN8-2.5	LT1460ACS8-2.5		
−40°C to 85°C	0.10	10	LT1460BIN8-2.5	LT1460BIS8-2.5		
0°C to 70°C	0.10	15			LT1460CCMS8-2.5	
0°C to 70°C	0.10	20	LT1460DCN8-2.5	LT1460DCS8-2.5		
−40°C to 85°C	0.125	20	LT1460EIN8-2.5	LT1460EIS8-2.5		
0°C to 70°C	0.15	25			LT1460FCMS8-2.5	
0°C to 70°C	0.25	25				LT1460GCZ-2.5
−40°C to 85°C	0.25	25				LT1460GIZ-2.5
−40°C to 85°C/125°C	0.20	20/50		LT1460LHS8-2.5		
−40°C to 125°C	0.20	50		LT1460MHS8-2.5		

ELECTRICAL CHARACTERISTICS

$V_{IN} = 5V$, $I_{OUT} = 0$, $T_A = 25^\circ C$ unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage (Note 3)	LT1460ACN8, ACS8	2.49813 −0.075	2.500	2.50188 0.075	V %
	LT1460BIN8, BIS8, CCMS8, DCN8, DCS8	2.4975 −0.10	2.500	2.5025 0.10	V %
	LT1460EIN8, EIS8	2.49688 −0.125	2.500	2.50313 0.125	V %
	LT1460FCMS8	2.49625 −0.15	2.500	2.50375 0.15	V %
	LT1460GCZ, GIZ	2.49375 −0.25	2.500	2.50625 0.25	V %
	LT1460LHS8, MHS8	2.495 −0.20	2.500	2.505 0.20	V %
Output Voltage Temperature Coefficient (Note 4)	$T_{MIN} \leq T_J \leq T_{MAX}$				
	LT1460ACN8, ACS8, BIN8, BIS8	●	5	10	ppm/°C
	LT1460CCMS8	●	7	15	ppm/°C
	LT1460DCN8, DCS8, EIN8, EIS8	●	10	20	ppm/°C
	LT1460FCMS8, GCZ, GIZ	●	12	25	ppm/°C
	LT1460LHS8 −40°C to 85°C	●	10	20	ppm/°C
	LT1460LHS8 −40°C to 125°C	●	25	50	ppm/°C
Line Regulation	$3.4V \leq V_{IN} \leq 5V$	●	30	60 80	ppm/V ppm/V
	$5V \leq V_{IN} \leq 20V$	●	10	25 35	ppm/V ppm/V
Load Regulation Sourcing (Note 5)	$I_{OUT} = 100\mu A$	●	1500	2800 3500	ppm/mA ppm/mA
	$I_{OUT} = 10mA$	●	80	135 180	ppm/mA ppm/mA
	$I_{OUT} = 20mA$ 0°C to 70°C	●	70	100 140	ppm/mA ppm/mA
Thermal Regulation (Note 6)	$\Delta P = 200mW$		0.5	2.5	ppm/mW
Dropout Voltage (Note 7)	$V_{IN} - V_{OUT}$, $\Delta V_{OUT} \leq 0.1\%$, $I_{OUT} = 0$	●		0.9	V
	$V_{IN} - V_{OUT}$, $\Delta V_{OUT} \leq 0.1\%$, $I_{OUT} = 10mA$	●		1.3 1.4	V V
Output Current	Short V_{OUT} to GND		40		mA
Reverse Leakage	$V_{IN} = -15V$	●	0.5	10	μA
Supply Current		●	100	130	μA
				165	μA
Output Voltage Noise (Note 8)	$0.1Hz \leq f \leq 10Hz$		10		μV _{P-P}
	$10Hz \leq f \leq 1kHz$		10		μV _{RMS}
Long-Term Stability of Output Voltage, S8 Pkg (Note 9)			40		ppm/√kHr
Hysteresis (Note 10)	$\Delta T = -40^\circ C$ to $85^\circ C$		160		ppm
	$\Delta T = 0^\circ C$ to $70^\circ C$		25		ppm

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the specified temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: If the part is stored outside of the specified temperature range, the output may shift due to hysteresis.

Note 3: ESD (Electrostatic Discharge) sensitive device. Extensive use of ESD protection devices are used internal to the LT1460, however, high electrostatic discharge can damage or degrade the device. Use proper ESD handling precautions.

Note 4: Temperature coefficient is measured by dividing the change in output voltage by the specified temperature range. Incremental slope is also measured at 25°C.

Note 5: Load regulation is measured on a pulse basis from no load to the specified load current. Output changes due to die temperature change must be taken into account separately.

Note 6: Thermal regulation is caused by die temperature gradients created by load current or input voltage changes. This effect must be added to normal line or load regulation. This parameter is not 100% tested.

Note 7: Excludes load regulation errors.

Note 8: Peak-to-peak noise is measured with a single highpass filter at 0.1Hz and 2-pole lowpass filter at 10Hz. The unit is enclosed in a still-air environment to eliminate thermocouple effects on the leads. The test time

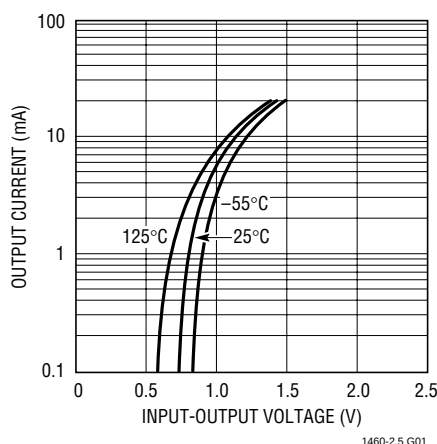
is 10 sec. RMS noise is measured with a single highpass filter at 10Hz and a 2-pole lowpass filter at 1kHz. The resulting output is full wave rectified and then integrated for a fixed period, making the final reading an average as opposed to RMS. A correction factor of 1.1 is used to convert from average to RMS and a second correction of 0.88 is used to correct for the nonideal bandpass of the filters.

Note 9: Long-term stability typically has a logarithmic characteristic and therefore, changes after 1000 hours tend to be much smaller than before that time. Total drift in the second thousand hours is normally less than one third that of the first thousand hours with a continuing trend toward reduced drift with time. Significant improvement in long-term drift can be realized by preconditioning the IC with a 100 hour to 200 hour, 125°C burn-in. Long-term stability will also be affected by differential stresses between the IC and the board material created during board assembly. See PC Board Layout in the Applications Information section.

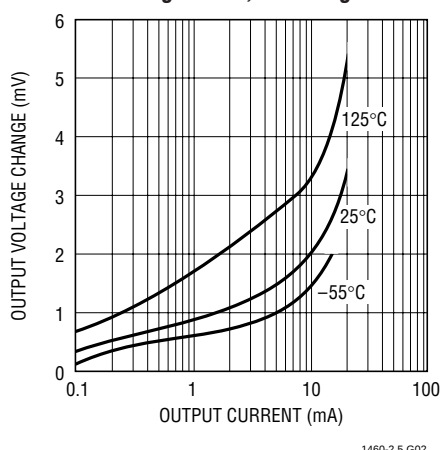
Note 10: Hysteresis in output voltage is created by package stress that differs depending on whether the IC was previously at a higher or lower temperature. Output voltage is always measured at 25°C, but the IC is cycled to 85°C or –40°C before successive measurements. Hysteresis is roughly proportional to the square of the temperature change. Hysteresis is not normally a problem for operational temperature excursions where the instrument might be stored at high or low temperature.

TYPICAL PERFORMANCE CHARACTERISTICS

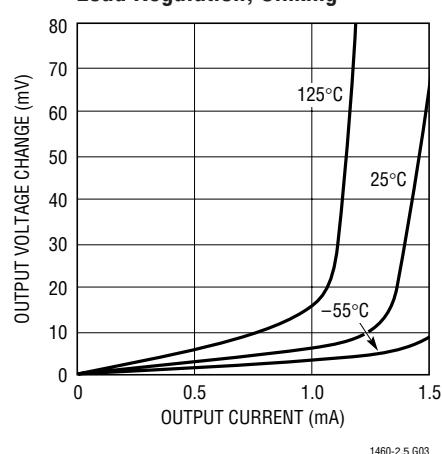
Minimum Input-Output Voltage Differential



Load Regulation, Sourcing

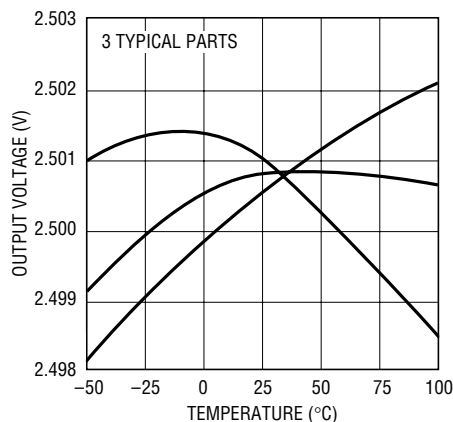


Load Regulation, Sinking

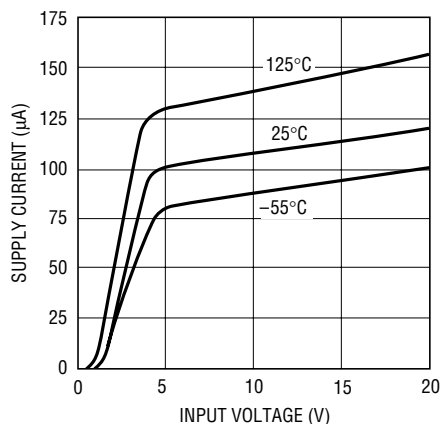


TYPICAL PERFORMANCE CHARACTERISTICS

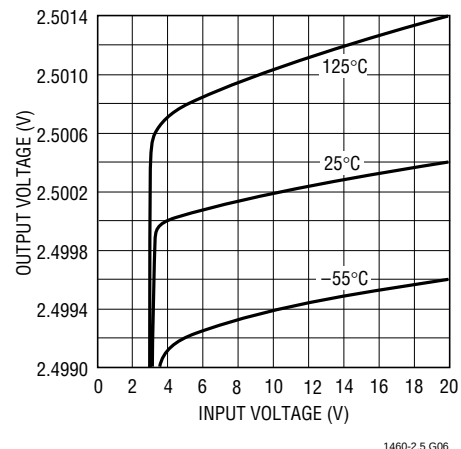
Output Voltage Temperature Drift



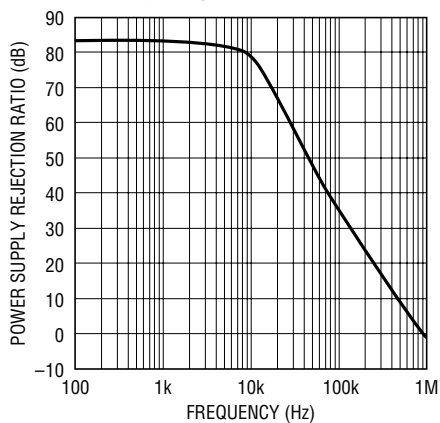
Supply Current vs Input Voltage



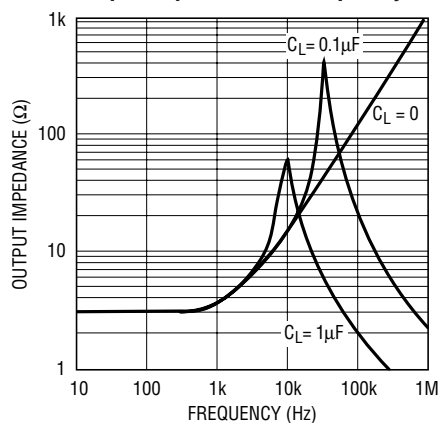
Line Regulation



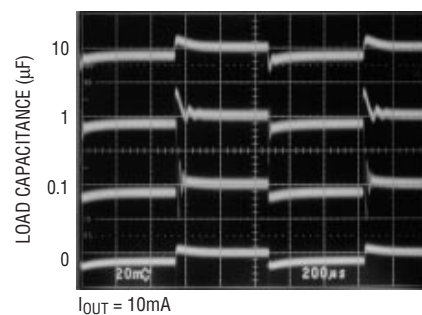
Power Supply Rejection Ratio vs Frequency



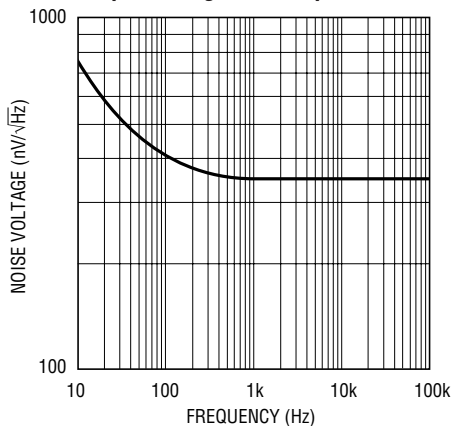
Output Impedance vs Frequency



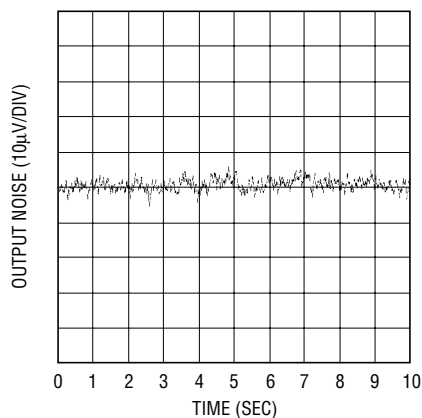
Transient Responses



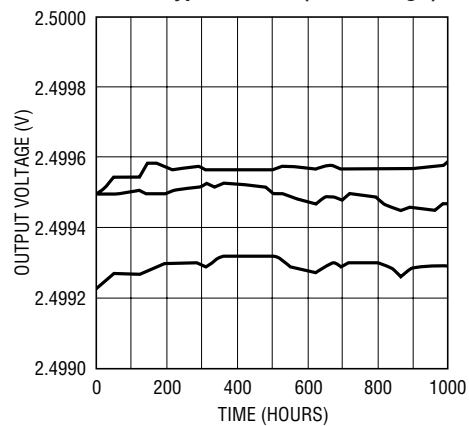
Output Voltage Noise Spectrum



Output Noise 0.1Hz to 10Hz



Long-Term Drift
Three Typical Parts (S8 Package)



APPLICATIONS INFORMATION

Longer Battery Life

Series references have a large advantage over older shunt style references. Shunt references require a resistor from the power supply to operate. This resistor must be chosen to supply the maximum current that can ever be demanded by the circuit being regulated. When the circuit being controlled is not operating at this maximum current, the shunt reference must always sink this current, resulting in high dissipation and short battery life.

The LT1460-2.5 series reference does not require a current setting resistor and can operate with any supply voltage from $V_{OUT} + 0.9V$ to 20V. When the circuitry being regulated does not demand current, the LT1460-2.5 reduces its dissipation and battery life is extended. If the reference is not delivering load current it dissipates only 500 μW on a 5V supply, yet the same configuration can deliver 20mA of load current when demanded.

Capacitive Loads

The LT1460-2.5 is designed to be stable with capacitive loads. With no capacitive load, the reference is ideal for fast settling or applications where PC board space is a premium. The test circuit shown in Figure 1 is used to measure the response time for various load currents and load capacitors. The 1V step from 2.5V to 1.5V produces a current step of 1mA or 100 μA for $R_L = 1k$ or $R_L = 10k$. Figure 2 shows the response of the reference with no load capacitance.

The reference settles to 2.5mV (0.1%) in less than 1 μs for a 100 μA pulse and to 0.1% in 1.5 μs with a 1mA step. When load capacitance is greater than 0.01 μF , the reference begins to ring due to the pole formed with the output impedance. Figure 3 shows the response of the reference to a 1mA and 100 μA load with a 0.01 μF load capacitor. The ringing can be greatly reduced with a DC load as small as 200 μA . With large output capacitors, $\geq 1\mu F$, the ringing can be reduced with a small resistor in series with the reference output as shown in Figure 4. Figure 5 shows the

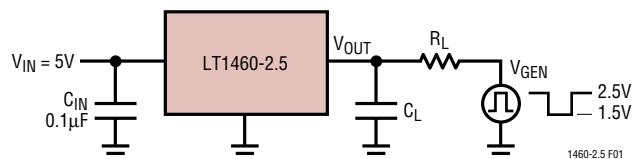


Figure 1. Response Time Test Circuit

response of the LT1460-2.5 with a $R_S = 2\Omega$ and $C_L = 1\mu F$. R_S should not be made arbitrarily large because it will limit the load regulation.

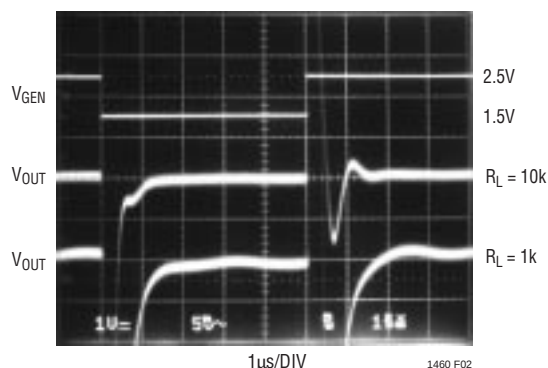


Figure 2. $C_L = 0$

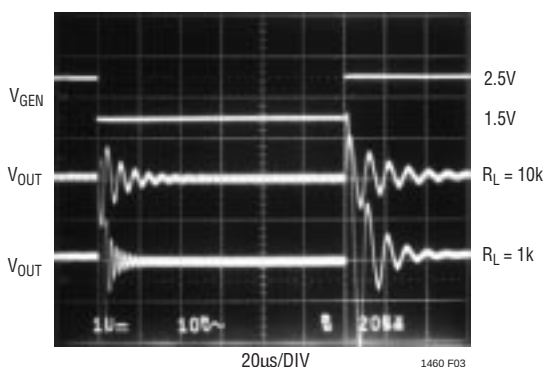


Figure 3. $C_L = 0.01\mu F$

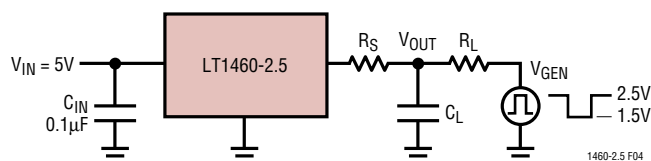


Figure 4. Isolation Resistor Test Circuit

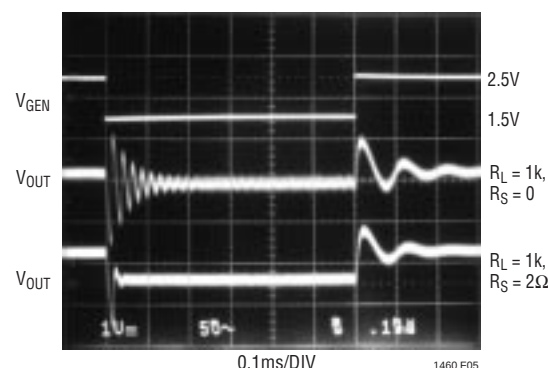


Figure 5. Effect of R_S for $C_L = 1\mu F$

APPLICATIONS INFORMATION

Fast Turn-On

It is recommended to add a 0.1μF or larger input capacitor to the input pin of the LT1460-2.5. This helps stability with large load currents and speeds up turn-on. The LT1460-2.5 can start in 2μs, but it is important to limit the dv/dt of the input. Under light load conditions and with a very fast input, internal nodes overslew and this requires finite recovery time. Figure 6 shows the result of no bypass capacitance on the input and no output load. In this case the supply dv/dt is 5V in 30ns which causes internal overslew, and the output does not bias to 2.5V until 500μs. Figure 7 shows the effect of a 0.1μF bypass capacitor

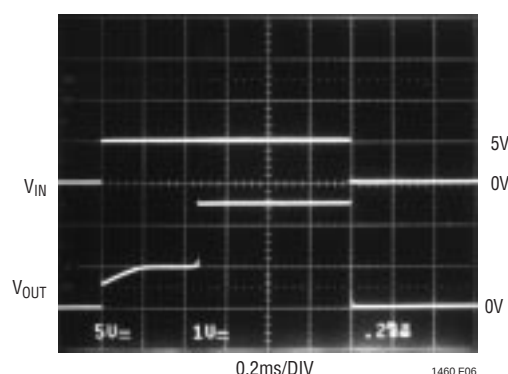


Figure 6. $C_{IN} = 0$

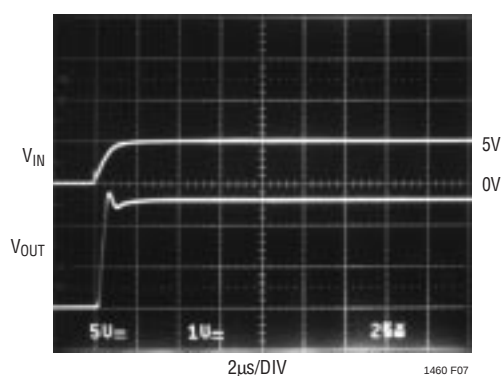


Figure 7. $C_{IN} = 0.1\mu F$

which limits the input dv/dt to approximately 5V in 2μs and the output settles quickly.

Output Accuracy

Like all references, either series or shunt, the error budget of the LT1460-2.5 is made up of primarily three components: initial accuracy, temperature coefficient and load regulation. Line regulation is neglected because it typically contributes only 30ppm/V, or 75μV for a 1V input change. The LT1460-2.5 typically shifts less than 0.01% when soldered into a PCB, so this is also neglected (see PCB Board Layout section). The output errors are calculated as follows for a 100μA load and 0°C to 70°C temperature range:

LT1460AC

Initial accuracy = 0.075%

For $I_O = 100\mu A$,

$$\Delta V_{OUT} = \left(\frac{3500 \text{ ppm}}{\text{mA}} \right) (0.1 \text{ mA}) (2.5 \text{ V}) = 875 \mu \text{ V}$$

which is 0.035%.

For temperature 0°C to 70°C the maximum $\Delta T = 70^\circ \text{C}$,

$$\Delta V_{OUT} = \left(\frac{10 \text{ ppm}}{^\circ \text{C}} \right) (70^\circ \text{C}) (2.5 \text{ V}) = 1.75 \text{ mV}$$

which is 0.07%.

Total worst-case output error is:

$$0.075\% + 0.035\% + 0.070\% = 0.180\%.$$

Table 1 gives worst-case accuracy for the LT1460AC, CC, DC, FC, GC from 0°C to 70°C and the LT1460BI, EI, GI from -40°C to 85°C.

Table 1. Worst-Case Output Accuracy Over Temperature

I_{OUT}	LT1460AC	LT1460BI	LT1460CC	LT1460DC	LT1460EI	LT1460FC	LT1460GC	LT1460GI
0	0.145%	0.225%	0.205%	0.240%	0.375%	0.325%	0.425%	0.562%
100μA	0.180%	0.260%	0.240%	0.275%	0.410%	0.360%	0.460%	0.597%
10mA	0.325%	0.405%	0.385%	0.420%	0.555%	0.505%	0.605%	0.742%
20mA	0.425%	N/A	0.485%	0.520%	N/A	0.605%	0.705%	N/A

APPLICATIONS INFORMATION

PC Board Layout

In 13- to 16-bit systems where initial accuracy and temperature coefficient calibrations have been done, the mechanical and thermal stress on a PC board (in a cardcage for instance) can shift the output voltage and mask the true temperature coefficient of a reference. In addition, the mechanical stress of being soldered into a PC board can cause the output voltage to shift from its ideal value. Surface mount voltage references (MS8 and S8) are the most susceptible to PC board stress because of the small amount of plastic used to hold the lead frame.

A simple way to improve the stress-related shifts is to mount the reference near the short edge of the PC board, or in a corner. The board edge acts as a stress boundary, or a region where the flexure of the board is minimum. The package should always be mounted so that the leads absorb the stress and not the package. The package is generally aligned with the leads parallel to the long side of the PC board as shown in Figure 9a.

A qualitative technique to evaluate the effect of stress on voltage references is to solder the part into a PC board and deform the board a fixed amount as shown in Figure 8. The flexure #1 represents no displacement, flexure #2 is concave movement, flexure #3 is relaxation to no displacement and finally, flexure #4 is a convex movement. This motion is repeated for a number of cycles and the relative output deviation is noted. The result shown in Figure 9a is for two LT1460S8-2.5s mounted vertically and Figure 9b is for two LT1460S8-2.5s mounted horizontally. The parts oriented in Figure 9a impart less stress into the package because stress is absorbed in the leads. Figures 9a and 9b show the deviation to be between 125 μ V and 250 μ V and implies a 50ppm and 100ppm change respectively. This corresponds to a 13- to 14-bit system and is not a problem for most 10- to 12-bit systems unless the system has a calibration. In this case, as with temperature hysteresis, this low level can be important and even more careful techniques are required.

The most effective technique to improve PC board stress is to cut slots in the board around the reference to serve as a strain relief. These slots can be cut on three sides of the

reference and the leads can exit on the fourth side. This “tongue” of PC board material can be oriented in the long direction of the board to further reduce stress transferred to the reference.

The results of slotting the PC boards of Figures 9a and 9b are shown in Figures 10a and 10b. In this example the slots can improve the output shift from about 100ppm to nearly zero.

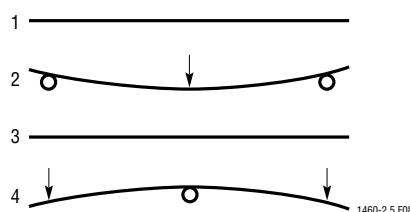


Figure 8. Flexure Numbers

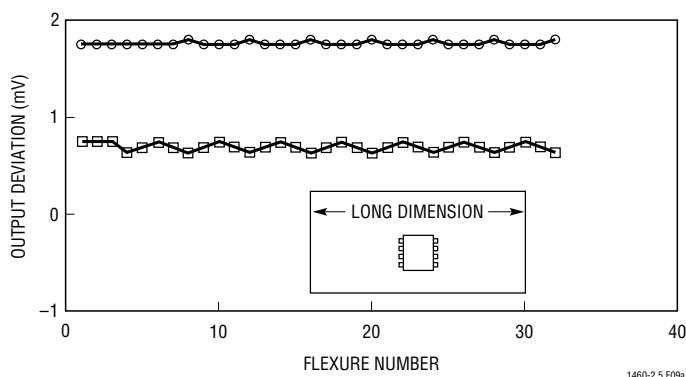


Figure 9a. Two Typical LT1460S8-2.5s, Vertical Orientation Without Slots

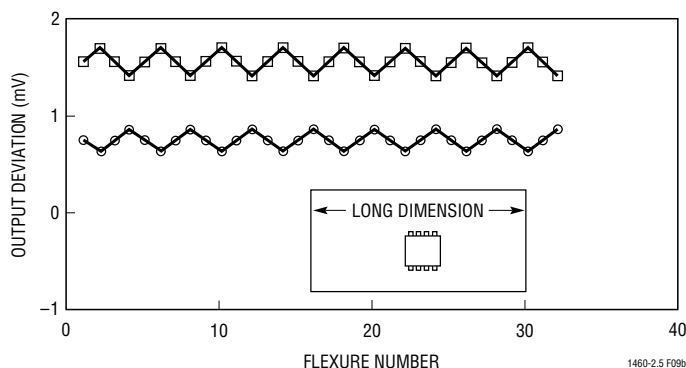


Figure 9b. Two Typical LT1460S8-2.5s, Horizontal Orientation Without Slots

APPLICATIONS INFORMATION

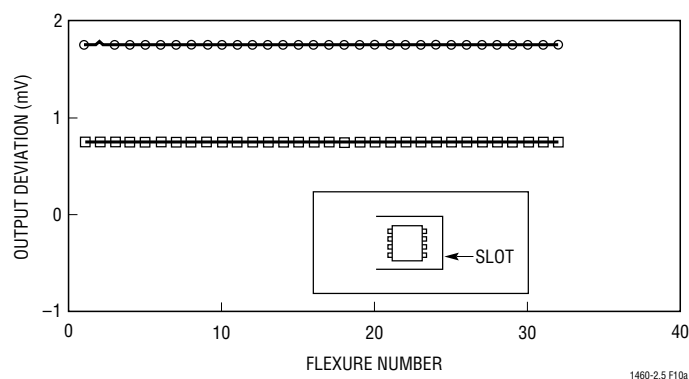


Figure 10a. Same Two LT1460S8-2.5s in Figure 9a, but With Slots

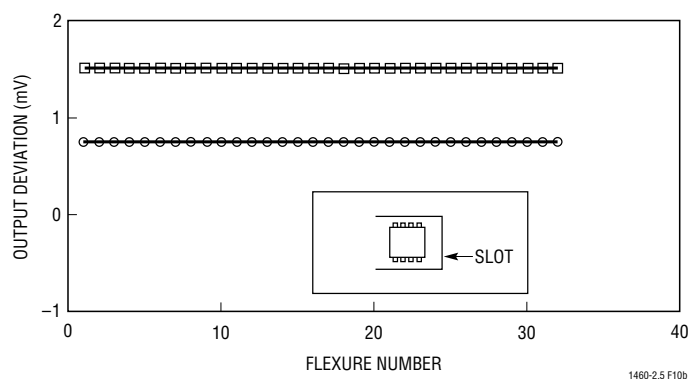
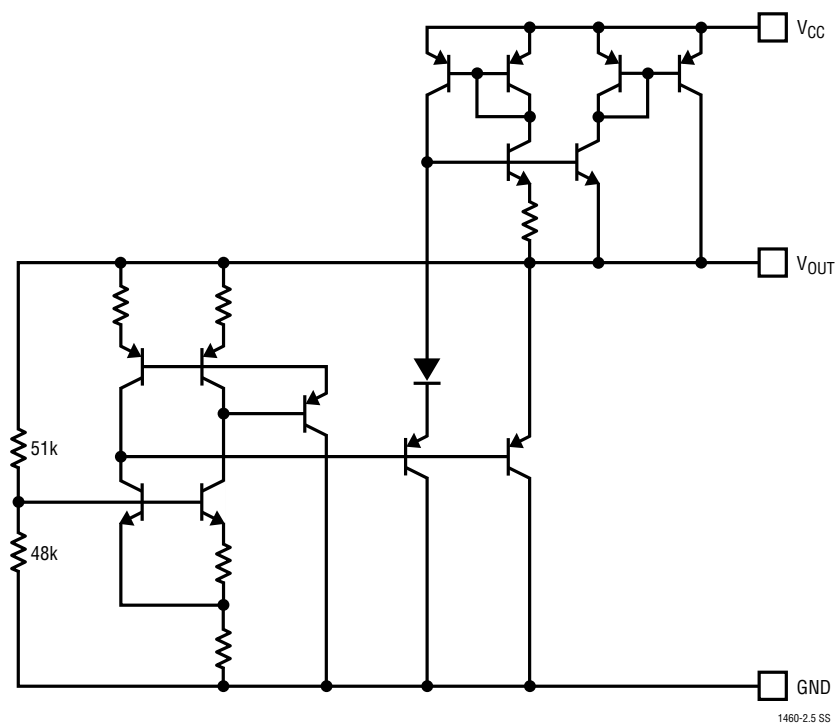


Figure 10b. Same Two LT1460S8-2.5s in Figure 9b, but With Slots

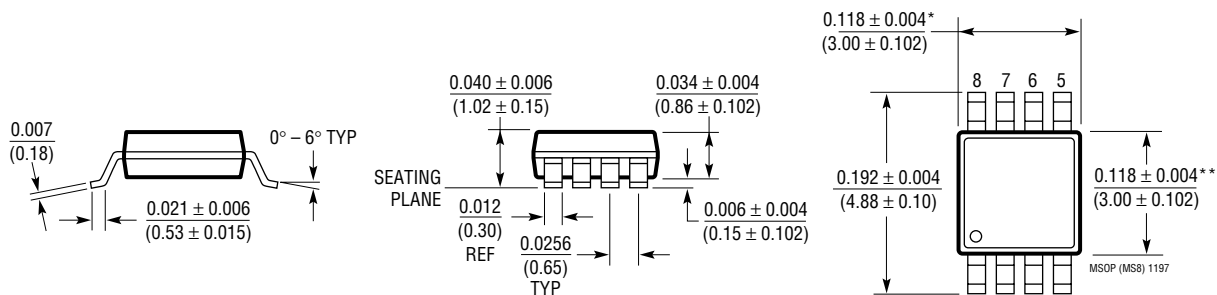
SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

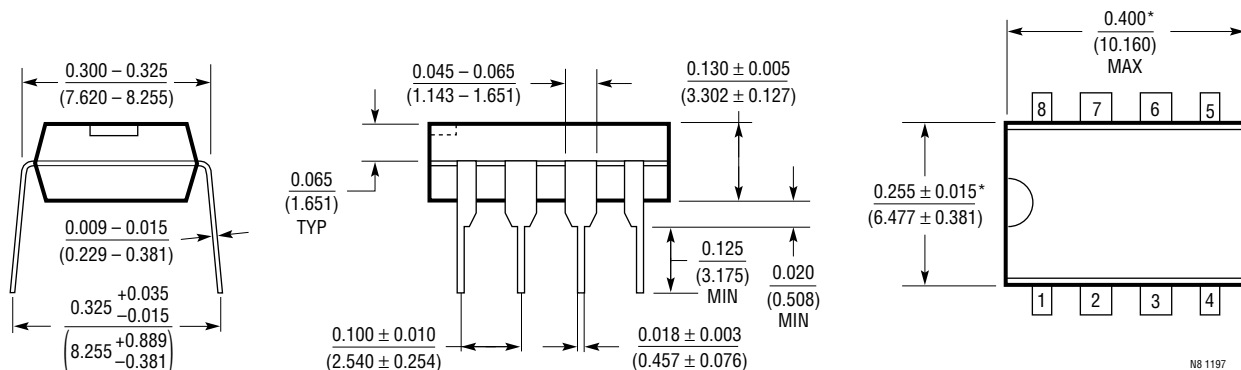
MS8 Package 8-Lead Plastic MSOP (LTC DWG # 05-08-1660)



* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006^* (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006^* (0.152mm) PER SIDE

N8 Package 8-Lead PDIP (Narrow 0.300) (LTC DWG # 05-08-1510)

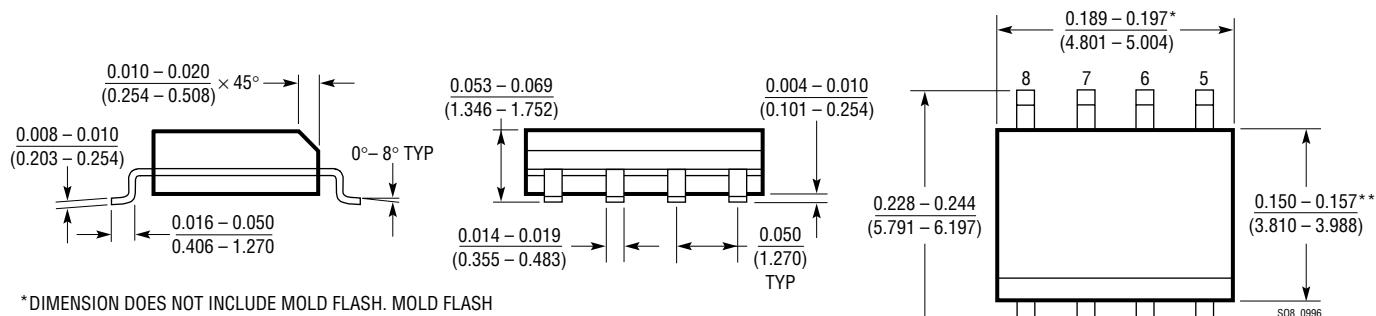


* THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

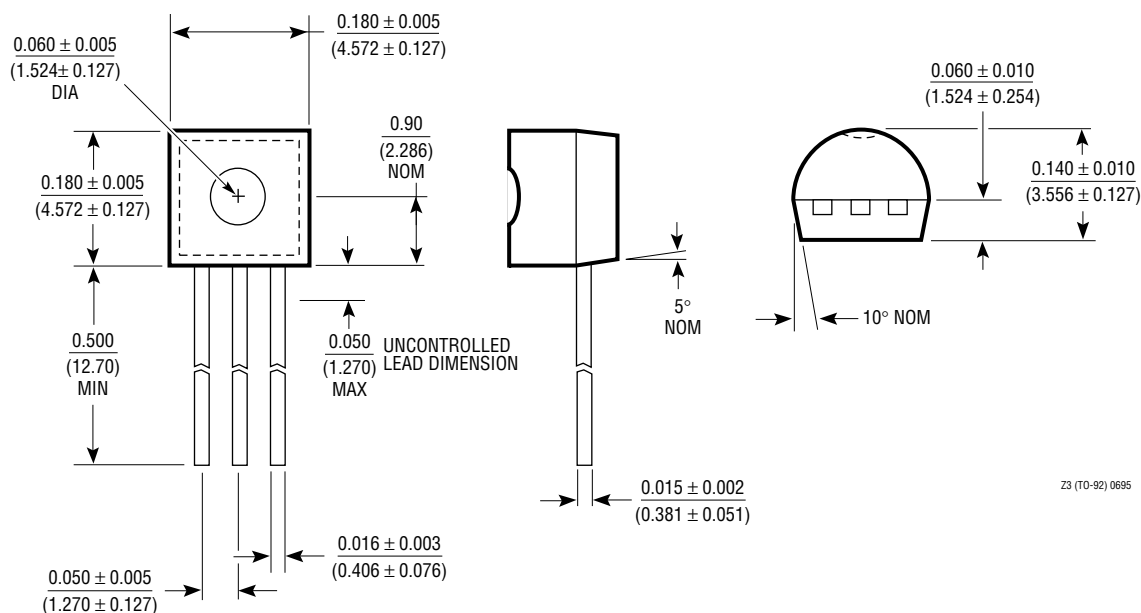
S8 Package 8-Lead Plastic Small Outline (Narrow 0.150) (LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

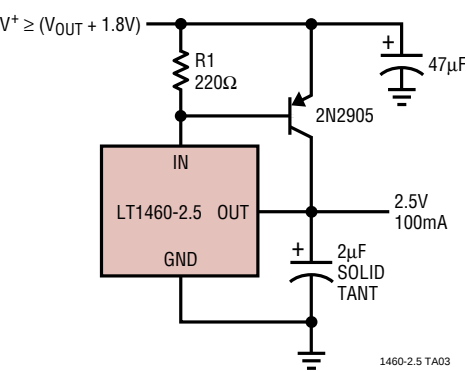
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

Z Package 3-Lead Plastic TO-92 (Similar to TO-226) (LTC DWG # 05-08-1410)

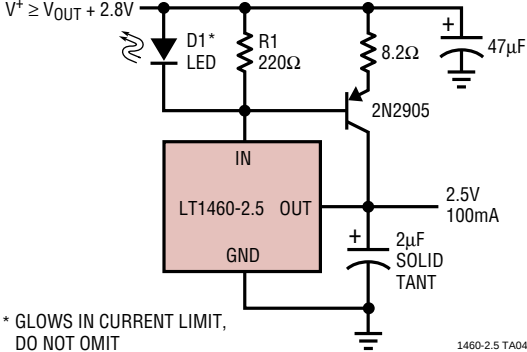


TYPICAL APPLICATIONS

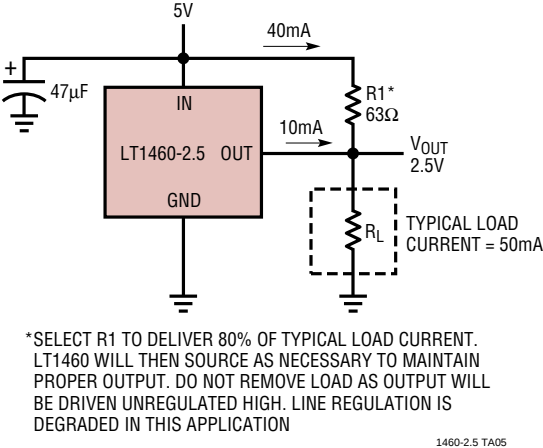
Boosted Output Current with No Current Limit



Boosted Output Current with Current Limit



Handling Higher Load Currents



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1236	Precision Low Noise Reference	0.05% Max, 5ppm/°C Max, SO Package
LT1019	Precision Bandgap Reference	0.05% Max, 5ppm/°C Max
LT1027	Precision 5V Reference	0.02%, 2ppm/°C Max