

3.3V Low Power EIA/TIA562 Transceiver

FEATURES

- Operates from a Single 3.3V Supply
- Low Supply Current: $I_{CC} = 200\mu A$
- ESD Protection Over $\pm 10kV$
- Available in 16-Pin SOIC Narrow Package
- Uses Small Capacitors: $0.1\mu F$
- Operates to 120kbaud
- Output Overvoltage Does Not Force Current Back into Supplies
- EIA/TIA562 I/O Lines Can Be Forced to $\pm 25V$ Without Damage
- Pin Compatible with LT1181A

APPLICATIONS

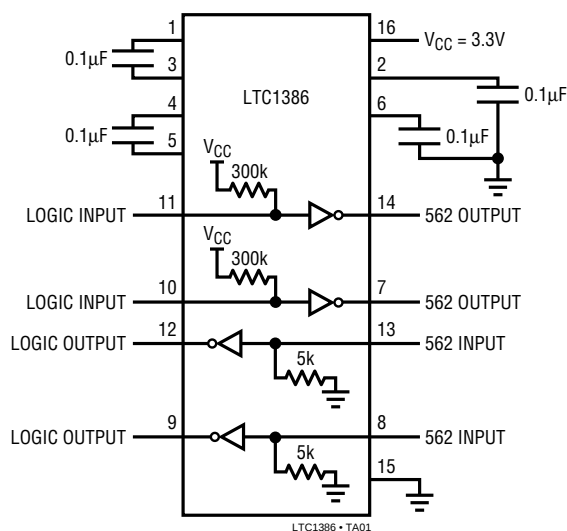
- Notebook Computers
- Palmtop Computers

DESCRIPTION

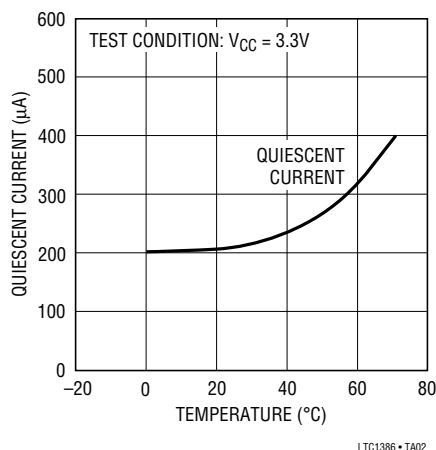
The LTC1386 is an ultra-low power 2-driver/2-receiver EIA/TIA562 transceiver that operates from a single 3.3V supply. The charge pump requires only four space-saving $0.1\mu F$ capacitors. The supply current (I_{CC}) of the transceiver is only $200\mu A$ with driver outputs unloaded.

The LTC1386 is fully compliant with all data rate and overvoltage EIA/TIA562 specifications. The transceiver can operate up to 120kbaud with a $1000pF$, $3k\Omega$ load. Both driver outputs and receiver inputs can be forced to $\pm 25V$ without damage and can survive multiple $\pm 10kV$ ESD strikes.

TYPICAL APPLICATION



Quiescent Supply Current vs Temperature



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})	5V
Input Voltage	
Driver	-0.3V to $V_{CC} + 0.3V$
Receiver	-25V to 25V
Digital Input	-0.3V to $V_{CC} + 0.3V$
Output Voltage	
Driver	-25V to 25V
Receiver	-0.3V to $V_{CC} + 0.3V$
Short-Circuit Duration	
V^+	30 sec
V^-	30 sec
Driver Output	Indefinite
Receiver Output	Indefinite
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW N PACKAGE 16-LEAD PLASTIC DIP S PACKAGE 16-LEAD NARROW PLASTIC SOIC $T_{JMAX} = 125^{\circ}C$, $\theta_{JA} = 65^{\circ}C/W$ (N) $T_{JMAX} = 125^{\circ}C$, $\theta_{JA} = 95^{\circ}C/W$ (S)	ORDER PART NUMBER
	LTC1386CN LTC1386CS

Consult factory for Industrial and Military grade parts.

DC ELECTRICAL CHARACTERISTICS

 $V_{CC} = 3.3V$, $C1 = C2 = C3 = C4 = 0.1\mu F$, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Any Driver					
Output Voltage Swing	3k to GND	Positive	3.7	4.5	V
		Negative	-3.7	-4.5	V
Logic Input Voltage Level	Input Low Level ($V_{OUT} = \text{High}$)	0.8	1.3		V
	Input High Level ($V_{OUT} = \text{Low}$)	2.0	1.4	0.8	V
Logic Input Current	$V_{IN} = V_{CC}$			5	μA
	$V_{IN} = 0V$		-20	-40	μA
Output Short-Circuit Current	$V_{OUT} = 0V$		± 10		mA
Any Receiver					
Input Voltage Thresholds	Input Low Threshold	0.8	1.3		V
	Input High Threshold		1.7	2.4	V
Hysteresis		0.1	0.4	1	V
Input Resistance	$-10V \leq V_{IN} \leq 10V$	3	5	7	k Ω
Output Voltage	Output Low, $I_{OUT} = -1.6mA$ ($V_{CC} = 3.3V$)		0.2	0.4	V
	Output High, $I_{OUT} = 160\mu A$ ($V_{CC} = 3.3V$)	3.0	3.2		V
Output Short-Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$	-5	-20		mA
	Sourcing Current, $V_{OUT} = GND$	2	7		mA
Power Supply Generator					
V^+ Output Voltage	$I_{OUT} = 0mA$		5.7		V
	$I_{OUT} = 5mA$		5.5		V
V^- Output Voltage	$I_{OUT} = 0mA$		-5.3		V
	$I_{OUT} = -5mA$		-5.0		V
Power Supply					
V_{CC} Supply Current	No Load (Note 2)		0.2	0.5	mA

AC CHARACTERISTICS $V_{CC} = 3.3V$, $C_1 = C_2 = C_3 = C_4 = 0.1\mu F$, unless otherwise noted.

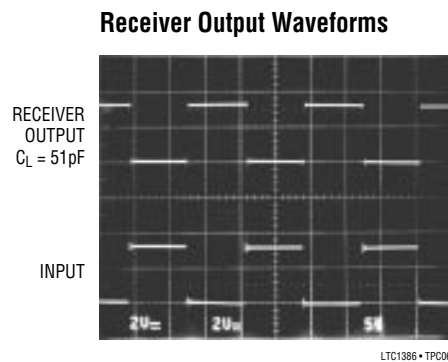
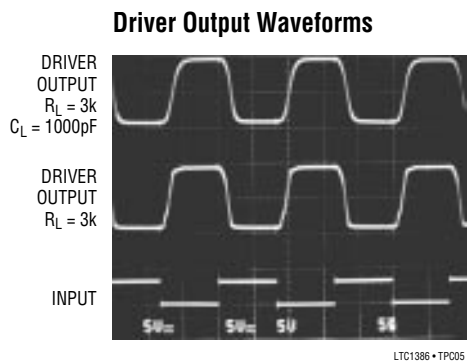
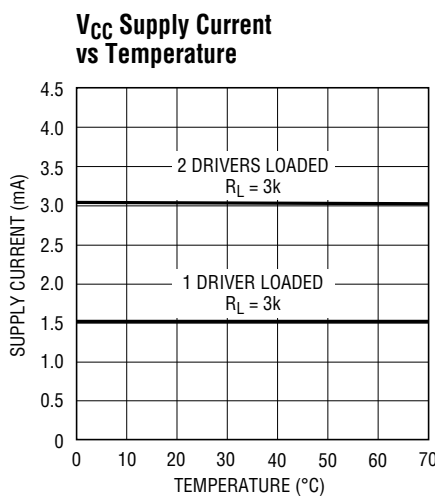
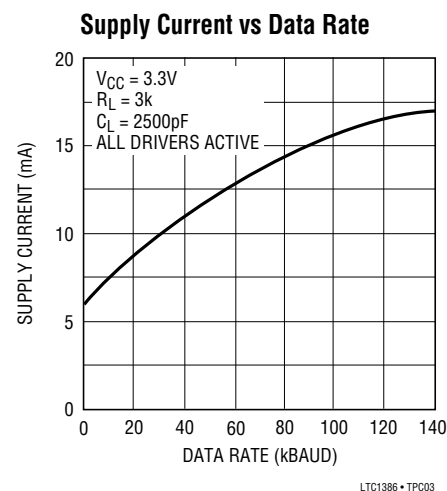
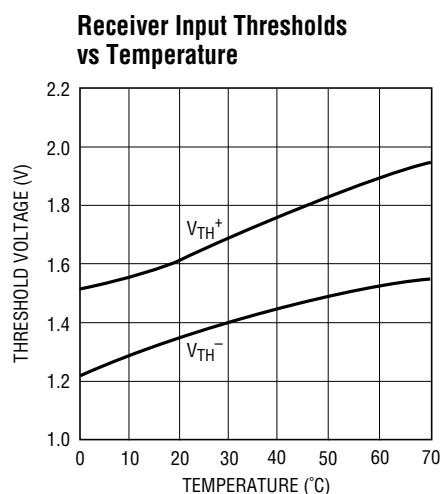
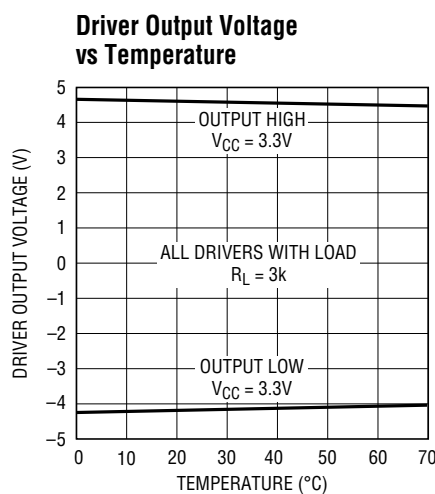
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Slew Rate	$R_L = 3k$, $C_L = 51pF$		8	30	$V/\mu s$
	$R_L = 3k$, $C_L = 1000pF$	3	5		$V/\mu s$
Driver Propagation Delay (TTL to EIA/TIA562)	t_{HLD} (Figure 1)	●	2	3.5	μs
	t_{LHD} (Figure 1)	●	2	3.5	μs
Receiver Propagation Delay (EIA/TIA562 to TTL)	t_{HLR} (Figure 2)	●	0.3	0.8	μs
	t_{LHR} (Figure 2)	●	0.3	0.8	μs

The ● denotes specifications which apply over the operating temperature range of $0^\circ C \leq T_A \leq 70^\circ C$.

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: Supply current is measured with driver and receiver outputs unloaded.

TYPICAL PERFORMANCE CHARACTERISTICS



PIN FUNCTIONS

V_{CC}: 3.3V Input Supply Pin. This pin should be decoupled with a 0.1μF ceramic capacitor.

GND: Ground Pin.

V⁺: Positive Supply Output (EIA/TIA562 Drivers). $V^+ \cong 2V_{CC} - 1V$. This pin requires an external capacitor $C = 0.1\mu F$ for charge storage. The capacitor may be tied to ground or V_{CC} . With multiple devices, the V^+ and V^- pins may share a common capacitor. For large numbers of devices, increasing the size of the shared common storage capacitors is recommended to reduce ripple.

V⁻: Negative Supply Output (RS232 Drivers). $V^- \cong -(2V_{CC} - 1.3V)$. This pin requires an external capacitor $C = 0.1\mu F$ for charge storage.

C1⁺, C1⁻, C2⁺, C2⁻: Commutating Capacitor Inputs. These pins require two external capacitors $C = 0.1\mu F$: one from C1⁺ to C1⁻ and another from C2⁺ to C2⁻. To maintain

charge pump efficiency, the capacitor's effective series resistance should be less than 2Ω.

TR IN: EIA/TIA562 Driver Input Pins. Inputs are TTL/CMOS compatible. The inputs of unused drivers can be left unconnected since 300k input pull-up resistors to V_{CC} are included on chip.

TR OUT: Driver Outputs at EIA/TIA562 Voltage Levels. The driver outputs are protected against ESD to ±10kV for human body model discharges.

RX IN: Receiver Inputs. These pins can be forced to ±25V without damage. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity.

RX OUT: Receiver Outputs with TTL/CMOS Voltage Levels.

SWITCHING TIME WAVEFORMS

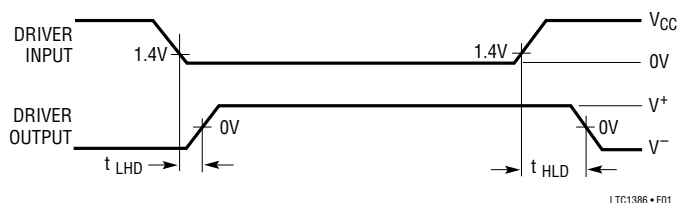


Figure 1. Driver Propagation Delay Timing

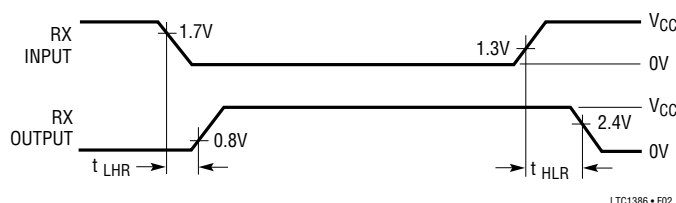
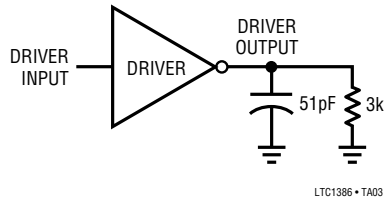


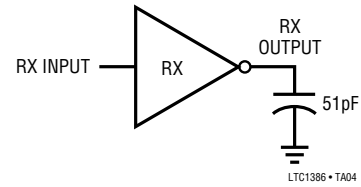
Figure 2. Receiver Propagation Delay Timing

TEST CIRCUITS

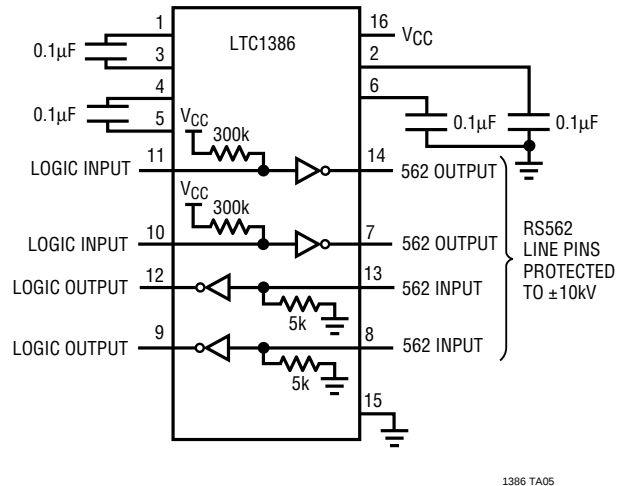
Driver Timing Test Load



Receiver Timing Test Load



ESD Test Circuit



The left diagram shows the LTC1386 with the following connections:

- Supply:** Pin 16 is connected to $V_{CC} = 3.3V$. Pin 2 is connected to a $0.1\mu F$ capacitor to ground. Pin 6 is connected to a $0.1\mu F$ capacitor to ground.
- Logic Inputs:** Pin 11 is connected to a $0.1\mu F$ capacitor to ground. Pin 10 is connected to a $0.1\mu F$ capacitor to ground. Pin 12 is connected to a $300k\Omega$ resistor to V_{CC} and a $5k\Omega$ resistor to ground.
- Logic Outputs:** Pin 9 is connected to a $300k\Omega$ resistor to V_{CC} and a $5k\Omega$ resistor to ground. Pin 14 is connected to a $300k\Omega$ resistor to V_{CC} and a $5k\Omega$ resistor to ground.
- 562 Inputs:** Pin 13 is connected to a $5k\Omega$ resistor to ground. Pin 8 is connected to a $5k\Omega$ resistor to ground.
- 562 Outputs:** Pin 14 is connected to a $300k\Omega$ resistor to V_{CC} and a $5k\Omega$ resistor to ground. Pin 7 is connected to a $300k\Omega$ resistor to V_{CC} and a $5k\Omega$ resistor to ground.

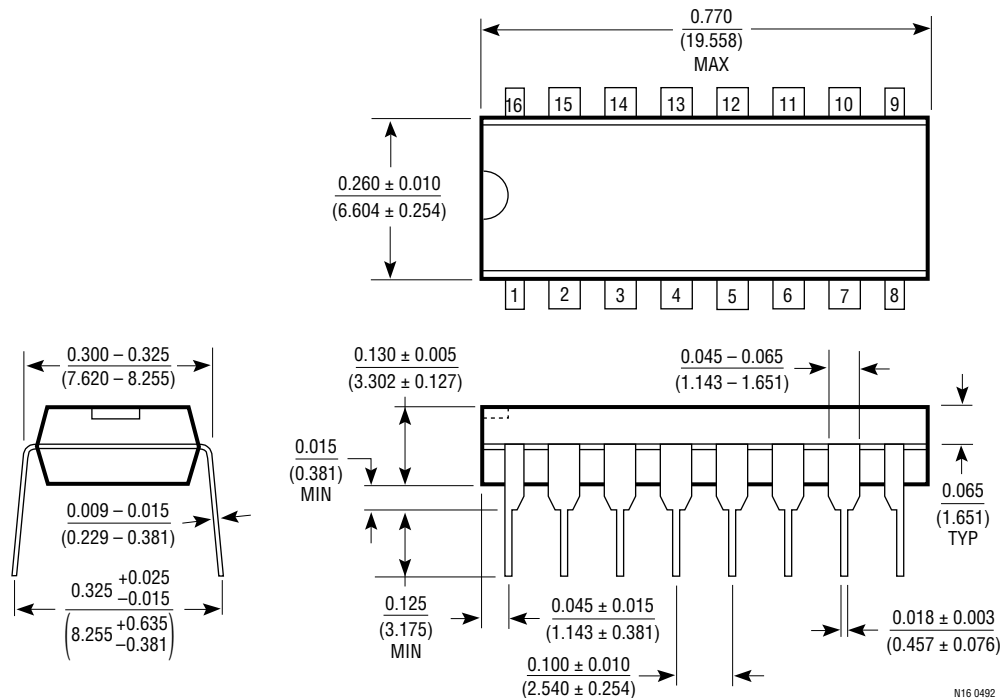
The right diagram shows the LTC1386 with the following connections:

- Supply:** Pin 16 is connected to $V_{CC} = 3.3V$. Pin 2 is connected to a $0.1\mu F$ capacitor to ground. Pin 6 is connected to a $0.1\mu F$ capacitor to ground.
- Logic Inputs:** Pin 11 is connected to a $0.1\mu F$ capacitor to ground. Pin 10 is connected to a $0.1\mu F$ capacitor to ground. Pin 12 is connected to a $300k\Omega$ resistor to V_{CC} and a $5k\Omega$ resistor to ground.
- Logic Outputs:** Pin 9 is connected to a $300k\Omega$ resistor to V_{CC} and a $5k\Omega$ resistor to ground. Pin 14 is connected to a $300k\Omega$ resistor to V_{CC} and a $5k\Omega$ resistor to ground.
- 562 Inputs:** Pin 13 is connected to a $5k\Omega$ resistor to ground. Pin 8 is connected to a $5k\Omega$ resistor to ground.
- 562 Outputs:** Pin 14 is connected to a $300k\Omega$ resistor to V_{CC} and a $5k\Omega$ resistor to ground. Pin 7 is connected to a $300k\Omega$ resistor to V_{CC} and a $5k\Omega$ resistor to ground.

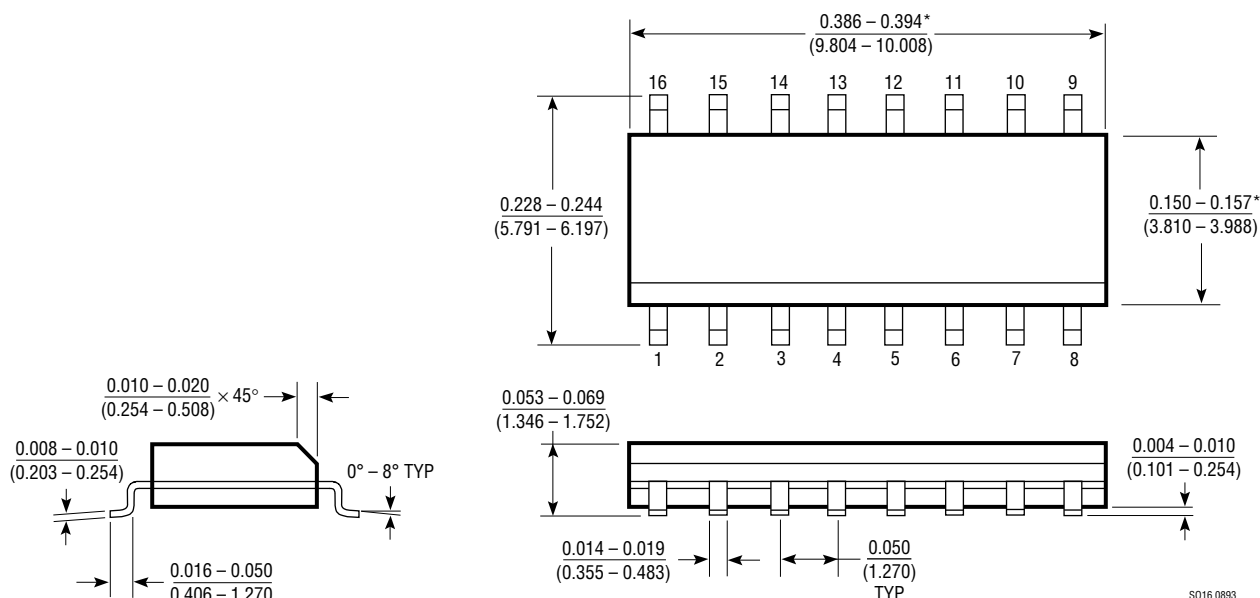
PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N Package 16-Lead Plastic DIP



S Package 16-Lead Plastic SOIC



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

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