High Power Synchronous Switching Regulator Controller

FEATURES

- **High Power Buck Converter from 5V or 3.3V Main Power**
- **Adjustable Current Limit in SO-8 with Topside FET $R_{DS(ON)}$ Sensing**
- **No External Sense Resistor Required**
- Hiccup Mode Current Limit Protection
- Adjustable, Fixed 1.9V, 2.5V, 2.8V and 3.3V Output
- All N-Channel MOSFET Synchronous Driver
- Excellent Output Regulation: ±2% over Line, Load and Temperature Variations
- High Efficiency: Over 95% Possible
- Fast Transient Response
- Fixed 300kHz Frequency Operation
- Internal Soft-Start Circuit
- Quiescent Current: 1mA, 45µA in Shutdown

APPLICATIONS

- Power Supply for Pentium® II, AMD-K6®-2, SPARC, ALPHA and PA-RISC Microprocessors
- High Power 5V to 1.3V-3.5V Regulators

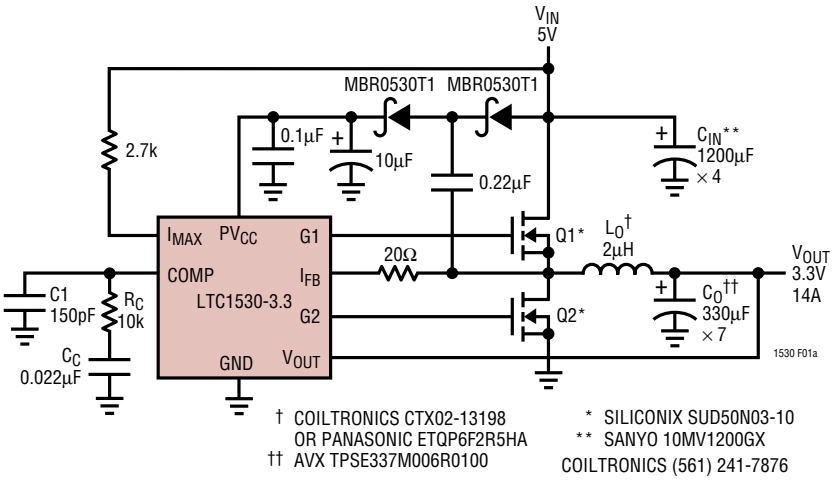
DESCRIPTION

The LTC®1530 is a high power synchronous switching regulator controller optimized for 5V to 1.3V-3.5V output applications. Its synchronous switching architecture drives two external N-channel MOSFET devices to provide high efficiency. The LTC1530 contains a precision trimmed reference and feedback system that provides worst-case output voltage regulation of ±2% over temperature, load current and line voltage shifts. Current limit circuitry senses the output current through the on-resistance of the topside N-channel MOSFET, providing an adjustable current limit without requiring an external low value sense resistor.

The LTC1530 includes a fixed frequency PWM oscillator that free runs at 300kHz, providing greater than 90% efficiency in converter designs from 1A to 20A of output current. Shutdown mode drops the LTC1530 supply current to 45µA.

The LTC1530 is specified for commercial and industrial temperature ranges and is available in the SO-8 package.

TYPICAL APPLICATION



Efficiency vs Load Current

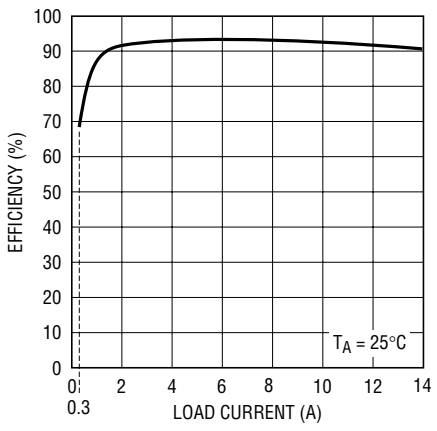


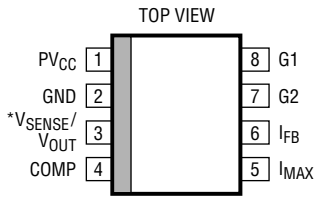
Figure 1. Single 5V to 3.3V Supply

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
PV_{CC} 14V
Input Voltage
I_{FB} (Note 2) ..... PV_{CC} + 0.3V
I_{MAX} ..... –0.3V to 14V
I_{FB} Input Current (Notes 2,3) ..... –100mA
Operating Ambient Temperature Range
LTC1530C ..... 0°C to 70°C
LTC1530I ..... –40°C to 85°C
Maximum Junction Temperature
LTC1530C, LTC1530I ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

*V_{OUT} FOR FIXED VOLTAGE VERSIONS

ORDER PART NUMBER
LTC1530CS8
LTC1530CS8-1.9
LTC1530CS8-2.5
LTC1530CS8-2.8
LTC1530CS8-3.3
LTC1530IS8
LTC1530IS8-1.9
LTC1530IS8-2.5
LTC1530IS8-2.8
LTC1530IS8-3.3

S8 PART MARKING			
1530	153028	1530I	530I28
153019	153033	530I19	530I33
153025		530I25	

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at 0°C ≤ T_A ≤ 70°C. PV_{CC} = 12V unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{SENSE}	Internal Feedback Voltage	LTC1530CS8 (Note 4)		1.223	1.235	1.247	V
			●	1.216	1.235	1.254	V
V_{OUT}	Output Voltage	LTC1530CS8-1.9 (Note 4)		1.881	1.9	1.919	V
			●	1.871	1.9	1.929	V
		LTC1530CS8-2.5 (Note 4)		2.475	2.5	2.525	V
			●	2.462	2.5	2.538	V
		LTC1530CS8-2.8 (Note 4)		2.772	2.8	2.828	V
			●	2.758	2.8	2.842	V
		LTC1530CS8-3.3 (Note 4)		3.267	3.3	3.333	V
			●	3.250	3.3	3.350	V
g_{mERR}	Error Amplifier Transconductance	(Note 5)	●	1.6	2	2.6	millimho

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at –40°C ≤ T_A ≤ 85°C. PV_{CC} = 12V unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PV_{CC}	Supply Voltage	(Note 6)	●			13.2	V
V_{UVLO}	Undervoltage Lockout Voltage	(Note 7)			3.5	3.75	V
V_{SENSE}	Internal Feedback Voltage	LTC1530IS8 (Note 4)		1.223	1.235	1.247	V
			●	1.210	1.235	1.260	V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at –40°C ≤ T_A ≤ 85°C. PV_{CC} = 12V unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	Output Voltage	LTC1530IS8-1.9 (Note 4)	 ●	1.881 1.862	1.9 1.9	1.919 1.938	V V
		LTC1530IS8-2.5 (Note 4)	 ●	2.475 2.450	2.5 2.5	2.525 2.550	V V
		LTC1530IS8-2.8 (Note 4)	 ●	2.772 2.744	2.8 2.8	2.828 2.856	V V
		LTC1530IS8-3.3 (Note 4)	 ●	3.267 3.234	3.3 3.3	3.333 3.366	V V
ΔV_{OUT}	Output Load Regulation	I_{OUT} = 0 to 14A			–5		mV
	Output Line Regulation	V_{IN} = 4.75V to 5.25V, I_{OUT} = 0			±1		mV
I_{PVCC}	Operating Supply Current	Figure 3, V_{FB} = 0V (Note 8)			15		mA
	Quiescent Current	Figure 3, COMP = 0.5V, V_{FB} = 5V	●		1.0	1.4	mA
	Shutdown Supply Current	Figure 3, COMP = 0 (Note 9)	●		45	80	µA
f_{OSC}	Internal Oscillator Frequency	Figure 4	●	250	300	350	kHz
	Oscillator Valley Voltage	V_{COMP} at 0% Duty Cycle			2.5		V
	Oscillator Peak Voltage	V_{COMP} at Max Duty Cycle			3.5		V
G_{ERR}	Error Amplifier Open-Loop DC Gain	(Note 5)	●	40	54		dB
g_{mERR}	Error Amplifier Transconductance	(Note 5)	●	1.6	2	2.8	millimho
I_{MAX}	I_{MAX} Sink Current	V_{IMAX} = 5V V_{IMAX} = 5V	 ●	170 120	200 200	230 300	µA µA
	I_{MAX} Sink Current Tempco	V_{IMAX} = 5V			3300		ppm/°C
V_{SHDN}	Shutdown Threshold Voltage	Figure 4, Measured at COMP Pin (Note 9)	●	100	180		mV
SR_{SS}	Internal Soft-Start Slew Rate	Figure 4, COMP Pulls High, V_{FB} = 0V (Notes 9, 10)			0.4		V/ms
t_{SS}	Internal Soft-Start Wake-Up Time	Figure 4, COMP Pulls High to G1↑ (Note 10)			3.5		ms
t_r, t_f	Driver Rise and Fall Time	Figure 4	●		90	140	ns
t_{NOL}	Driver Nonoverlap Time	Figure 4	●	30	100		ns
DC_{MAX}	Maximum G1 Duty Cycle	Figure 4	●	81	86		%

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: If I_{FB} is taken below GND, it is clamped by an internal diode. This pin handles input currents ≤ 100mA below GND without latch-up. In the positive direction, it is not clamped to PV_{CC}.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: The LTC1530 is tested in an op amp feedback loop which regulates V_{SENSE} or V_{OUT} based on V_{COMP} = 2V for the error amplifier.

Note 5: The Open-loop DC gain and transconductance from the V_{FB} pin to the COMP pin are G_{ERR} and g_{mERR} respectively. For fixed output voltage versions, the actual open-loop DC gain and transconductance are G_{ERR} and g_{mERR} multiplied by the ratio 1.235/V_{OUT}.

Note 6: The total voltage from the PV_{CC} pin to the GND pin must be ≥8V for the current limit protection circuit to be active.

Note 7: G1 and G2 begin to switch once PV_{CC} is ≥ the undervoltage lockout threshold voltage.

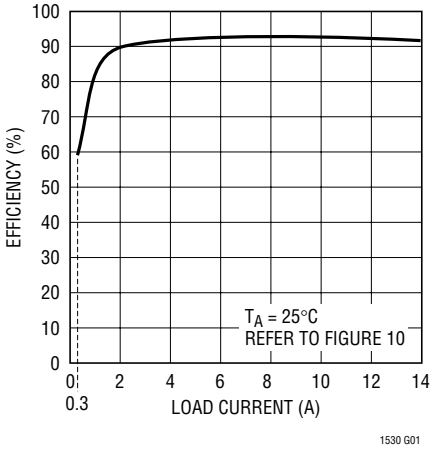
Note 8: Supply current in normal operation is dominated by the current needed to charge and discharge the external FET gates. This current varies with the LTC1530 operating frequency, supply voltage and the external FETs used.

Note 9: The LTC1530 enters shutdown if COMP is pulled low.

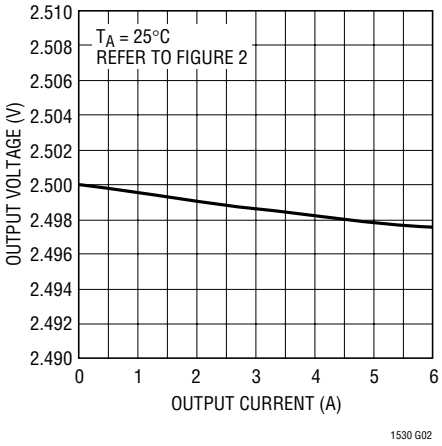
Note 10: Slew rate is measured at the COMP pin on the transition from shutdown to active mode.

TYPICAL PERFORMANCE CHARACTERISTICS

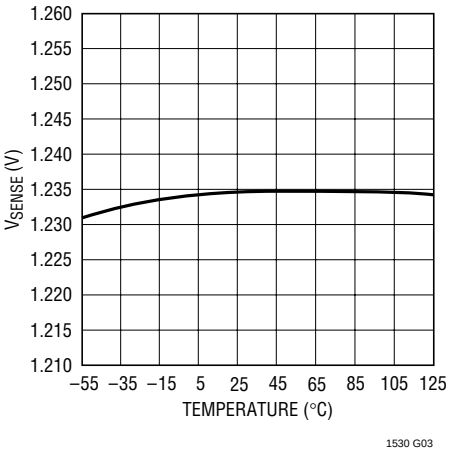
Efficiency vs Load Current



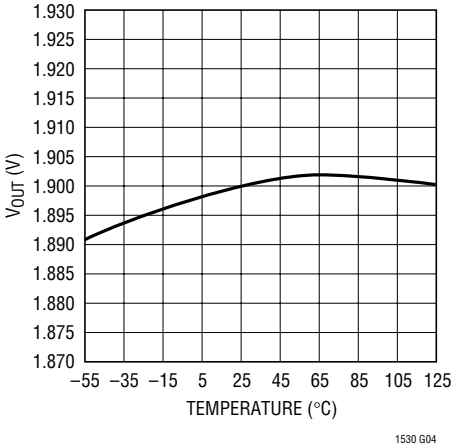
Load Regulation



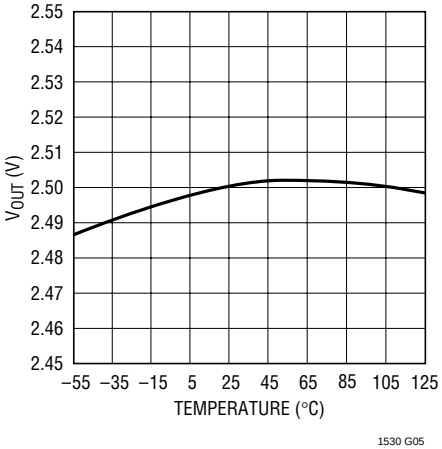
LTC1530 V_{SENSE} vs Temperature



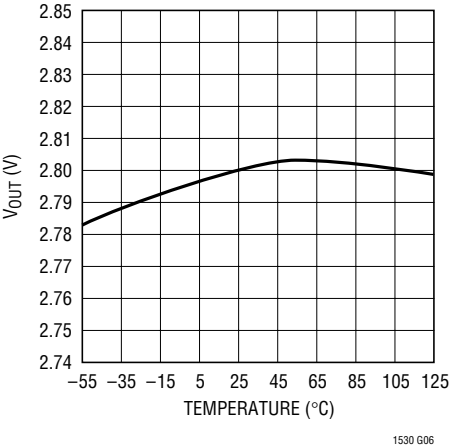
LTC1530-1.9 V_{OUT} vs Temperature



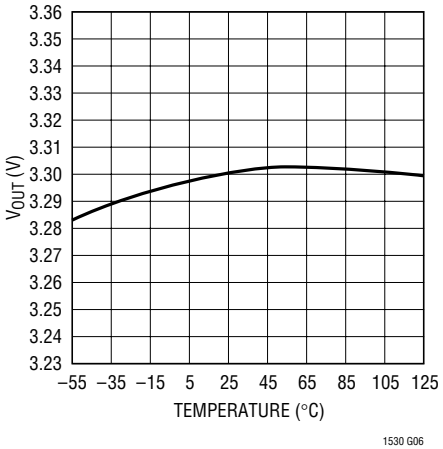
LTC1530-2.5 V_{OUT} vs Temperature



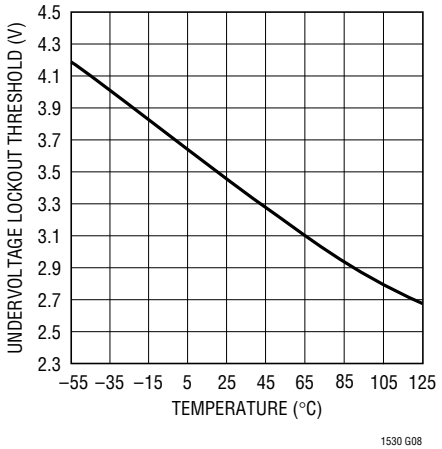
LTC1530-2.8 V_{OUT} vs Temperature



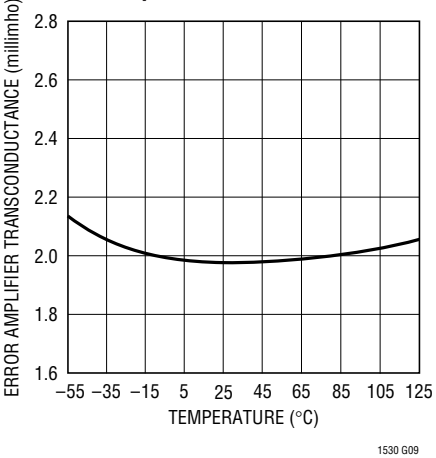
LTC1530-3.3 V_{OUT} vs Temperature



Undervoltage Lockout Threshold Voltage vs Temperature

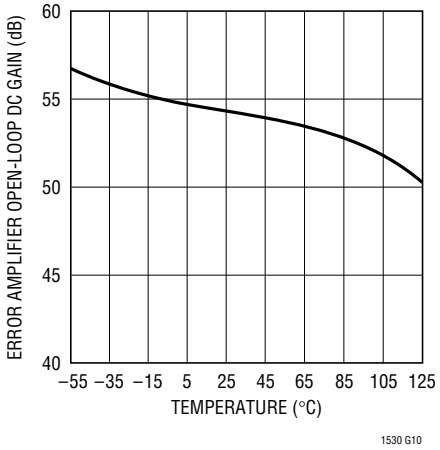


Error Amplifier Transconductance vs Temperature

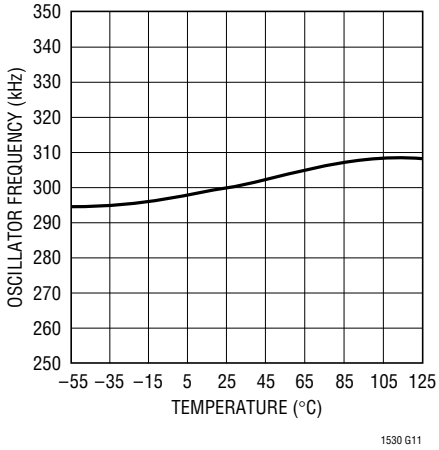


TYPICAL PERFORMANCE CHARACTERISTICS

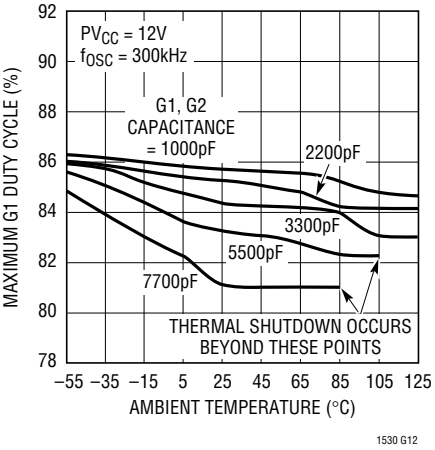
Error Amplifier Open-Loop Gain vs Temperature



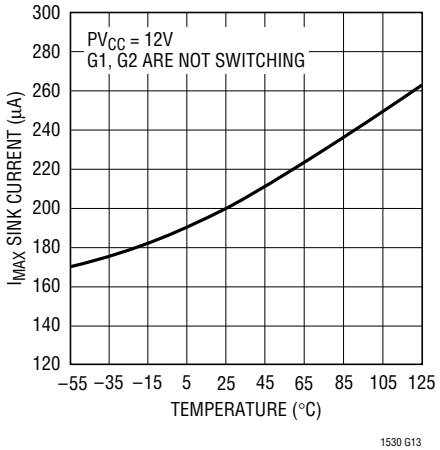
Oscillator Frequency vs Temperature



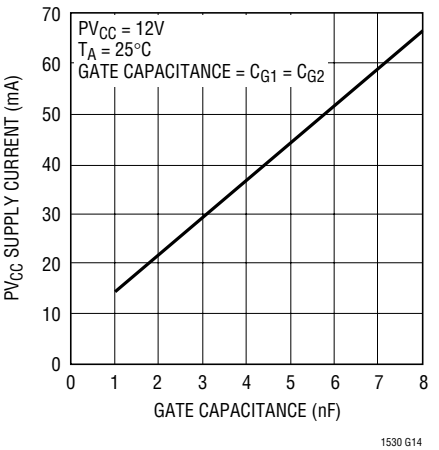
Maximum G1 Duty Cycle vs Ambient Temperature



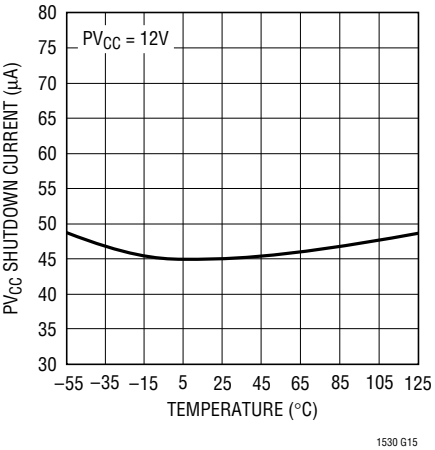
I_{MAX} Sink Current vs Temperature



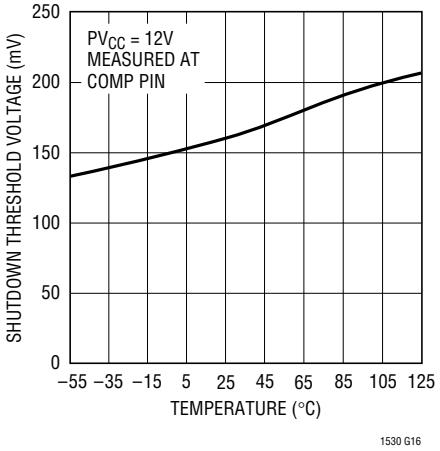
PV_{CC} Supply Current vs Gate Capacitance



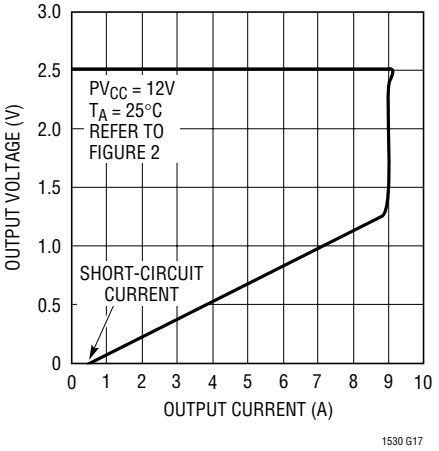
PV_{CC} Shutdown Supply Current vs Temperature



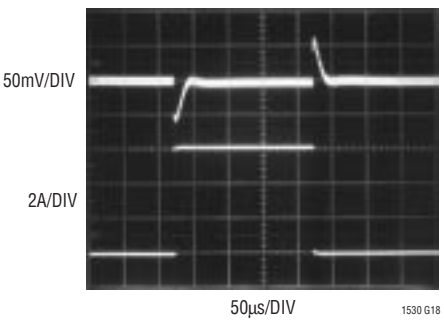
Shutdown Threshold Voltage vs Temperature



Output Overcurrent Protection



Transient Response



PIN FUNCTIONS

PV_{CC} (Pin 1): Power Supply for G1, G2 and Logic. PV_{CC} must connect to a potential of at least $V_{IN} + V_{GS(ON)Q1}$. If V_{IN} = 5V, generate PV_{CC} using a simple charge pump connected to the switching node between Q1 and Q2 (see Figure 1) or connect PV_{CC} to a 12V supply. Bypass PV_{CC} properly or erratic operation will result. A low ESR 10µF capacitor or larger bypass capacitor along with a 0.1µF surface mount ceramic capacitor in parallel is recommended from PV_{CC} directly to GND to minimize switching ripple. Switching ripple should be ≤100mV at the PV_{CC} pin.

GND (Pin 2): Power and Logic Ground. GND is connected to the internal gate drive circuitry and the feedback circuitry. To obtain good output voltage regulation, use proper ground techniques between the LTC1530 GND and bottom-side FET source and the negative terminal of the output capacitor. See the Applications Information section for more details on PCB layout techniques.

V_{SENSE}/V_{OUT} (Pin 3): Feedback Voltage Pin. For the adjustable LTC1530, use an external resistor divider to set the required output voltage. Connect the tap point of the resistor divider network to V_{SENSE} and the top of the divider network to the output voltage. For fixed output voltage versions of the LTC1530, the resistor divider is internal and the top of the resistor divider network is brought out to V_{OUT}. In general, the resistor divider network for each fixed output voltage version sinks approximately 30µA. Connect V_{OUT} to the output voltage either at the output capacitors or at the actual point of load. V_{SENSE}/V_{OUT} is sensitive to switching noise injected into the pin. Isolate high current switching traces from this pin and its PCB trace.

COMP (Pin 4): External Compensation. The COMP pin is connected to the error amplifier output and the input of the PWM comparator. An RC + C network is typically used at COMP to compensate the feedback loop for optimum transient response. To shut down the LTC1530, pull this pin below 0.1V with an open-collector or open-drain transistor. Supply current is typically reduced to 45µA in shutdown. An internal 4µA pullup ensures start-up.

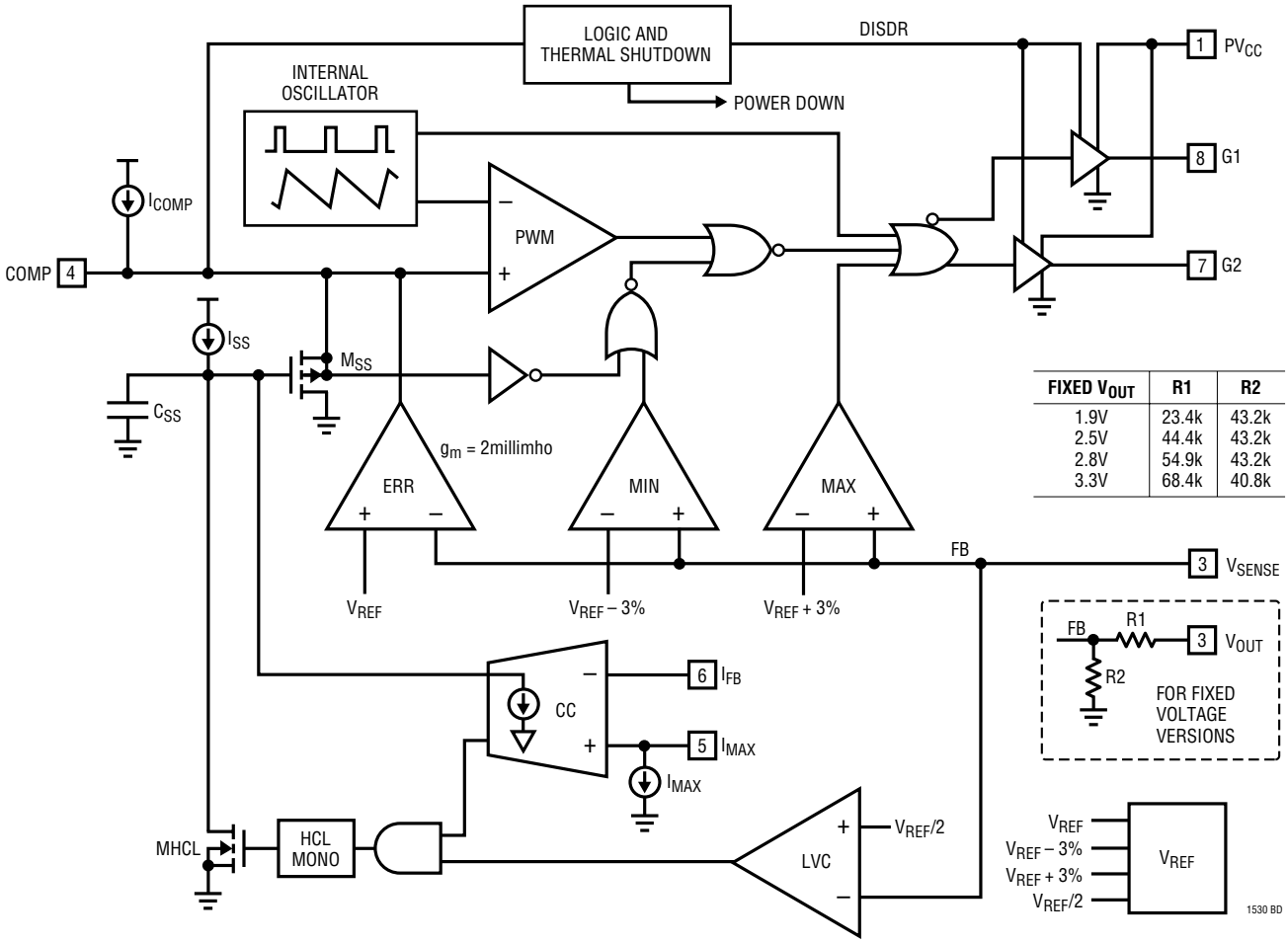
I_{MAX} (Pin 5): Current Limit Threshold. Current limit is set by the voltage drop across an external resistor connected between the drain of Q1 and I_{MAX}. This voltage is compared with the voltage across the $R_{DS(ON)}$ of the high side MOSFET. The LTC1530 contains a 200µA internal pulldown at I_{MAX} to set current limit. This 200µA current source has a positive temperature coefficient to provide first order correction for the temperature coefficient of the external N-channel MOSFET's $R_{DS(ON)}$.

I_{FB} (Pin 6): Current Limit Sense Pin. Connect I_{FB} to the switching node between Q1's source and Q2's drain. If I_{FB} drops below I_{MAX} with G1 on, the LTC1530 enters current limit. Under this condition, the internal soft-start capacitor is discharged and COMP is pulled low slowly. Duty cycle is reduced and output power is limited. The current limit circuitry is only activated if $PV_{CC} \geq 8V$. This action eases start-up considerations as PV_{CC} is ramping up because the MOSFET's $R_{DS(ON)}$ can be significantly higher than what is measured under normal operating conditions. The current limit circuit is disabled by floating I_{MAX} and shorting I_{FB} to PV_{CC}.

G2 (Pin 7): Gate Drive for the Low Side N-Channel MOSFET, Q2. This output swings from PV_{CC} to GND. It is always low if G1 is high or if the output is disabled. To prevent undershoot during a soft-start cycle, G2 is held low until G1 first transitions high.

G1 (Pin 8): Gate Drive for the Topside N-Channel MOSFET, Q1. This output swings from PV_{CC} to GND. It is always low if G2 is high or if the output is disabled.

BLOCK DIAGRAM



FIXED V_{OUT}	R1	R2
1.9V	23.4k	43.2k
2.5V	44.4k	43.2k
2.8V	54.9k	43.2k
3.3V	68.4k	40.8k

TEST CIRCUITS

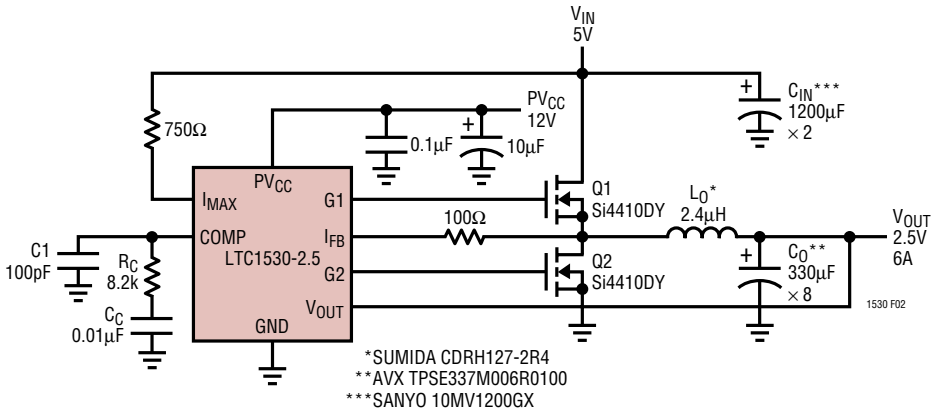


Figure 2

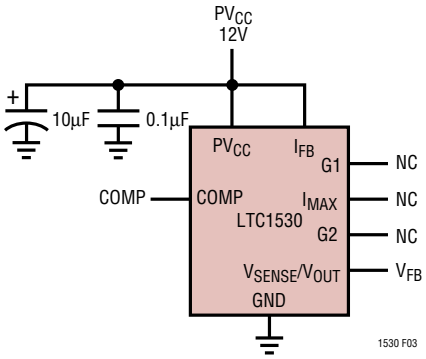


Figure 3

TEST CIRCUITS

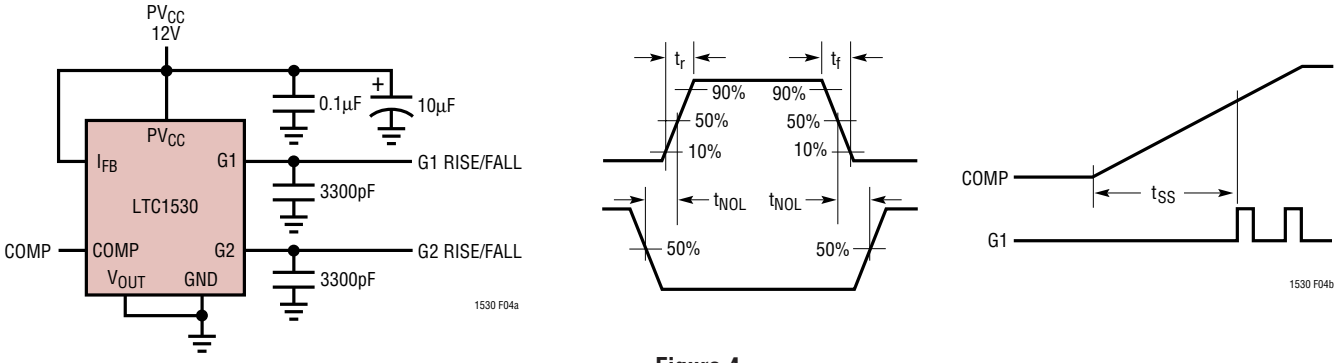


Figure 4

APPLICATIONS INFORMATION

OVERVIEW

The LTC1530 is a voltage feedback, synchronous switching regulator controller (see Block Diagram) designed for use in high power, low voltage step-down (buck) converters. It includes an on-chip soft-start capacitor, a PWM generator, a precision reference trimmed to ±1%, two high power MOSFET gate drivers and all the necessary feedback and control circuitry to form a complete switching regulator circuit running at 300kHz.

The LTC1530 includes a current limit sensing circuit that uses the topside external N-channel power MOSFET as a current sensing element, eliminating the need for an external sense resistor. If the current comparator, CC, detects an overcurrent condition, the duty cycle is reduced by discharging the internal soft-start capacitor through a voltage-controlled current source. Under severe overloads or output short-circuit conditions, the soft-start capacitor is pulled to ground and a start-up cycle is initiated. If the short circuit or overload persists, the chip repeats soft-start cycles and prevents damage to external components.

THEORY OF OPERATION

Primary Feedback Loop

The LTC1530 compares the output voltage with the internal reference at the error amplifier inputs. The error amplifier outputs an error signal to the PWM comparator. This signal is compared to the fixed frequency oscillator sawtooth waveform to generate the PWM signal. The PWM signal drives the external MOSFETs at the G1 and G2 pins. The resulting chopped waveform is filtered by L_O and C_{OUT} which closes the loop. Loop frequency compensation is typically accomplished with an external RC + C network at the COMP pin, which is the output node of the transconductance error amplifier.

MIN, MAX Feedback Loops

Two additional comparators in the feedback loop provide high speed fault correction in situations where the error amplifier cannot respond quickly enough. MIN compares the feedback signal to a voltage 3% below the internal reference. If the signal is below the comparator threshold, the MIN comparator overrides the error amplifier and forces the loop to maximum duty cycle, typically 86%. Similarly, the MAX comparator forces the output to 0% duty cycle if the feedback signal is greater than 3% above the internal reference. To prevent these two comparators from triggering due to noise, the MIN and MAX comparators' response times are deliberately delayed by two to three microseconds. These comparators help prevent extreme output perturbations with fast output load current transients, while allowing the main feedback loop to be optimally compensated for stability.

Thermal Shutdown

The LTC1530 has a thermal protection circuit that disables both internal gate drivers if activated. G1 and G2 are held low and the LTC1530 supply current drops to about 1mA.

APPLICATIONS INFORMATION

Typically, thermal shutdown is activated if the LTC1530's junction temperature exceeds 150°C. G1 and G2 resume switching when the junction temperature drops below 100°C.

Soft-Start and Current Limit

Unlike other PWM parts, the LTC1530 includes an on-chip soft-start capacitor that is used during start-up and current limit operation. On power-up, an internal 4μA pull-up at COMP brings the LTC1530 out of shutdown mode. An internal current source then charges the internal C_{SS} capacitor. The COMP pin is clamped to one V_{GS} above the voltage on C_{SS} during start-up. This prevents the error amplifier from forcing the loop to maximum duty cycle. The LTC1530 operates at low duty cycle as the COMP pin voltage increases above about 2.4V. The slew rate of the soft-start capacitor is typically 0.4V/ms. As the voltage on C_{SS} continues to increase, M_{SS} eventually turns off and the error amplifier regulates the output. The MIN comparator is disabled if soft-start is active to prevent an override of the soft-start function.

The LTC1530 includes another feedback loop to control operation in current limit. Before each falling edge of G1, the current comparator, CC, samples and holds the voltage drop across external MOSFET Q1 with the LTC1530's I_{FB} pin. CC compares the voltage at I_{FB} to the voltage at the I_{MAX} pin. As peak current rises, the voltage across the $R_{DS(ON)}$ of Q1 increases. If the voltage at I_{FB} drops below I_{MAX}, indicating that Q1's drain current has exceeded the maximum desired level, CC pulls current out of C_{SS}. Duty cycle decreases and the output current is controlled. The CC comparator pulls current out of C_{SS} in proportion to the voltage difference between I_{FB} and I_{MAX}. Under minor overload conditions, the voltage at C_{SS} falls gradually, creating a time delay before current limit activates. Very short, mild overloads may not affect the output voltage at all. Significant overload conditions allow the voltage on C_{SS} to reach a steady state and the output remains at a reduced voltage until the overload is removed. Serious overloads generate a large overdrive and allow CC to pull the C_{SS} voltage down quickly, thus preventing damage to the external components.

By using the $R_{DS(ON)}$ of Q1 to measure output current, the current limit circuit eliminates the sense resistor that would otherwise be required. This minimizes the number of components in the high current power path. The current limit circuitry is not designed to be highly accurate. It is primarily meant to prevent damage to the power supply circuitry during fault conditions. The exact current level where current limiting takes effect will vary from unit to unit as the $R_{DS(ON)}$ of Q1 varies.

Figure 5a illustrates the basic connections for the current limit circuitry. For a given current limit level, the external resistor from I_{MAX} to V_{IN} is determined by:

$$R_{IMAX} = \frac{(I_{LMAX})R_{DS(ON)Q1}}{I_{IMAX}}$$

where,

$$I_{LMAX} = I_{LOAD} + \frac{I_{RIPPLE}}{2}$$

I_{LOAD} = Maximum load current

I_{RIPPLE} = Inductor ripple current

$$= \frac{(V_{IN} - V_{OUT})(V_{OUT})}{(f_{OSC})(L_O)(V_{IN})}$$

f_{OSC} = LTC1530 oscillator frequency = 300kHz

L_O = Inductor value

$R_{DS(ON)Q1}$ = On-resistance of Q1 at I_{LMAX}

I_{IMAX} = 200μA sink current

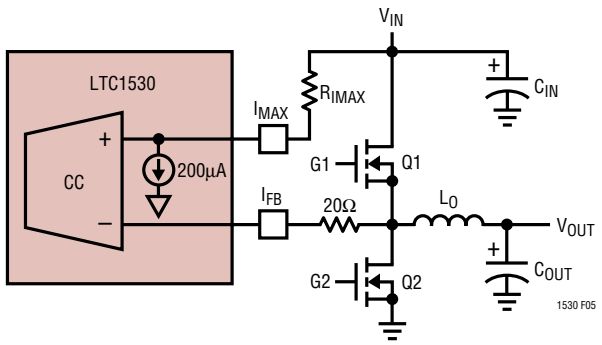


Figure 5a. Current Limit Setting (Use Kelvin-Sense Connections Directly at the Drain and Source of Q1)

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Figure 5b is derived based on the condition that $I_{LMAX} = I_{LOAD} + I_{RIPPLE}/2$. Therefore, it only provides the minimum R_{IMAX} value. It must be understood that during the initial power-up phase (V_{OUT} = 0V), the initial start-up I_{LMAX} can be much higher than the steady state condition I_{LMAX}. Therefore, R_{IMAX} must be selected with the start-up I_{LMAX} in mind. In general, high output capacitance combined with a low value inductor increases the start-up I_{LMAX}. Figures 6a and 6b plot the start-up I_{LMAX} vs output capacitance and inductance for unloaded and loaded conditions with the current limit circuit disabled. Figures 6a and 6b are provided as examples. Actual I_{LMAX} under start-up conditions must be measured for any application circuit so that R_{IMAX} can be properly chosen.

In order for the current limit circuit to operate properly and to obtain a reasonably accurate current limit threshold, the I_{MAX} and I_{FB} pins must be Kelvin sensed at Q1's drain and source pins. A 0.1µF decoupling capacitor can also be connected across R_{IMAX} to filter switching noise. In addition, LTC recommends that the voltage drop across the R_{IMAX} resistor be set to ≥100mV. Otherwise, noise spikes or ringing at Q1's source can cause the actual current limit to be greater than the desired current limit set point.

MOSFET Gate Drive

The PV_{CC} supply must be greater than the input supply voltage, V_{IN}, by at least one power MOSFET $V_{GS(ON)}$ for efficient operation. This higher voltage can be supplied with a separate supply, or it can be generated using a simple charge pump as shown in Figure 7. The 86% maximum duty cycle ensures sufficient off-time to refresh the charge pump during each cycle.

As PV_{CC} is powered up from 0V, the LTC1530 undervoltage lockout circuit prevents G1 and G2 from pulling high until PV_{CC} reaches about 3.5V. To prevent Q1's high $R_{DS(ON)}$ from triggering the current limit comparator while PV_{CC} is slewing, the current limit circuit is disabled until PV_{CC} is ≥8V. In addition, on start-up or recovery from thermal shutdown, the driver logic is designed to hold G2 low until G1 first goes high.

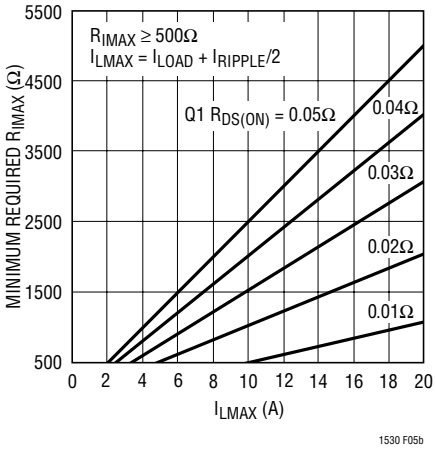

Figure 5b. Minimum Required R_{IMAX} vs I_{LMAX}

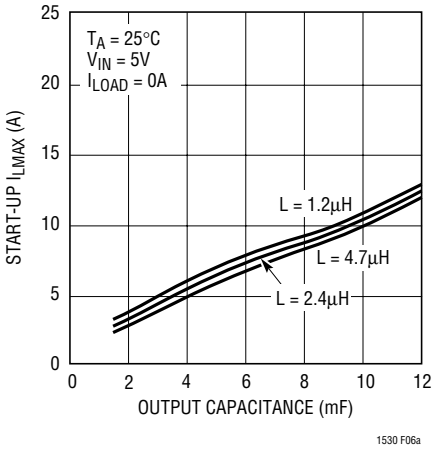

Figure 6a. Start-Up I_{LMAX} vs Output Capacitance

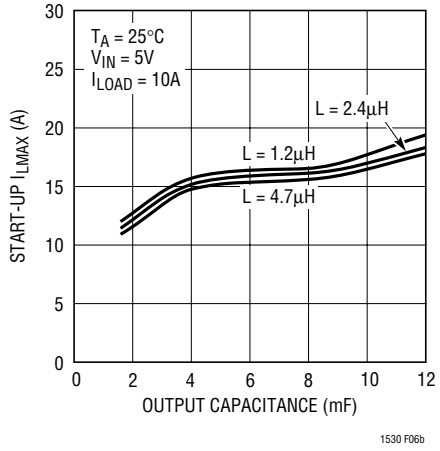

Figure 6b. Start-Up I_{LMAX} vs Output Capacitance

APPLICATIONS INFORMATION

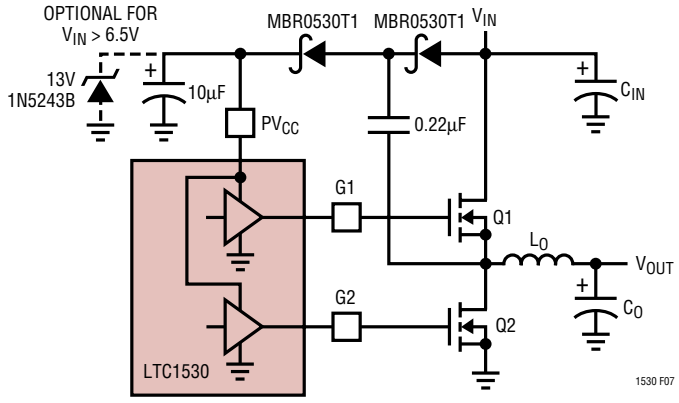

Figure 7. Doubling Charge Pump

Power MOSFETs

Two N-channel power MOSFETs are required for synchronous LTC1530 circuits. They should be selected based primarily on threshold voltage and on-resistance considerations. Thermal dissipation is often a secondary concern in high efficiency designs. The required MOSFET threshold should be determined based on the available power supply voltages and/or the complexity of the gate drive charge pump scheme. In 5V input designs where a 12V supply is used to power PV_{CC}, standard MOSFETs with $R_{DS(ON)}$ specified at V_{GS} = 5V or 6V can be used with good results. The current drawn from the 12V supply varies with the MOSFETs used and the LTC1530's operating frequency, but is generally less than 50mA.

LTC1530 applications that use a 5V V_{IN} voltage and a doubling charge pump to generate PV_{CC} do not provide enough gate drive voltage to fully enhance standard power MOSFETs. Under this condition, the effective MOSFET $R_{DS(ON)}$ may be quite high, raising the dissipation in the FETs and reducing efficiency. In addition, power supply start-up problems can occur with standard power MOSFETs. These start-up problems can occur for two reasons. First, if the MOSFET is not fully enhanced, the higher effective $R_{DS(ON)}$ causes the LTC1530 to activate current limit at a much lower level than the desired trip point. Second, standard MOSFETs have higher GATE threshold voltages than logic level MOSFETs, thereby increasing the PV_{CC} voltage required to turn them on. A MOSFET whose $R_{DS(ON)}$ is rated at V_{GS} = 4.5V does not necessarily have a logic level MOSFET GATE threshold voltage. Logic level FETs are the recommended choice for 5V-only systems. Logic level FETs can be fully enhanced with a doubler charge pump and will operate at maximum efficiency. Note that doubler charge pump designs running from supplies higher than 6.5V should include a Zener diode clamp at PV_{CC} to prevent transients from exceeding the absolute maximum rating of the pin.

After the MOSFET threshold voltage is selected, choose the $R_{DS(ON)}$ based on the input voltage, the output voltage, allowable power dissipation and maximum output current. In a typical LTC1530 buck converter circuit, operating in continuous mode, the average inductor current is equal to the output load current. This current flows through either Q1 or Q2 with the power dissipation split up according to the duty cycle:

$$DC(Q1) = \frac{V_{OUT}}{V_{IN}}$$

$$DC(Q2) = 1 - \frac{V_{OUT}}{V_{IN}} = \frac{(V_{IN} - V_{OUT})}{V_{IN}}$$

The $R_{DS(ON)}$ required for a given conduction loss can now be calculated by rearranging the relation $P = I^2R$.

$$R_{DS(ON)Q1} = \frac{P_{MAX(Q1)}}{[DC(Q1)](I_{MAX}^2)} = \frac{(V_{IN})[P_{MAX(Q1)}]}{(V_{OUT})(I_{MAX}^2)}$$

$$R_{DS(ON)Q2} = \frac{P_{MAX(Q2)}}{[DC(Q2)](I_{MAX}^2)} = \frac{(V_{IN})[P_{MAX(Q2)}]}{(V_{IN} - V_{OUT})(I_{MAX}^2)}$$

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P_{MAX} should be calculated based primarily on required efficiency or allowable thermal dissipation. A high efficiency buck converter designed for the Pentium II with 5V input and a 2.8V, 11.2A output might allow no more than 4% efficiency loss at full load for each MOSFET. Assuming roughly 90% efficiency at this current level, this gives a P_{MAX} value of:

(2.8)(11.2A/0.9)(0.04) = 1.39W per FET

and a required $R_{DS(ON)}$ of:

$$R_{DS(ON)Q1} = \frac{5V(1.39W)}{2.8V(11.2A^2)} = 0.020\Omega$$

$$R_{DS(ON)Q2} = \frac{5V(1.39W)}{(5V - 2.8V)(11.2A^2)} = 0.025\Omega$$

Note that while the required $R_{DS(ON)}$ values suggest large MOSFETs, the power dissipation numbers are only 1.39W per device or less—large TO-220 packages and heat sinks are not necessarily required in high efficiency applications. Siliconix Si4410DY or International Rectifier IRF7413 (both in SO-8) or Siliconix SUD50N03 or Motorola MTD20N03HDL (both in DPAK) are small footprint surface mount devices with $R_{DS(ON)}$ values below 0.03Ω at 5V of V_{GS} that work well in LTC1530 circuits. With higher output voltages, the $R_{DS(ON)}$ of Q1 may need to be significantly lower than that for Q2. These conditions can often be met by paralleling two MOSFETs for Q1 and using a single device for Q2. Using a higher P_{MAX} value in the $R_{DS(ON)}$ calculations generally decreases the MOSFET cost and the circuit efficiency and increases the MOSFET heat sink requirements.

In most LTC1530 applications, $R_{DS(ON)}$ is used as the current sensing element. MOSFET $R_{DS(ON)}$ has a positive temperature coefficient. Therefore, the LTC1530 I_{MAX} sink current is designed with a positive 3300ppm/°C temperature coefficient. The positive tempco of I_{MAX} provides first order correction for current limit vs temperature. Therefore, current limit does not have to be set to an increased level at room temperature to guarantee a desired output current at elevated temperatures.

Table 1 highlights a variety of power MOSFETs that are suitable for use in LTC1530 applications.

Table 1. Recommended MOSFETs for LTC1530 Applications

MANUFACTURER	PART NO.	PACKAGE	RDS(ON) AT 25°C (Ω)	RATED CURRENT (A)	TYPICAL INPUT CAPACITANCE Ciss (pF)	θ_{JC} (°C/W)	T_{JMAX} (°C)
Siliconix	SUD50N03-10	TO-252	0.019	15A at 25°C 10A at 100°C	3200	1.8	175
Siliconix	Si4410DY	SO-8	0.020	10A at 25°C 8A at 75°C	2700	—	150
ON Semiconductor	MTD20N03HDL	DPAK	0.035	20A at 25°C 16A at 100°C	880	1.67	150
Fairchild	FDS6680	SO-8	0.01	11.5A at 25°C	2070	25	150
ON Semiconductor	MTB75N03HDL*	D^2PAK	0.0075	75A at 25°C 59A at 100°C	4025	1.0	150
IR	IRL3103S	D^2PAK	0.014	56A at 25°C 40A at 100°C	1600	1.8	175
IR	IRLZ44	TO-220	0.028	50A at 25°C 36A at 100°C	3300	1.0	175
Fuji	2SK1388	TO-220	0.037	35A at 25°C	1750	2.08	150

Note: Please refer to the manufacturer's data sheet for testing conditions and detailed information.
*Users must consider the power dissipation and thermal effects in the LTC1530 if driving external MOSFETs with high values of input capacitance. Refer to the PV_{CC} Supply Current vs GATE Capacitance in the Typical Performance Characteristics section.

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Inductor Selection

The inductor is often the largest component in an LTC1530 design and must be chosen carefully. Choose the inductor value and type based on output slew rate requirements and expected peak current. The required output slew rate primarily controls the inductor value. The maximum rate of rise of inductor current is set by the inductor's value, the input-to-output voltage differential and the LTC1530's maximum duty cycle. In a typical 5V input, 2.8V output application, the maximum rise time will be:

$$DC_{MAX}\left(\frac{V_{IN}-V_{OUT}}{L}\right)=\frac{1.85}{L}\quad\frac{A}{\mu s}$$

where L is the inductor value in µH. With proper frequency compensation, the combination of the inductor and output capacitor values determine the transient recovery time. In general, a smaller value inductor improves transient response at the expense of ripple and inductor core saturation rating. A 2µH inductor has a 0.9A/µs rise time in this application, resulting in a 5.5µs delay in responding to a 5A load current step. During this 5.5µs, the difference between the inductor current and the output current is made up by the output capacitor. This action causes a temporary voltage droop at the output. To minimize this effect, the inductor value should usually be in the 1µH to 5µH range for most 5V input LTC1530 circuits. Different combinations of input and output voltages and expected loads may require different values.

Once the required inductor value is selected, choose the inductor core type based on peak current and efficiency requirements. Peak current in the inductor is equal to the maximum output load current plus half of the peak-to-peak inductor ripple current. Inductor ripple current is set by the inductor's value, the input voltage, the output voltage and the operating frequency. If the efficiency is high, ripple current is approximately equal to:

$$I_{RIPPLE}=\frac{\left(V_{IN}-V_{OUT}\right)\left(V_{OUT}\right)}{\left(f_{OSC}\right)\left(L_O\right)\left(V_{IN}\right)}$$

where
f_{OSC} = LTC1530 oscillator frequency
L_O = Inductor value

Solving this equation for a typical 5V to 2.8V application with a 2µH inductor, ripple current is:

$$\frac{\left(2.2V\right)\left(0.56\right)}{\left(300kHz\right)\left(2\mu H\right)}=2A_{P-P}$$

Peak inductor current at 11.2A load:

$$11.2A+\frac{2A}{2}=12.2A$$

The ripple current should generally fall between 10% and 40% of the output current. The inductor must be able to withstand this peak current without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss. Note that in circuits not employing the current limit function, the current in the inductor may rise above this maximum under short circuit or fault conditions; the inductor should be sized accordingly to withstand this additional current. Inductors with gradual saturation characteristics (example: powdered iron) are often the best choice.

Input and Output Capacitors

A typical LTC1530 design places significant demands on both the input and the output capacitors. During normal steady load operation, a buck converter like the LTC1530 draws square waves of current from the input supply at the switching frequency. The peak current value is equal to the output load current plus 1/2 the peak-to-peak ripple current. Most of this current is supplied by the input bypass capacitor. The resulting RMS current flow in the input capacitor heats it and causes premature capacitor failure in extreme cases. Maximum RMS current occurs with 50% PWM duty cycle, giving an RMS current value equal to $I_{OUT}/2$. A low ESR input capacitor with an adequate ripple current rating must be used to ensure reliable operation. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours (3 months) lifetime at rated temperature. Further derating of the input capacitor ripple current beyond the manufacturer's specification is recommended to extend the useful life of the circuit. Lower operating temperature has the largest effect on capacitor longevity.

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The output capacitor in a buck converter under steady state conditions sees much less ripple current than the input capacitor. Peak-to-peak current is equal to inductor ripple current, usually 10% to 40% of the total load current. Output capacitor duty places a premium not on power dissipation but on ESR. During an output load transient, the output capacitor must supply all of the additional load current demanded by the load until the LTC1530 adjusts the inductor current to the new value. ESR in the output capacitor results in a step in the output voltage equal to the ESR value multiplied by the change in load current. An 11A load step with a 0.05Ω ESR output capacitor results in a 550mV output voltage shift; this is 19.6% of the output voltage for a 2.8V supply! Because of the strong relationship between output capacitor ESR and output load transient response, choose the output capacitor for ESR, not for capacitance value. A capacitor with suitable ESR will usually have a larger capacitance value than is needed to control steady-state output ripple.

Electrolytic capacitors rated for use in switching power supplies with specified ripple current ratings and ESR can be used effectively in LTC1530 applications. OS-CON electrolytic capacitors from Sanyo and other manufacturers give excellent performance and have a very high performance/size ratio for electrolytic capacitors. Surface mount applications can use either electrolytic or dry tantalum capacitors. Tantalum capacitors must be surge tested and specified for use in switching power supplies. Low cost, generic tantalums are known to have very short lives followed by explosive deaths in switching power supply applications. AVX TPS series surface mount devices are popular surge tested tantalum capacitors that work well in LTC1530 applications.

A common way to lower ESR and raise ripple current capability is to parallel several capacitors. A typical LTC1530 application might exhibit 5A input ripple current. Sanyo OS-CON capacitors, part number 10SA220M (220µF/10V), feature 2.3A allowable ripple current at 85°C; three in parallel at the input (to withstand the input ripple current) meet the above requirements. Similarly, AVX TPSE337M006R0100 (330µF/6V) capacitors have a rated maximum ESR of 0.1Ω; seven in parallel lower the net output capacitor ESR to 0.014Ω. For low cost applications, the Sanyo MV-GX capacitor series can be used with acceptable performance.

Feedback Loop Compensation

The LTC1530 voltage feedback loop is compensated at the COMP pin, which is the output node of the g_m error amplifier. The feedback loop is generally compensated with an RC + C network from COMP to GND as shown in Figure 8a.

Loop stability is affected by the values of the inductor, the output capacitor, the output capacitor ESR, the error amplifier transconductance and the error amplifier compensation network. The inductor and the output capacitor create a double pole at the frequency:

$$f_{LC} = \frac{1}{2\pi\sqrt{L_O\left(C_{OUT}\right)}}$$

The ESR of the output capacitor and the output capacitor value form a zero at the frequency:

$$f_{ESR} = \frac{1}{\left(2\pi\right)\left(ESR\right)\left(C_{OUT}\right)}$$

The compensation network used with the error amplifier must provide enough phase margin at the 0dB crossover frequency for the overall open-loop transfer function. The zero and pole from the compensation network are:

$$f_Z = \frac{1}{\left(2\pi\right)\left(R_C\right)\left(C_C\right)} \quad \text{and} \quad f_P = \frac{1}{\left(2\pi\right)\left(R_C\right)\left(C1\right)}$$

respectively. Figure 8b shows the Bode plot of the overall transfer function.

The compensation values used in this design are based on the following criteria, $f_{SW} = 12f_{CO}$, $f_Z = f_{LC}$, $f_P = 5f_{CO}$. At the closed-loop frequency f_{CO}, the attenuation due to the LC filter and the input resistor divider is compensated by the gain of the PWM modulator and the gain of the error amplifier $(g_{mERR})(R_C)$.

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Although a mathematical approach to frequency compensation can be used, the added complication of input and/or output filters, unknown capacitor ESR, and gross operating point changes with input voltage, load current variations and frequency of operation all suggest a more practical empirical method. This can be done by injecting a transient current at the load and using an RC network box to iterate toward the final compensation values or by obtaining the optimum loop response using a network analyzer to find the actual loop poles and zeros.

Table 2 shows the suggested compensation components for 5V input applications based on the inductor and output capacitor values. The values were calculated using multiple paralleled 330µF AVX TPS series surface mount tantalum capacitors for the output capacitor. The optimum component values might deviate from the suggested values slightly because of board layout and operating condition differences.

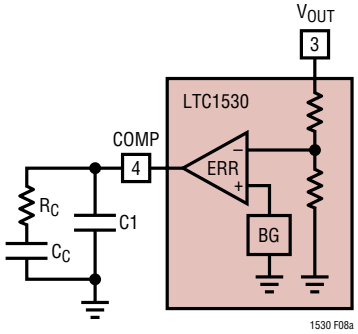

Figure 8a. Compensation Pin Hook-Up

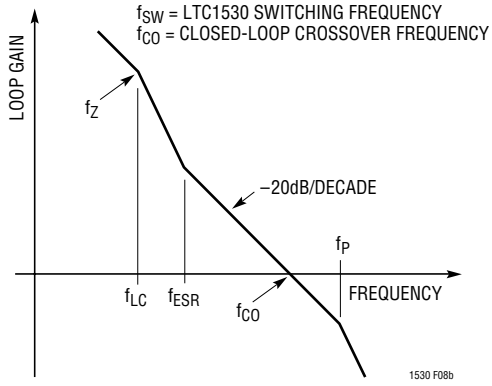

Figure 8b. Bode Plot of the LTC1530 Overall Transfer Function

Table 2. Suggested Compensation Network for a 5V Input Application Using Multiple Paralleled 330µF AVX TPS Output Capacitors for 2.5V Output

L_O (µH)	C_O (µF)	R_C (kΩ)	C_C (µF)	C1 (pF)
1	990	1.3	0.022	1000
1	1980	2.7	0.022	470
1	4950	6.8	0.01	220
2.7	990	3.6	0.022	330
2.7	1980	7.5	0.01	220
2.7	4950	18	0.01	68
5.6	990	7.5	0.01	220
5.6	1980	15	0.01	100
5.6	4950	36	0.0047	47

An alternate output capacitor is the Sanyo MV-GX series. Using multiple paralleled 1500µF Sanyo MV-GX capacitors for the output capacitor, Table 3 shows the suggested compensation components for 5V input applications based on the inductor and output capacitor values.

Table 3. Suggested Compensation Network for a 5V Input Application Using Multiple Paralleled 1500µF SANYO MV-GX Output Capacitors for 2.5V Output

L_O (µH)	C_O (µF)	R_C (kΩ)	C_C (µF)	C1 (pF)
1	4500	3	0.022	470
1	6000	4	0.022	330
1	9000	6	0.022	220
2.7	4500	8.2	0.022	150
2.7	6000	11	0.01	100
2.7	9000	16	0.01	100
5.6	4500	16	0.01	100
5.6	6000	22	0.01	68
5.6	9000	33	0.01	47

Note: For different values of V_{OUT}, multiply the R_C value by $V_{OUT}/2.5$ and multiply the C_C and C1 values by $2.5/V_{OUT}$. This maintains the same crossover frequency for the closed-loop transfer function.

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Thermal Considerations

Limit the LTC1530's junction temperature to less than 125°C. The LTC1530's SO-8 package is rated at 130°C/W and care must be taken to ensure that the worst-case input voltage and gate drive load current requirements do not cause excessive die temperatures. Short-circuit or fault conditions may activate the internal thermal shutdown circuit.

LAYOUT CONSIDERATIONS

When laying out the printed circuit board (PCB), the following checklist should be used to ensure proper operation of the LTC1530. These items are illustrated graphically in the layout diagram of Figure 9. The thicker lines show the high current power paths. Note that at 10A current levels or above, current density in the PCB itself is a serious concern. Traces carrying high current should be as wide as possible. For example, a PCB fabricated with 2oz copper requires a minimum trace width of 0.15" to carry 10A, and only if trace length is kept short.

1. In general, begin the layout with the location of the power devices. Orient the power circuitry so that a clean power flow path is achieved. Maximize conductor widths but minimize conductor lengths. Keep high current connections on one side of the PCB if possible. If not, minimize the use of vias and keep the current density in the vias to <1A/via, preferably < 0.5A/via. After achieving a satisfactory power path layout, proceed with the control circuitry layout. It is much easier to find routes for the relatively small traces in the control circuits than it is to find circuitous routes for high current paths.
2. Tie the GND pin to the ground plane at a single point, preferably at a fairly quiet point in the circuit, such as the bottom of the output capacitors. However, this is not always practical due to physical constraints. Connect the low side source to the input capacitor ground. Connect the input and output capacitor to the ground plane. Run a separate trace for the low side FET source to the input capacitors. Do not tie this single point ground in the trace run between the low side FET source and the input capacitor ground. This area of the ground plane is very noisy.
3. Locate the small signal resistor and capacitors used for frequency compensation close to the COMP pin. Use a separate ground trace for these components that ties directly to the GND pin of the LTC1530. Do not connect these components to the ground plane!
4. Place the PV_{CC} decoupling capacitor as close to the LTC1530 as possible. The 10µF bypass capacitor shown at PV_{CC} helps provide optimum regulation performance by minimizing ripple at the PV_{CC} pin.
5. Connect the (+) plate of C_{IN} as close as possible to the drain of the upper MOSFET. LTC recommends an additional 1µF low ESR ceramic capacitor between V_{IN} and power ground.
6. The V_{SENSE}/V_{OUT} pin is very sensitive to pickup from the switching node. Care must be taken to isolate this pin from capacitive coupling to the high current inductor switching signals. A 0.1µF is recommended between the V_{OUT} pin and the GND pin directly at the LTC1530 for fixed voltage versions. For the adjustable voltage version, keep the resistor divider close to the LTC1530. The bottom resistor's ground connection should tie directly to the LTC1530's GND pin.
7. Kelvin sense I_{MAX} and I_{FB} at the drain and source pins of Q1.
8. Minimize the length of the gate lead connections.

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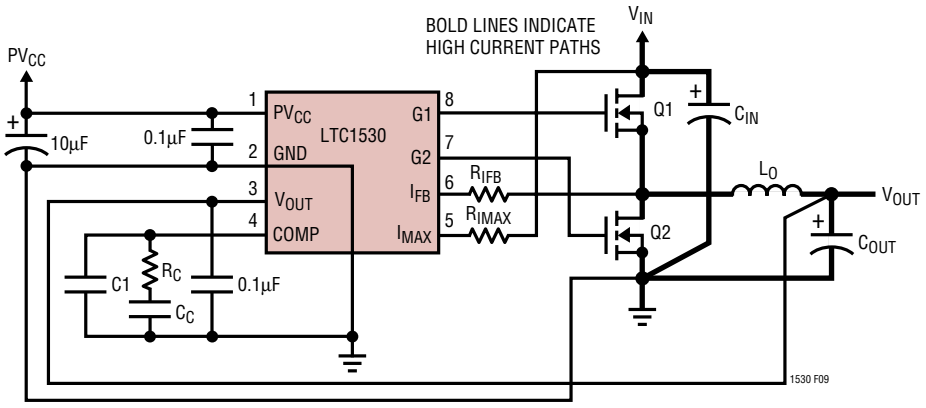
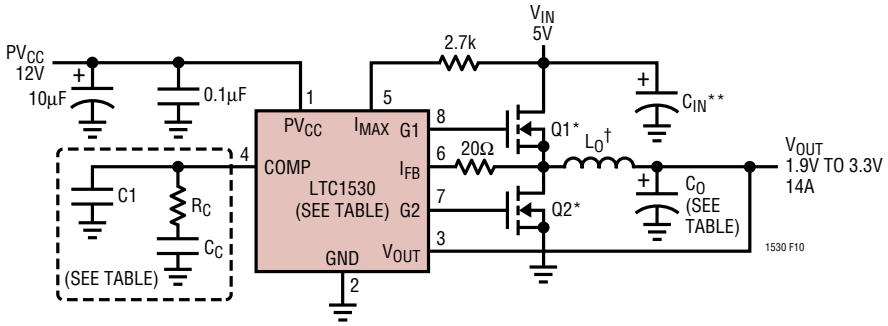


Figure 9. LTC1530 Layout Diagram



* SILICONIX SUD50N03-10
** 3× SANYO 10MV1200GX OR
3× SANYO OS-CON 6SH330K

† COILTRONICS CTX02-13198 (2µH) OR
PANASONIC ETQP6F2R5HA PCC-N6 (2.5µH)

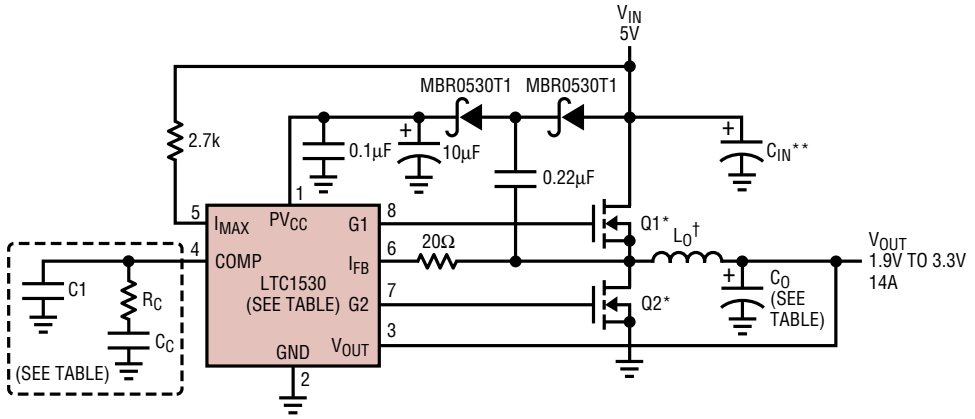
DEVICE	OUTPUT CAPACITOR (C_O)	R_C	C_C	C1
LTC1530-3.3	7 X330µF AVX TPSE337M006R0100	10k	0.022µF	150pF
LTC1530-3.3	4 X1500µF SANYO 6MV1500GX	15k	0.022µF	100pF
LTC1530-2.8	7 X330µF AVX TPSE337M006R0100	8.6k	0.022µF	150pF
LTC1530-2.8	4 X1500µF SANYO 6MV1500GX	13k	0.022µF	100pF
LTC1530-2.5	7 X330µF AVX TPSE337M006R0100	7.5k	0.022µF	220pF
LTC1530-2.5	4 X1500µF SANYO 6MV1500GX	11k	0.022µF	120pF
LTC1530-1.9	7 X330µF AVX TPSE337M006R0100	5.6k	0.033µF	220pF
LTC1530-1.9	4 X1500µF SANYO 6MV1500GX	8.2k	0.022µF	220pF

1530 TA TBL

Figure 10. 5V to 1.9V-3.3V Synchronous Buck Converter PV_{CC} Is Powered from 12V Supply

TYPICAL APPLICATIONS

5V to 1.9V-3.3V Synchronous Buck Converter
PV_{CC} Is Generated from Charge Pump



* SILICONIX SUD50N03-10
** 3× SANYO 10MV1200GX OR
3× SANYO OS-CON 6SH330K

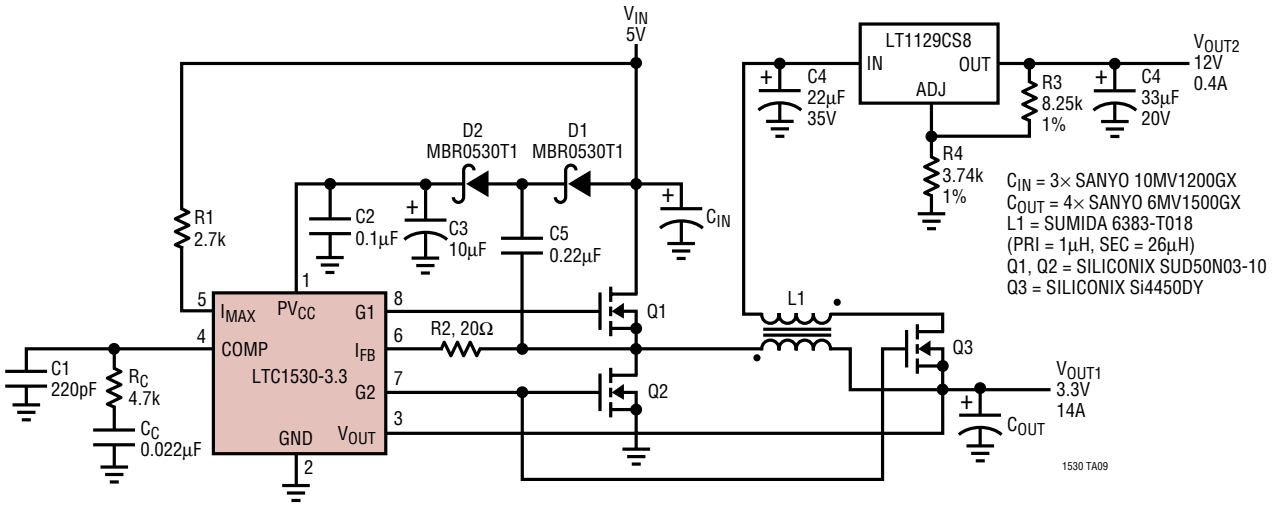
† COILTRONICS CTX02-13198 (2µH) OR
PANASONIC ETQP6F2R5HA PCC-N6 (2.5µH)

1530 TA02

DEVICE	OUTPUT CAPACITOR (C_O)	R_C	C_C	C1
LTC1530-3.3	7 X330µF AVX TPSE337M006R0100	10k	0.022µF	150pF
LTC1530-3.3	4 X1500µF SANYO 6MV1500GX	15k	0.022µF	100pF
LTC1530-2.8	7 X330µF AVX TPSE337M006R0100	8.6k	0.022µF	150pF
LTC1530-2.8	4 X1500µF SANYO 6MV1500GX	13k	0.022µF	100pF
LTC1530-2.5	7 X330µF AVX TPSE337M006R0100	7.5k	0.022µF	220pF
LTC1530-2.5	4 X1500µF SANYO 6MV1500GX	11k	0.022µF	120pF
LTC1530-1.9	7 X330µF AVX TPSE337M006R0100	5.6k	0.033µF	220pF
LTC1530-1.9	4 X1500µF SANYO 6MV1500GX	8.2k	0.022µF	220pF

1530 TA TBL

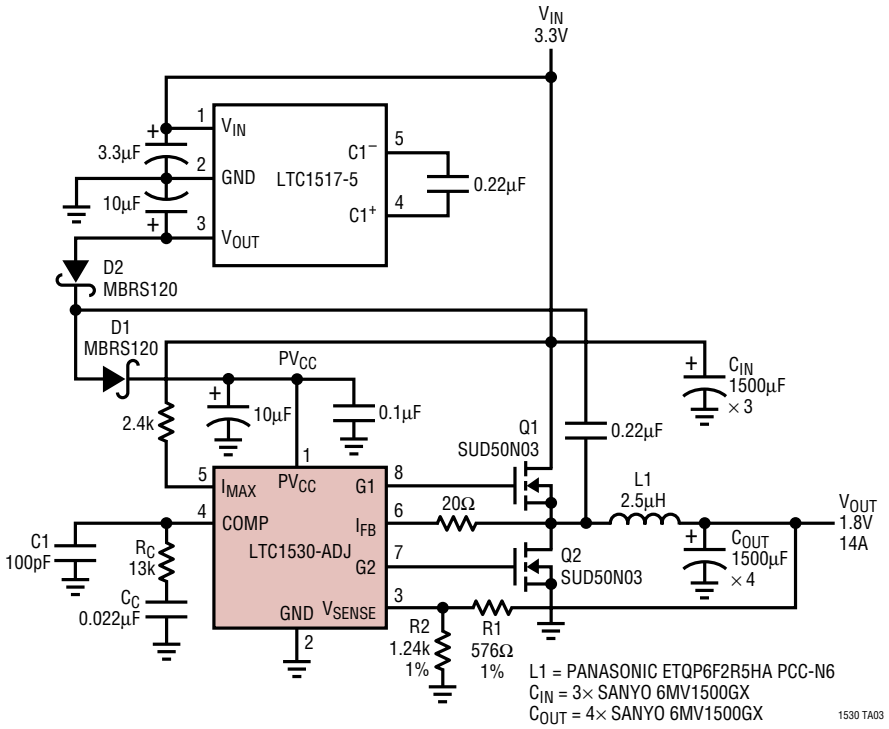
5V to Dual Output (3.3V and 12V) Synchronous Buck Converter



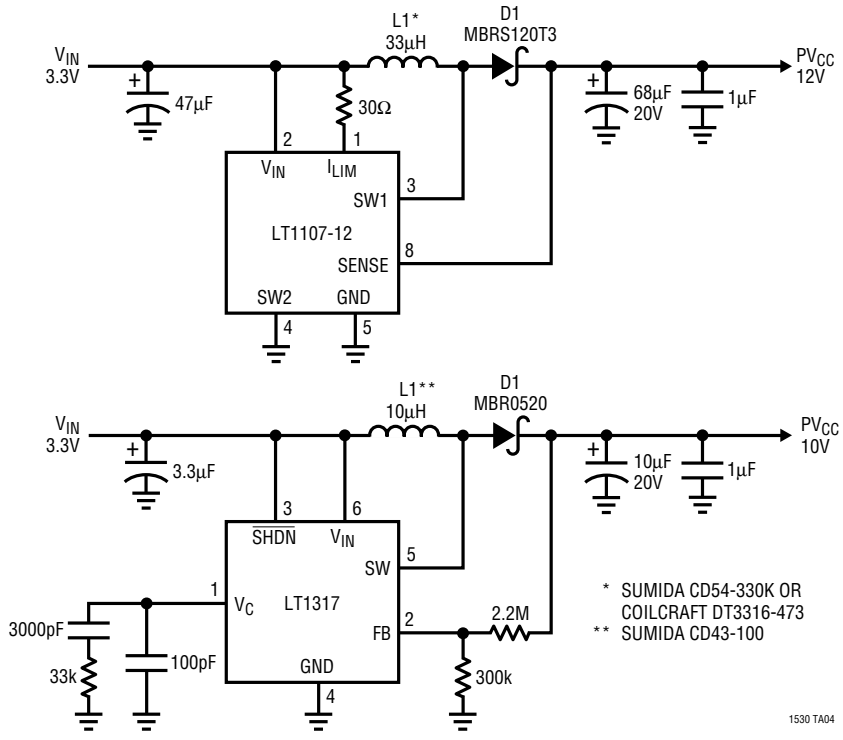
1530 TA09

TYPICAL APPLICATIONS

LTC1530 3.3V to 1.8V, 14A Application

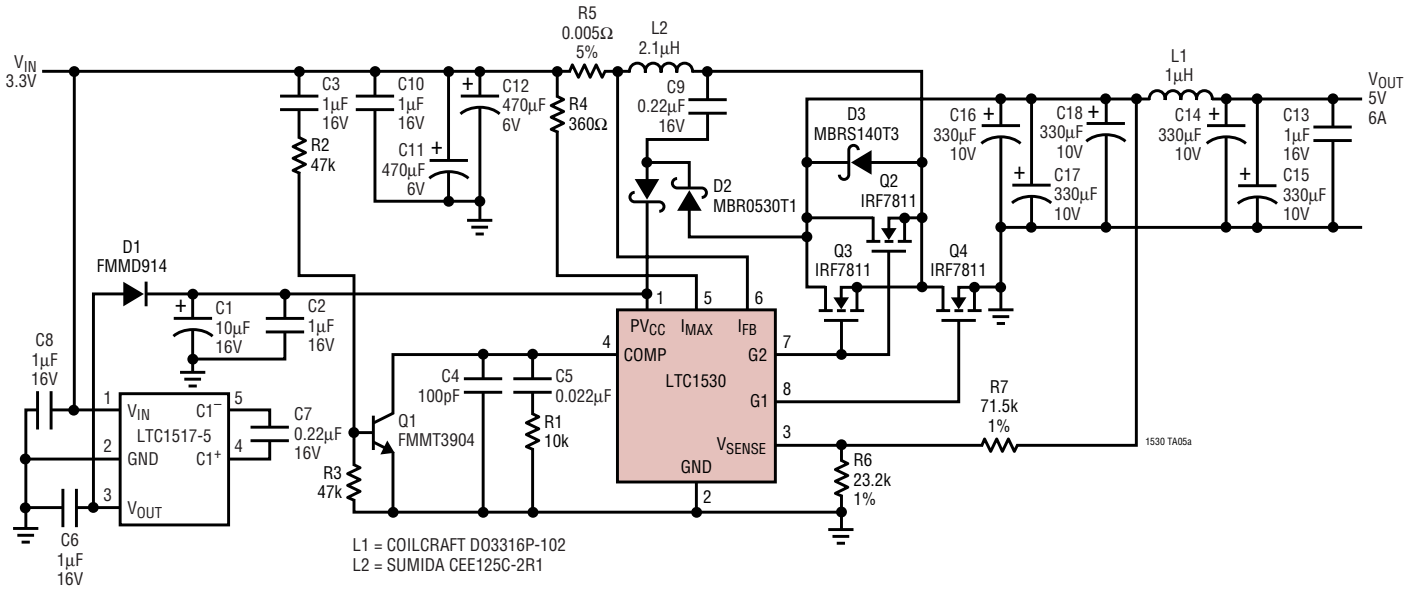


Other Methods to Generate PV_{CC} Supply from 3.3V Input

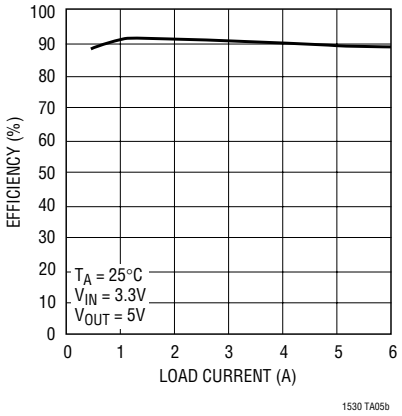


TYPICAL APPLICATIONS

LTC1530 High Efficiency Boost Converter

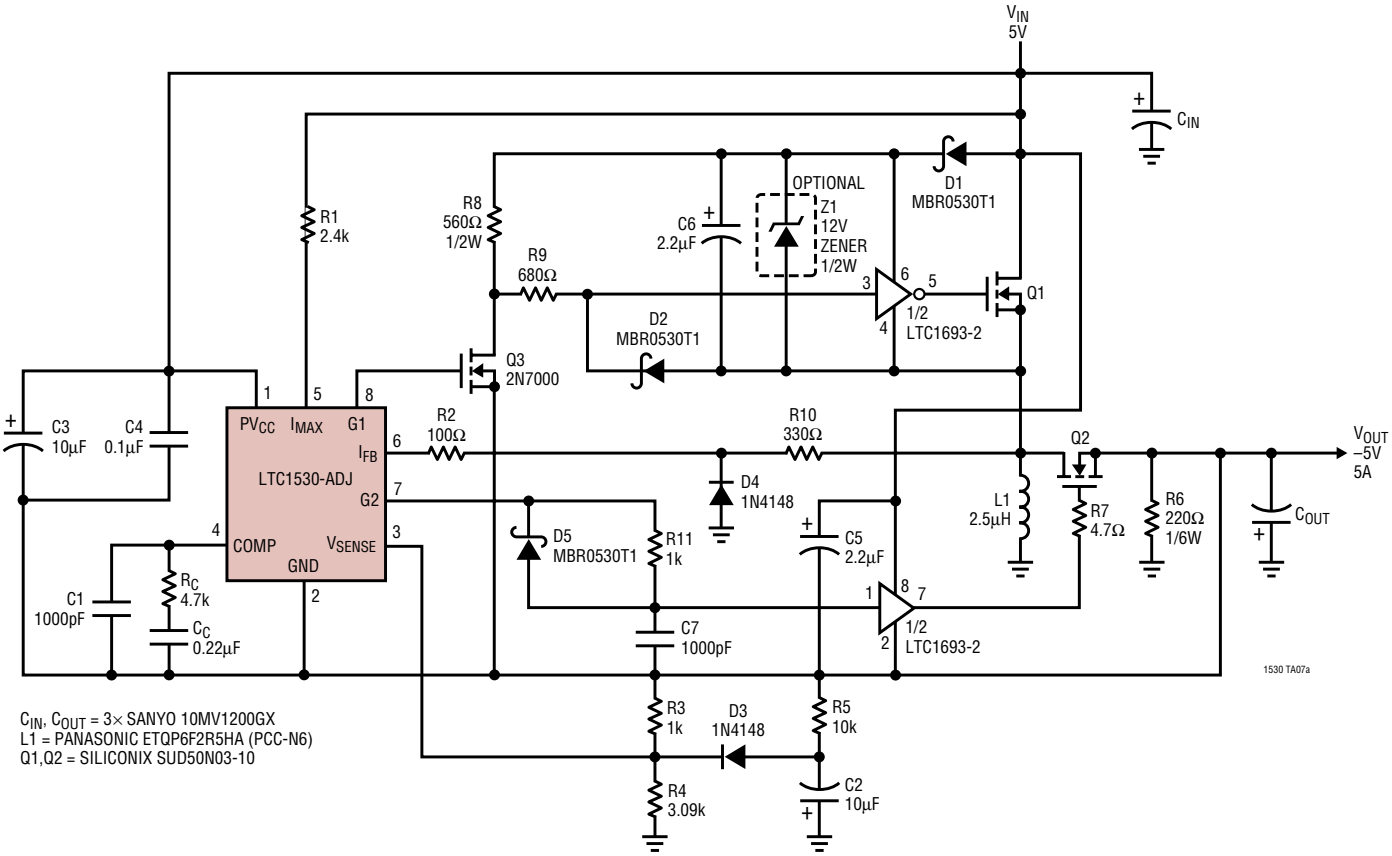


Efficiency vs Load Current

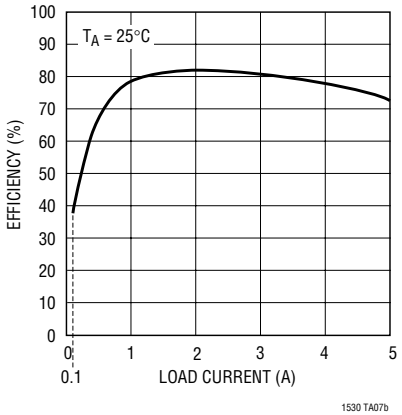


TYPICAL APPLICATIONS

LTC1530 5V to –5V Synchronous Inverter

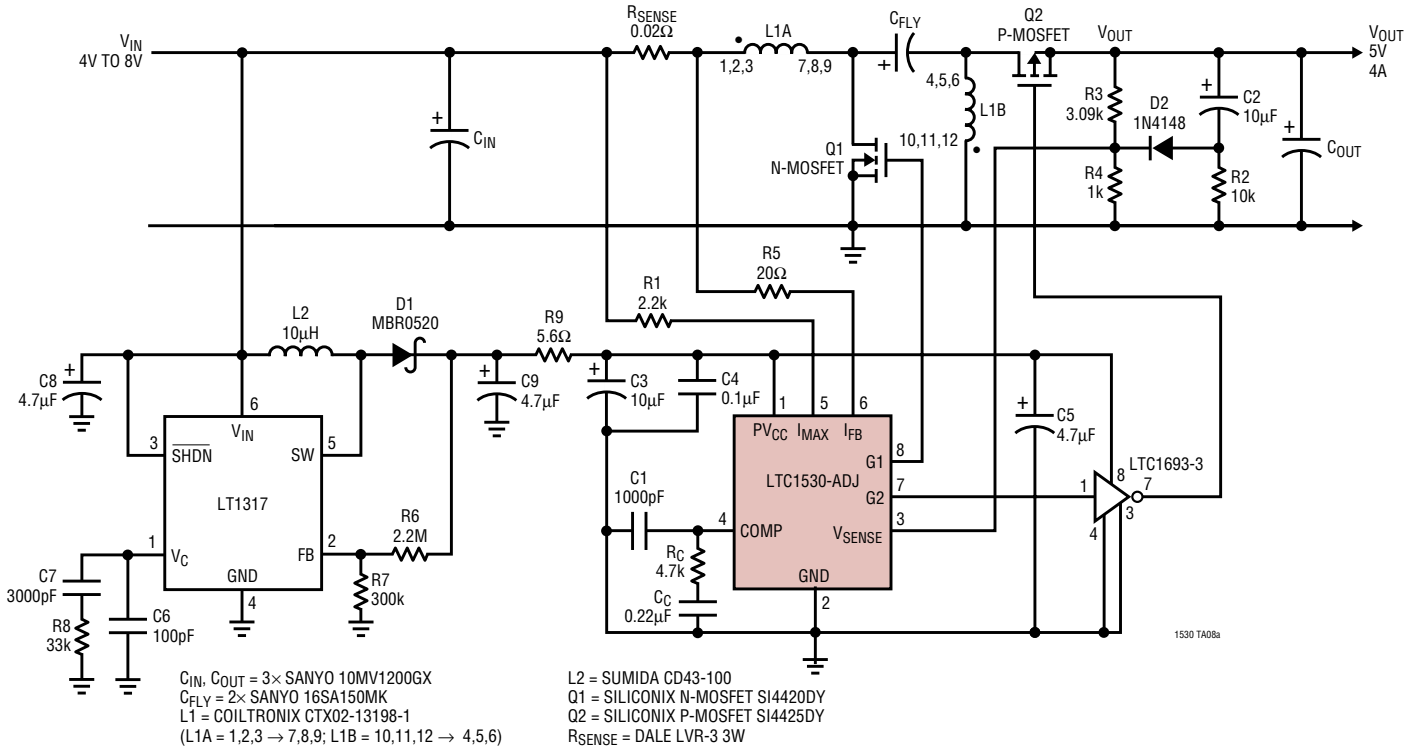


Efficiency vs Load Current

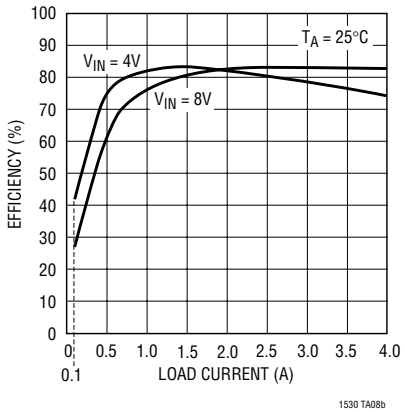


TYPICAL APPLICATIONS

LTC1530 Synchronous SEPIC Converter



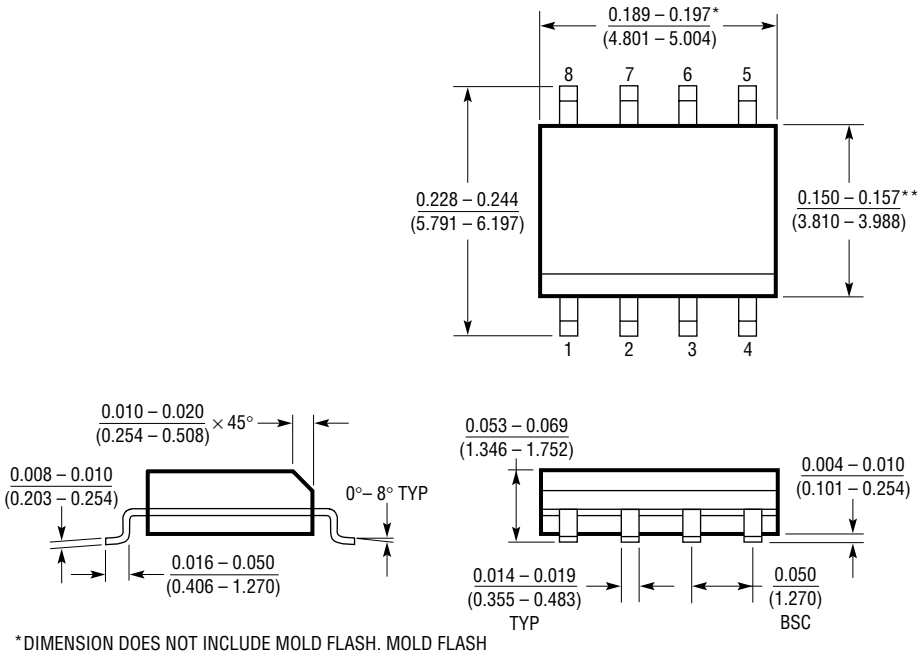
Efficiency vs Load Current



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



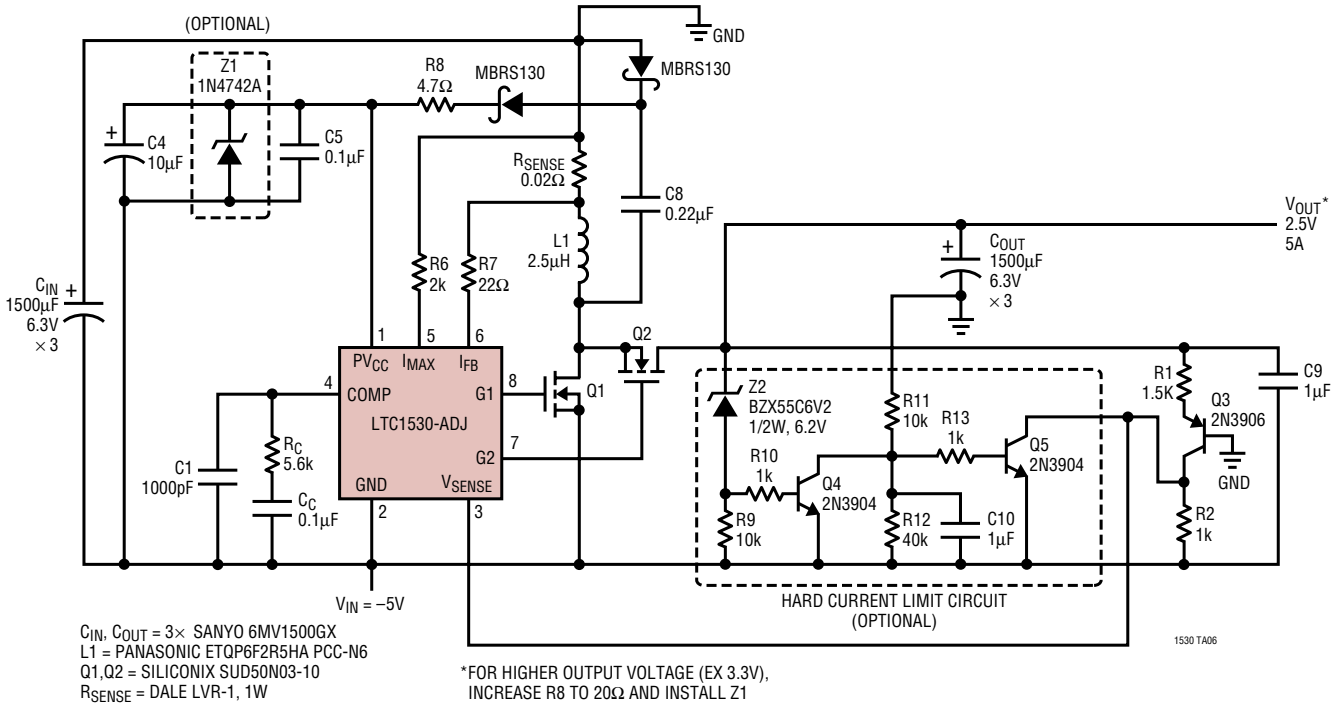
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

SO8 1298

TYPICAL APPLICATION

LTC1530 –5V to 2.5V, 5A Inverting Polarity Converter



C_{IN}, C_{OUT} = 3× SANYO 6MV1500GX
L1 = PANASONIC ETQP6F2R5HA PCC-N6
Q1,Q2 = SILICONIX SUD50N03-10
R_{SENSE} = DALE LVR-1, 1W

*FOR HIGHER OUTPUT VOLTAGE (EX 3.3V), INCREASE R8 TO 20Ω AND INSTALL Z1

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1266	Current Mode Step-Up/Down Switching Regulator Controller	Synchronous N- or P-Channel FETs, Comparator/Low-Battery Detector
LTC1430A	High Power Step-Down Switching Regulator Controller	Synchronous N-Channel FETs, 3.3V to 2.5V Conversion
LTC1553	5-Bit Programmable Synchronous Switching Regulator Controller for Pentium II Processor	Synchronous N-Channel FETs, Voltage Mode $PV_{CC} \leq 20V$, 1.8V to 3.5V Output
LTC1628	Dual High Efficiency Low Noise Synchronous Step-Down Switching Regulator	Constant Frequency, Standby 5V and 3.3V LDOs, $3.5V \leq V_{IN} \leq 36V$
LTC1629	20A to 200A PolyPhase™ Synchronous Controller	Expandable from 2-Phase to 12-Phase, Uses All Surface Mount Components, No Heat Sink
LTC1702	No R_{SENSE} 2-Phase Dual Synchronous Step-Down Controller	550kHz, No Sense Resistor
LTC1709	2-Phase Synchronous Controller with 5-Bit VID	Current Mode, V_{IN} to 36V, I_{OUT} Up to 42A, V_{OUT} from 1.3V to 3.5V
LTC1735	High Efficiency Synchronous Step-Down Switching Regulator	Drives Synchronous N-Channel FETs, $V_{IN} \leq 36V$
LTC1753	5-Bit Programmable Synchronous Switching Regulator Controller for Pentium II and Pentium III Processors	Synchronous N-Channel FETs, Voltage Mode $PV_{CC} \leq 14V$, 1.3V to 3.5V Output, VRM8.2 to VRM8.4
LTC1772	SOT-23 Step-Down Controller	100% Duty Cycle, Up to 4A, 2.2V to 9.8V V_{IN}
LTC1873	Dual 550kHz 2-Phase Synchronous Controller with 5-Bit VID	Desktop VID Codes, I_{OUT} Up to 25A On Each Channel, 28-Lead SSOP
LTC1929	2-Phase Synchronous Controller	Up to 42A, Uses All Surface Mount Components, No Heat Sink, $3.5V \leq V_{IN} \leq 36V$

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Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear-tech.com
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