LTC2224

12-Bit, 135Msps ADC

FEATURES

- **Sample Rate: 135Msps**
- **67.3dB SNR up to 140MHz Input**
- **80dB SFDR up to 150MHz Input**
- **775MHz Full Power Bandwidth S/H**
- **Single 3.3V Supply**
- **Low Power Dissipation: 630mW**
- CMOS Outputs
- Selectable Input Ranges: ±0.5V or ±1V
- No Missing Codes
- Optional Clock Duty Cycle Stabilizer
- Shutdown and Nap Modes
- Data Ready Output Clock
- Pin Compatible Family
  - 135Msps: LTC2224 (12-Bit), LTC2234 (10-Bit)
  - 105Msps: LTC2222 (12-Bit), LTC2232 (10-Bit)
  - 80Msps: LTC2223 (12-Bit), LTC2233 (10-Bit)
- 48-Pin 7mm × 7mm QFN Package

APPLICATIONS

- Wireless and Wired Broadband Communication
- Cable Head-End Systems
- Power Amplifier Linearization
- Communications Test Equipment

DESCRIPTION

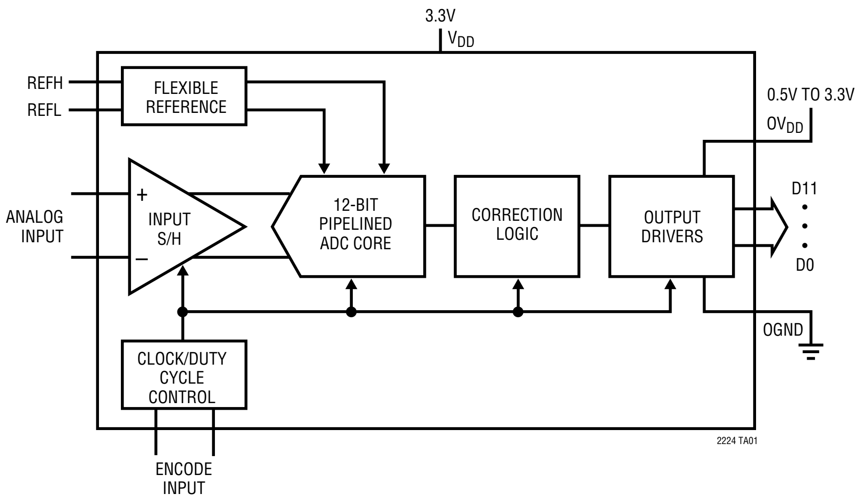
The LTC®2224 is a 135Msps, sampling 12-bit A/D converter designed for digitizing high frequency, wide dynamic range signals. The LTC2224 is perfect for demanding communications applications with AC performance that includes 67.3dB SNR and 80dB spurious free dynamic range for signals up to 150MHz. Ultralow jitter of $0.15ps_{RMS}$ allows undersampling of IF frequencies with excellent noise performance.

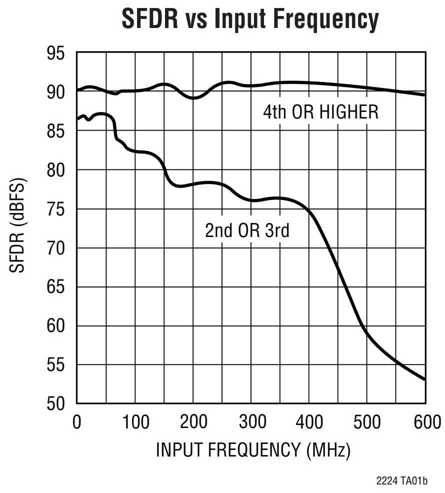
DC specs include ±0.4LSB INL (typ), ±0.3LSB DNL (typ) and no missing codes over temperature. The transition noise is a low $0.5LSB_{RMS}$.

A separate output power supply allows the CMOS output swing to range from 0.5V to 3.3V.

The ENC^+ and ENC^- inputs may be driven differentially or single ended with a sine wave, PECL, LVDS, TTL, or CMOS inputs. An optional clock duty cycle stabilizer allows high performance at full speed for a wide range of clock duty cycles.

TYPICAL APPLICATION



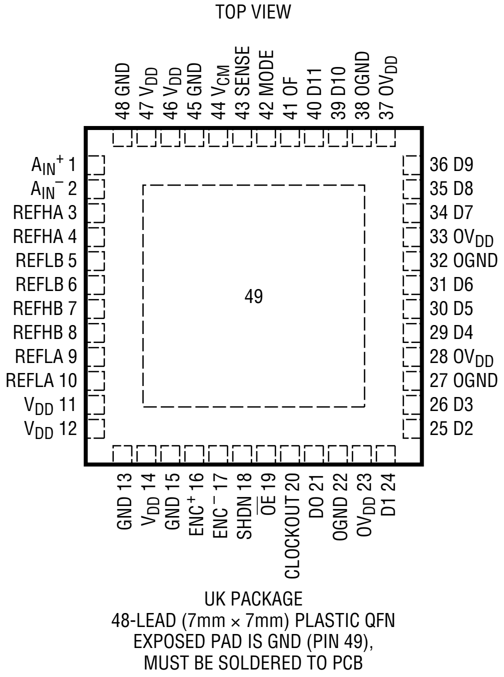

SFDR vs Input Frequency

ABSOLUTE MAXIMUM RATINGS

$OV_{DD} = V_{DD}$ (Notes 1, 2)

Supply Voltage (V_{DD}) 4V
Digital Output Ground Voltage (OGND) ....–0.3V to 1V
Analog Input Voltage (Note 3) .....–0.3V to (V_{DD} + 0.3V)
Digital Input Voltage ....–0.3V to (V_{DD} + 0.3V)
Digital Output Voltage............... –0.3V to (OV_{DD} + 0.3V)
Power Dissipation... 1500mW
Operating Temperature Range
  LTC2224C .... 0°C to 70°C
  LTC2224I..–40°C to 85°C
Storage Temperature Range ....–65°C to 125°C

PACKAGE/ORDER INFORMATION



UK PACKAGE
48-LEAD (7mm × 7mm) PLASTIC QFN
EXPOSED PAD IS GND (PIN 49),
MUST BE SOLDERED TO PCB
$T_{JMAX} = 125°C$, $\theta_{JA} = 29°C/W$

ORDER PART NUMBER	UK PART* MARKING
LTC2224CUK LTC2224IUK	LTC2224UK LTC2224UK

Consult LTC Marketing for parts specified with wider operating temperature ranges.
*The temperature grade is identified by a label on the shipping container.

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			Bits
Integral Linearity Error	Differential Analog Input (Note 5)	●	–1	±0.4	1	LSB
Differential Linearity Error	Differential Analog Input	●	–1	±0.3	1	LSB
Integral Linearity Error	Single-Ended Analog Input (Note 5)			±1		LSB
Differential Linearity Error	Single-Ended Analog Input			±0.3		LSB
Offset Error	(Note 6)	●	–35	±3	35	mV
Gain Error	External Reference	●	–2.5	±0.5	2.5	%FS
Offset Drift				±10		µV/C
Full-Scale Drift	Internal Reference External Reference			±30 ±15		ppm/C ppm/C
Transition Noise	SENSE = 1V			0.5		LSB_{RMS}

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range ($A_{IN}^+ – A_{IN}^–$)	3.1V < V_{DD} < 3.5V	●		±0.5 to ±1		V
$V_{IN, CM}$	Analog Input Common Mode	Differential Input	●	1	1.6	1.9	V
I_{IN}	Analog Input Leakage Current	0 < A_{IN}^+, $A_{IN}^–$ < V_{DD}	●	–1		1	µA
I_{SENSE}	SENSE Input Leakage	0V < SENSE < 1V	●	–1		1	µA
I_{MODE}	MODE Pin Pull-Down Current to GND				10		µA
t_{AP}	Sample and Hold Acquisition Delay Time				0		ns
t_{JITTER}	Sample and Hold Acquisition Delay Time Jitter				0.15		ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio				80		dB
	Full Power Bandwidth	Figure 8 Test Circuit			775		MHz

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SNR	Signal-to-Noise Ratio	30MHz Input (1V Range)			62.8		dB
		30MHz Input (2V Range)	●	66.5	67.6		dB
		70MHz Input (1V Range)			62.8		dB
		70MHz Input (2V Range)			67.6		dB
		140MHz Input (1V Range)			62.5		dB
		140MHz Input (2V Range)			67.3		dB
		250MHz Input (1V Range)			61.8		dB
		250MHz Input (2V Range)			65.9		dB
SFDR	Spurious Free Dynamic Range	30MHz Input (1V Range)			84		dB
		30MHz Input (2V Range)	●	72	84		dB
		70MHz Input (1V Range)			84		dB
		70MHz Input (2V Range)			84		dB
		140MHz Input (1V Range)			84		dB
		140MHz Input (2V Range)			84		dB
		250MHz Input (1V Range)			77		dB
		250MHz Input (2V Range)			77		dB
SFDR	Spurious Free Dynamic Range 4th Harmonic or Higher	30MHz Input (1V Range)			90		dB
		30MHz Input (2V Range)			90		dB
		70MHz Input (1V Range)			90		dB
		70MHz Input (2V Range)			90		dB
		140MHz Input (1V Range)			90		dB
		140MHz Input (2V Range)			90		dB
		250MHz Input (1V Range)			90		dB
		250MHz Input (2V Range)			90		dB
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	30MHz Input (1V Range)			62.8		dB
		30MHz Input (2V Range)	●	66	67.4		dB
		70MHz Input (1V Range)			62.8		dB
		70MHz Input (2V Range)			67.2		dB
IMD	Intermodulation Distortion	f_{IN1} = 138MHz, f_{IN2} = 140MHz			81		dBc

INTERNAL REFERENCE CHARACTERISTICS (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CM} Output Voltage	$I_{OUT} = 0$	1.575	1.600	1.625	V
V_{CM} Output Tempco			±25		ppm/C
V_{CM} Line Regulation	$3.1V < V_{DD} < 3.5V$		3		mV/V
V_{CM} Output Resistance	$–1mA < I_{OUT} < 1mA$		4		Ω

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ENCODE INPUTS (ENC^+, $ENC^–$)							
V_{ID}	Differential Input Voltage		●	0.2			V
V_{ICM}	Common Mode Input Voltage	Internally Set Externally Set (Note 7)	 ●	 1.1	1.6 1.6	 2.5	V V
R_{IN}	Input Resistance				6		kΩ
C_{IN}	Input Capacitance	(Note 7)			3		pF
LOGIC INPUTS ($\overline{OE}$, SHDN)							
V_{IH}	High Level Input Voltage	$V_{DD} = 3.3V$	●	2			V
V_{IL}	Low Level Input Voltage	$V_{DD} = 3.3V$	●			0.8	V
I_{IN}	Input Current	$V_{IN} = 0V$ to V_{DD}	●	–10		10	µA
C_{IN}	Input Capacitance	(Note 7)			3		pF
LOGIC OUTPUTS							
$OV_{DD} = 3.3V$							
C_{OZ}	Hi-Z Output Capacitance	$\overline{OE}$ = High (Note 7)			3		pF
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$			50		mA
I_{SINK}	Output Sink Current	$V_{OUT} = 3.3V$			50		mA
V_{OH}	High Level Output Voltage	$I_O = –10µA$ $I_O = –200µA$	 ●	 3.1	3.295 3.29		V V
V_{OL}	Low Level Output Voltage	$I_O = 10µA$ $I_O = 1.6mA$	 ●		0.005 0.09	 0.4	V V
$OV_{DD} = 2.5V$							
V_{OH}	High Level Output Voltage	$I_O = –200µA$			2.49		V
V_{OL}	Low Level Output Voltage	$I_O = 1.6mA$			0.09		V
$OV_{DD} = 1.8V$							
V_{OH}	High Level Output Voltage	$I_O = –200µA$			1.79		V
V_{OL}	Low Level Output Voltage	$I_O = 1.6mA$			0.09		V

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 8)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Analog Supply Voltage		●	3.1	3.3	3.5	V
OV_{DD}	Output Supply Voltage		●	0.5	3.3	3.6	V
I_{VDD}	Analog Supply Current		●		191	206	mA
P_{DISS}	Power Dissipation		●		630	680	mW
P_{SHDN}	Shutdown Power	SHDN = High, $\overline{OE}$ = High, No CLK			2		mW
P_{NAP}	Nap Mode Power	SHDN = High, $\overline{OE}$ = Low, No CLK			35		mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_S	Sampling Frequency		●	1		135	MHz
t_L	ENC Low Time	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	3.5 2	3.7 3.7	500 500	ns ns
t_H	ENC High Time	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	3.5 2	3.7 3.7	500 500	ns ns
t_{AP}	Sample-and-Hold Aperture Delay				0		ns
t_{OE}	Output Enable Delay	(Note 7)	●		5	10	ns
t_D	ENC to DATA Delay	(Note 7)	●	1.3	2.1	3.5	ns
t_C	ENC to CLOCKOUT Delay	(Note 7)	●	1.3	2.1	3.5	ns
	DATA to CLOCKOUT Skew	(t_C - t_D) (Note 7)	●	–0.6	0	0.6	ns
Pipeline Latency					5		Cycles

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with GND and OGND wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below GND or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above V_{DD} without latchup.

Note 4: V_{DD} = 3.3V, OV_{DD} = 1.8V, f_{SAMPLE} = 135MHz, differential ENC^+/ENC^- = $2V_{P-P}$ sine wave, input range = $2V_{P-P}$ with differential drive, unless otherwise noted.

Note 5: Integral nonlinearity is defined as the deviation of a code from a "best straight line" fit to the transfer curve. The deviation is measured from the center of the quantization band.

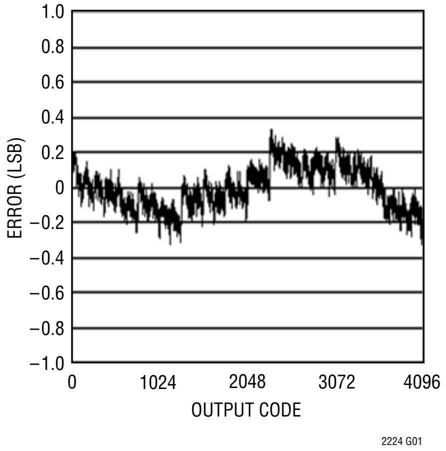
Note 6: Offset error is the offset voltage measured from –0.5 LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111 in 2's complement output mode.

Note 7: Guaranteed by design, not subject to test.

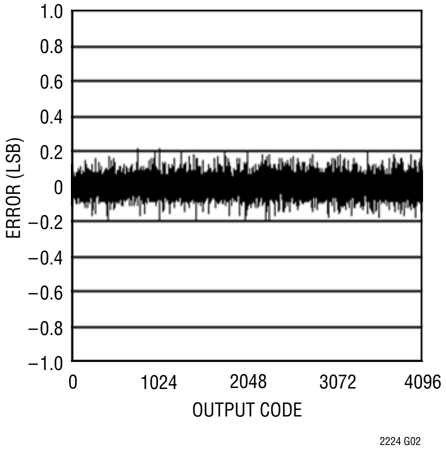
Note 8: V_{DD} = 3.3V, OV_{DD} = 1.8V, f_{SAMPLE} = 135MHz, differential ENC^+/ENC^- = $2V_{P-P}$ sine wave, input range = $1V_{P-P}$ with differential drive, output C_{LOAD} = 5pF.

TYPICAL PERFORMANCE CHARACTERISTICS

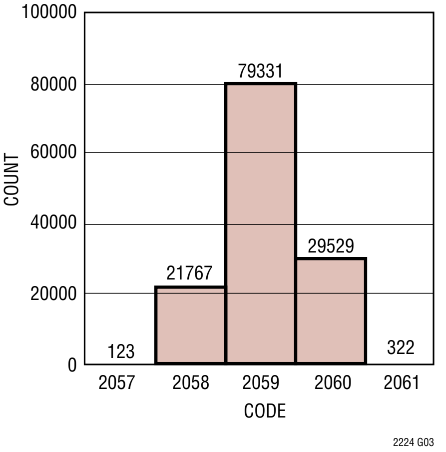
LTC2224: INL, 2V Range



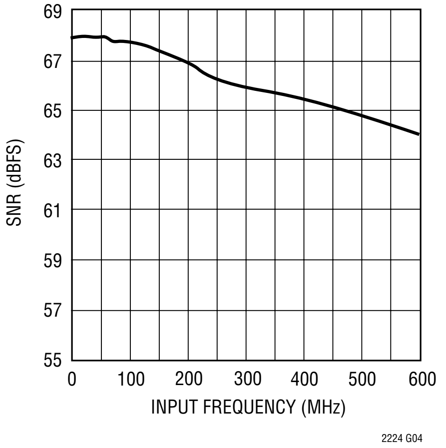
LTC2224: DNL, 2V Range



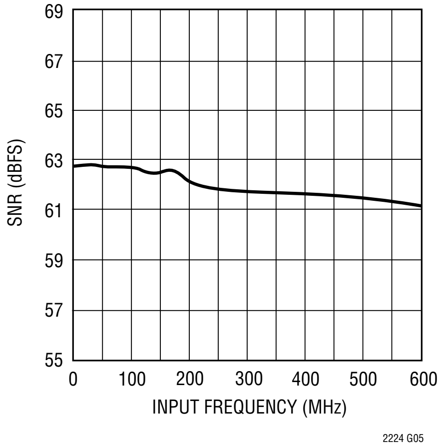
LTC2224: Noise Histogram



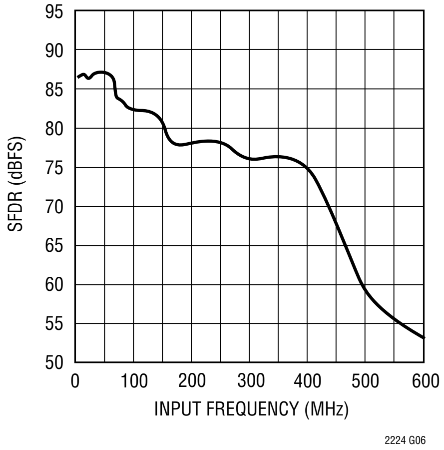
LTC2224: SNR vs Input Frequency, –1dB, 2V Range



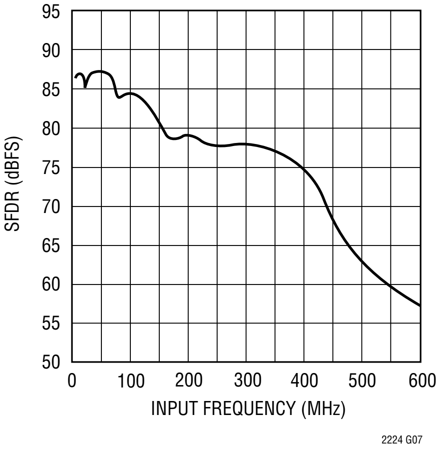
LTC2224: SNR vs Input Frequency, –1dB, 1V Range



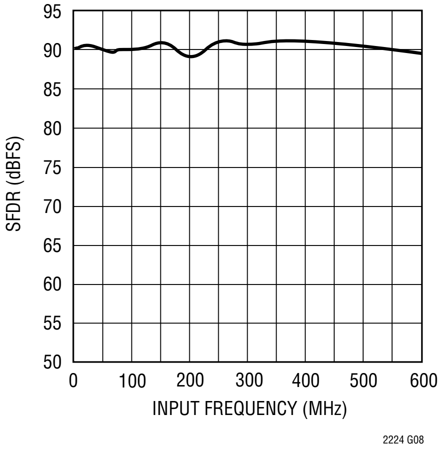
LTC2224: SFDR (HD2 and HD3) vs Input Frequency, –1dB, 2V Range



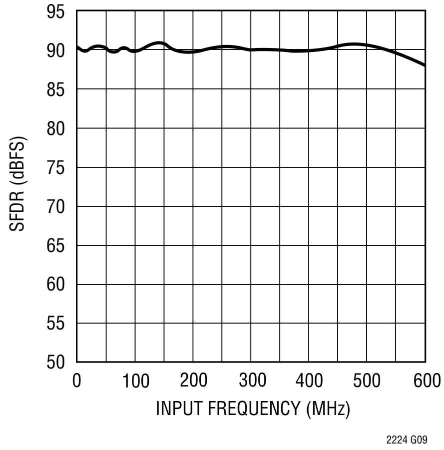
LTC2224: SFDR (HD2 and HD3) vs Input Frequency, –1dB, 1V Range



LTC2224: SFDR (HD4+) vs Input Frequency, –1dB, 2V Range

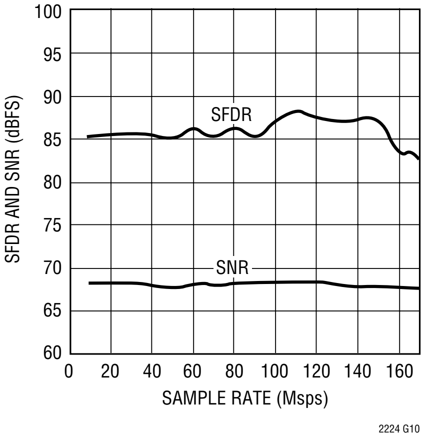


LTC2224: SFDR (HD4+) vs Input Frequency, –1dB, 1V Range

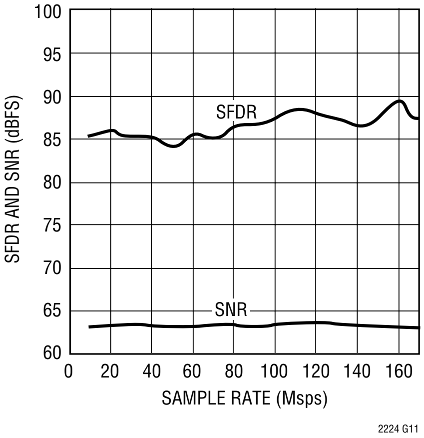


TYPICAL PERFORMANCE CHARACTERISTICS

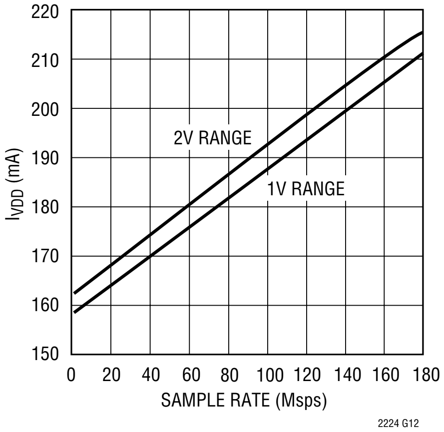
LTC2224: SFDR and SNR vs Sample Rate, 2V Range, f_{IN} = 30MHz, –1dB



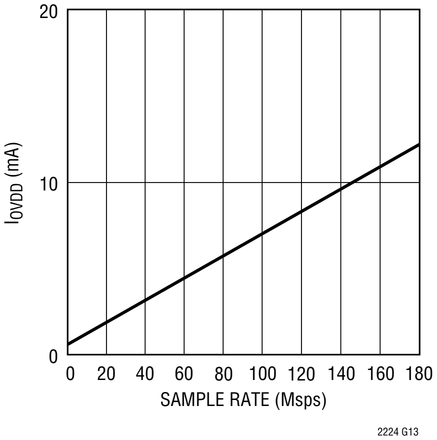
LTC2224: SFDR and SNR vs Sample Rate, 1V Range, f_{IN} = 30MHz, –1dB



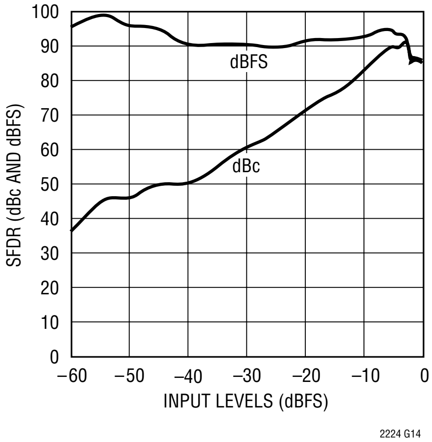
LTC2224: I_{VDD} vs Sample Rate, 5MHz Sine Wave Input, –1dB



LTC2224: I_{OVDD} vs Sample Rate, 5MHz Sine Wave Input, –1dB, OV_{DD} = 1.8V

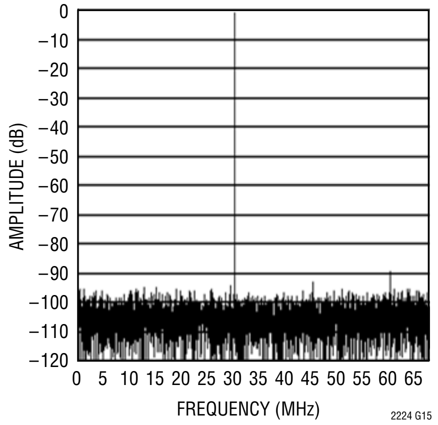


LTC2224: SFDR vs Input Level, f_{IN} = 70MHz, 2V Range

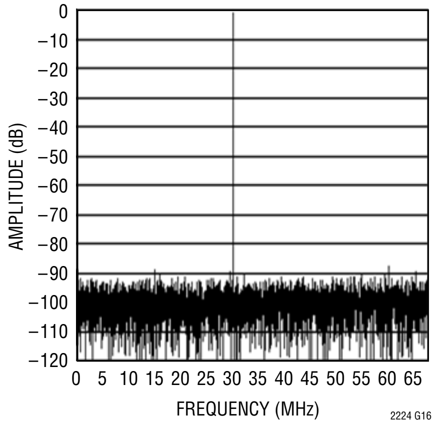


TYPICAL PERFORMANCE CHARACTERISTICS

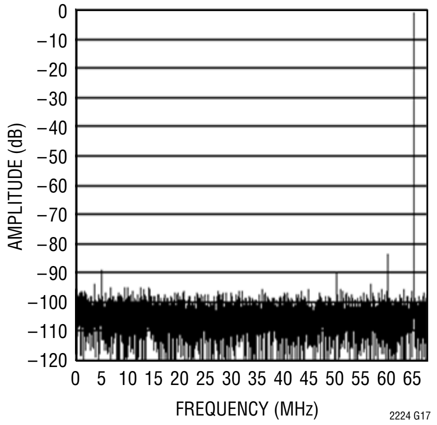
LTC2224: 8192 Point FFT, f_{IN} = 30MHz, –1dB, 2V Range



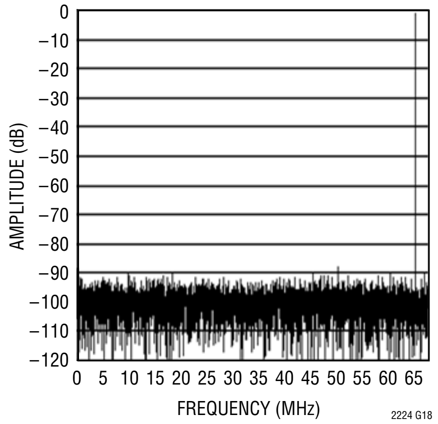
LTC2224: 8192 Point FFT, f_{IN} = 30MHz, –1dB, 1V Range



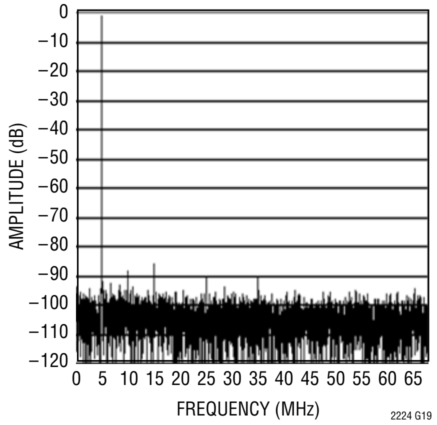
LTC2224: 8192 Point FFT, f_{IN} = 70MHz, –1dB, 2V Range



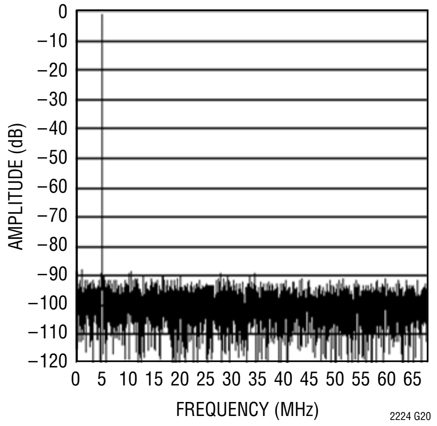
LTC2224: 8192 Point FFT, f_{IN} = 70MHz, –1dB, 1V Range



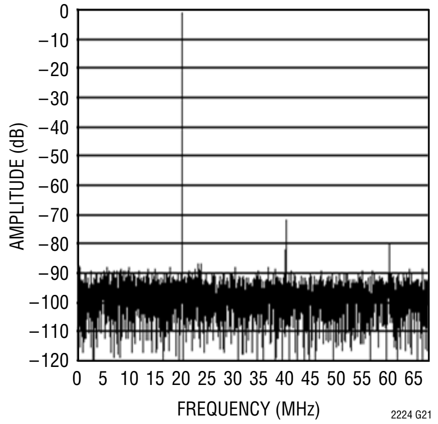
LTC2224: 8192 Point FFT, f_{IN} = 140MHz, –1dB, 2V Range



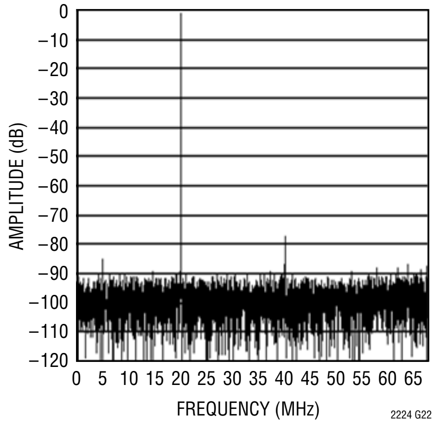
LTC2224: 8192 Point FFT, f_{IN} = 140MHz, –1dB, 1V Range



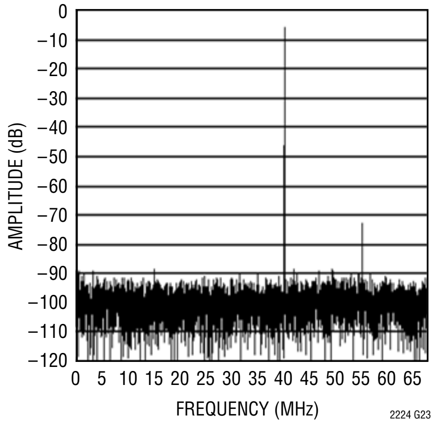
LTC2224: 8192 Point FFT, f_{IN} = 250MHz, –1dB, 2V Range



LTC2224: 8192 Point FFT, f_{IN} = 250MHz, –1dB, 1V Range



LTC2224: 8192 Point FFT, f_{IN} = 500MHz, –6dB, 1V Range



PIN FUNCTIONS

A_{IN}+ (Pin 1): Positive Differential Analog Input.

A_{IN}– (Pin 2): Negative Differential Analog Input.

REFHA (Pins 3, 4): ADC High Reference. Bypass to Pins 5, 6 with 0.1μF ceramic chip capacitor, to Pins 9, 10 with a 2.2μF ceramic capacitor and to ground with a 1μF ceramic capacitor.

REFLB (Pins 5, 6): ADC Low Reference. Bypass to Pins 3, 4 with 0.1μF ceramic chip capacitor. Do not connect to Pins 9, 10.

REFHB (Pins 7, 8): ADC High Reference. Bypass to Pins 9, 10 with 0.1μF ceramic chip capacitor. Do not connect to Pins 3, 4.

REFLA (Pins 9, 10): ADC Low Reference. Bypass to Pins 7, 8 with 0.1μF ceramic chip capacitor, to Pins 3, 4 with a 2.2μF ceramic capacitor and to ground with a 1μF ceramic capacitor.

V_{DD} (Pins 11, 12, 14, 46, 47): 3.3V Supply. Bypass to GND with 0.1μF ceramic chip capacitors. Adjacent pins can share a bypass capacitor.

GND (Pins 13, 15, 45, 48): ADC Power Ground.

ENC^+ (Pin 16): Encode Input. The input is sampled on the positive edge.

ENC^- (Pin 17): Encode Complement Input. The input is sampled on the negative edge. Bypass to ground with 0.1μF ceramic for single-ended ENCODE signal.

SHDN (Pin 18): Shutdown Mode Selection Pin. Connecting SHDN to GND and $\overline{OE}$ to GND results in normal operation with the outputs enabled. Connecting SHDN to GND and $\overline{OE}$ to V_{DD} results in normal operation with the outputs at high impedance. Connecting SHDN to V_{DD} and $\overline{OE}$ to GND results in nap mode with the outputs at high impedance. Connecting SHDN to V_{DD} and $\overline{OE}$ to V_{DD} results in sleep mode with the outputs at high impedance.

$\overline{OE}$ (Pin 19): Output Enable Pin. Refer to SHDN pin function.

CLOCKOUT (Pin 20): Data Valid Output. Latch data on the falling edge of CLOCKOUT.

D0 – D11 (Pins 21, 24, 25, 26, 29, 30, 31, 34, 35, 36, 39, 40): Digital Outputs. D11 is the MSB.

OGND (Pins 22, 27, 32, 38): Output Driver Ground.

OV_{DD} (Pins 23, 28, 33, 37): Positive Supply for the Output Drivers. Bypass to ground with 0.1μF ceramic chip capacitors.

OF (Pin 41): Over/Under Flow Output. High when an over or under flow has occurred.

MODE (Pin 42): Output Format and Clock Duty Cycle Stabilizer Selection Pin. Connecting MODE to 0V selects straight binary output format and turns the clock duty cycle stabilizer off. Connecting MODE to 1/3 V_{DD} selects straight binary output format and turns the clock duty cycle stabilizer on. Connecting MODE to 2/3 V_{DD} selects 2's complement output format and turns the clock duty cycle stabilizer on. Connecting MODE to V_{DD} selects 2's complement output format and turns the clock duty cycle stabilizer off.

SENSE (Pin 43): Reference Programming Pin. Connecting SENSE to V_{CM} selects the internal reference and a ±0.5V input range. V_{DD} selects the internal reference and a ±1V input range. An external reference greater than 0.5V and less than 1V applied to SENSE selects an input range of $\pm V_{SENSE}$. ±1V is the largest valid input range.

V_{CM} (Pin 44): 1.6V Output and Input Common Mode Bias. Bypass to ground with 2.2μF ceramic chip capacitor.

Exposed Pad (Pin 49): ADC Power Ground. The exposed pad on the bottom of the package needs to be soldered to ground.

FUNCTIONAL BLOCK DIAGRAM

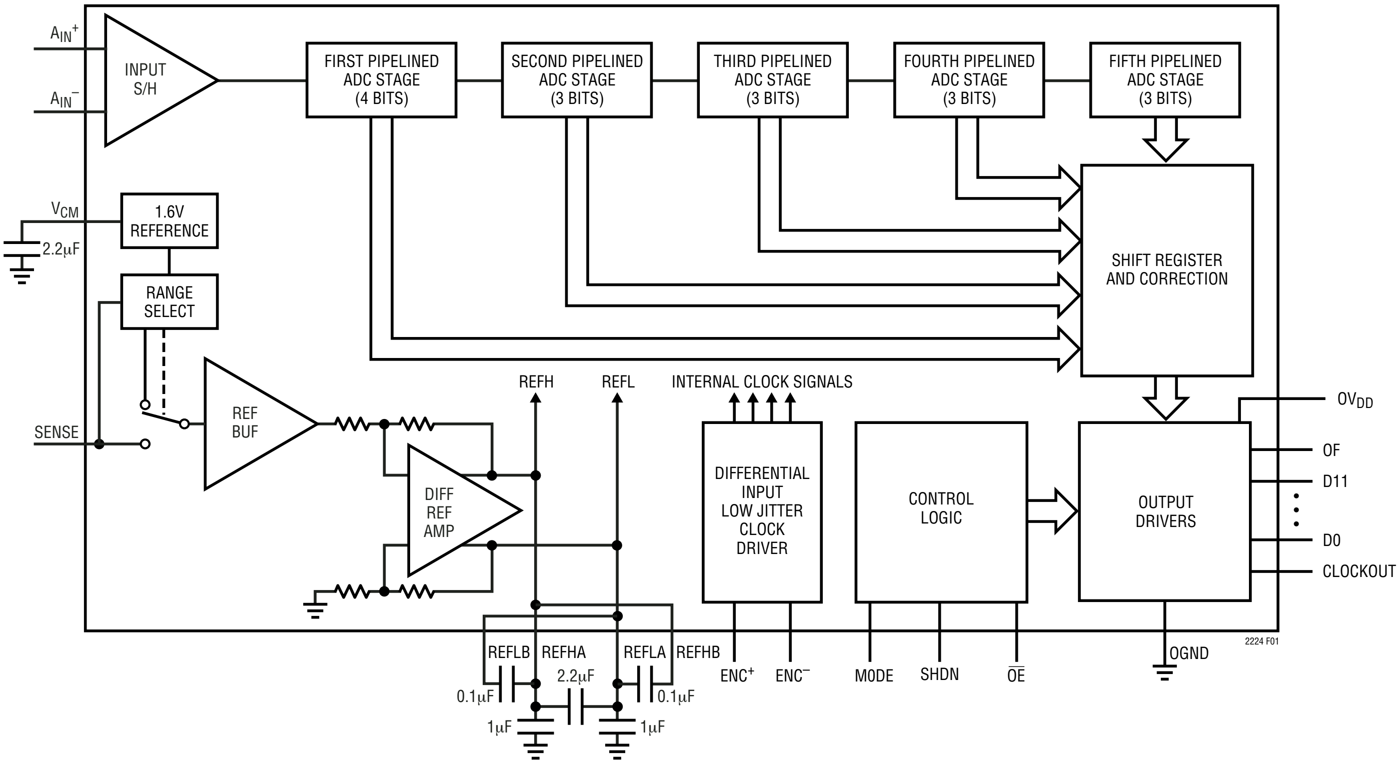
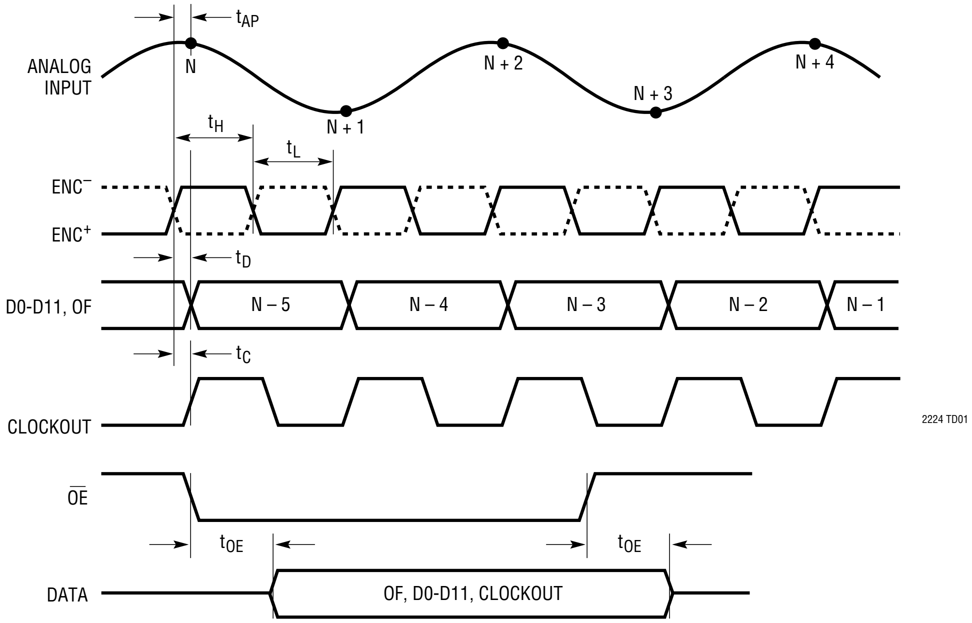


Figure 1. Functional Block Diagram

TIMING DIAGRAMS

Timing Diagram



APPLICATIONS INFORMATION

DYNAMIC PERFORMANCE

Signal-to-Noise Plus Distortion Ratio

The signal-to-noise plus distortion ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the ADC output. The output is band limited to frequencies above DC to below half the sampling frequency.

Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC.

Total Harmonic Distortion

Total harmonic distortion is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20Log \sqrt{(V2^2 + V3^2 + V4^2 + \ldots Vn^2)}/V1$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through Vn are the amplitudes of the second through nth harmonics. The THD calculated in this data sheet uses all the harmonics up to the fifth.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. The 3rd order intermodulation products are 2fa + fb, 2fb + fa, 2fa – fb and 2fb – fa. The intermodulation distortion is defined as the ratio of the RMS value of either input tone to the RMS value of the largest 3rd order intermodulation product.

Spurious Free Dynamic Range (SFDR)

Spurious free dynamic range is the peak harmonic or spurious noise that is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full scale input signal.

Full Power Bandwidth

The full power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full scale input signal.

Aperture Delay Time

The time from when a rising ENC^+ equals the ENC^- voltage to the instant that the input signal is held by the sample and hold circuit.

Aperture Delay Jitter

The variation in the aperture delay time from conversion to conversion. This random variation will result in noise when sampling an AC input. The signal to noise ratio due to the jitter alone will be:

$$SNR_{JITTER} = -20\log (2\pi) \bullet f_{IN} \bullet t_{JITTER}$$

APPLICATIONS INFORMATION

CONVERTER OPERATION

As shown in Figure 1, the LTC2224 is a CMOS pipelined multistep converter. The converter has five pipelined ADC stages; a sampled analog input will result in a digitized value five cycles later (see the Timing Diagram section). For optimal AC performance the analog inputs should be driven differentially. For cost sensitive applications, the analog inputs can be driven single-ended with slightly worse harmonic distortion. The encode input is differential for improved common mode noise immunity. The LTC2224 has two phases of operation, determined by the state of the differential ENC^+/ENC^- input pins. For brevity, the text will refer to ENC^+ greater than ENC^- as ENC high and ENC^+ less than ENC^- as ENC low.

Each pipelined stage shown in Figure 1 contains an ADC, a reconstruction DAC and an interstage residue amplifier. In operation, the ADC quantizes the input to the stage and the quantized value is subtracted from the input by the DAC to produce a residue. The residue is amplified and output by the residue amplifier. Successive stages operate out of phase so that when the odd stages are outputting their residue, the even stages are acquiring that residue and vice versa.

When ENC is low, the analog input is sampled differentially directly onto the input sample-and-hold capacitors, inside the "Input S/H" shown in the block diagram. At the instant that ENC transitions from low to high, the sampled input is held. While ENC is high, the held input voltage is buffered by the S/H amplifier which drives the first pipelined ADC stage. The first stage acquires the output of the S/H during this high phase of ENC. When ENC goes back low, the first stage produces its residue which is acquired by the second stage. At the same time, the input S/H goes back to acquiring the analog input. When ENC goes back high, the second stage produces its residue which is acquired by the third stage. An identical process is repeated for the third and fourth stages, resulting in a fourth stage residue that is sent to the fifth stage ADC for final evaluation.

Each ADC stage following the first has additional range to accommodate flash and amplifier offset errors. Results from all of the ADC stages are digitally synchronized such that the results can be properly combined in the correction logic before being sent to the output buffer.

SAMPLE/HOLD OPERATION AND INPUT DRIVE

Sample/Hold Operation

Figure 2 shows an equivalent circuit for the LTC2224 CMOS differential sample-and-hold. The analog inputs are connected to the sampling capacitors (C_{SAMPLE}) through NMOS transistors. The capacitors shown attached to each input ($C_{PARASITIC}$) are the summation of all other capacitance associated with each input.

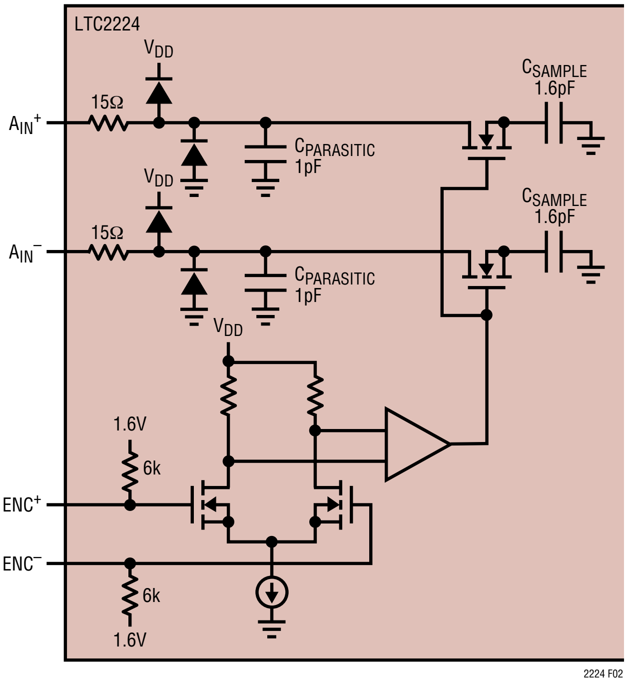


Figure 2. Equivalent Input Circuit

APPLICATIONS INFORMATION

During the sample phase when ENC is low, the transistors connect the analog inputs to the sampling capacitors and they charge to, and track the differential input voltage. When ENC transitions from low to high, the sampled input voltage is held on the sampling capacitors. During the hold phase when ENC is high, the sampling capacitors are disconnected from the input and the held voltage is passed to the ADC core for processing. As ENC transitions from high to low, the inputs are reconnected to the sampling capacitors to acquire a new sample. Since the sampling capacitors still hold the previous sample, a charging glitch proportional to the change in voltage between samples will be seen at this time. If the change between the last sample and the new sample is small, the charging glitch seen at the input will be small. If the input change is large, such as the change seen with input frequencies near Nyquist, then a larger charging glitch will be seen.

Single-Ended Input

For cost sensitive applications, the analog inputs can be driven single-ended. With a single-ended input the harmonic distortion and INL will degrade, but the SNR and DNL will remain unchanged. For a single-ended input, A_{IN}^+ should be driven with the input signal and A_{IN}^- should be connected to 1.6V or V_{CM}.

Common Mode Bias

For optimal performance the analog inputs should be driven differentially. Each input should swing ±0.5V for the 2V range or ±0.25V for the 1V range, around a common mode voltage of 1.6V. The V_{CM} output pin (Pin 60) may be used to provide the common mode bias level. V_{CM} can be tied directly to the center tap of a transformer to set the DC input level or as a reference level to an op amp differential driver circuit. The V_{CM} pin must be bypassed to ground close to the ADC with a 2.2µF or greater capacitor.

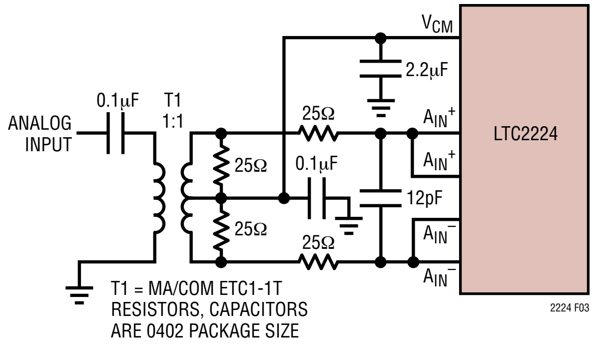
Input Drive Impedance

As with all high performance, high speed ADCs, the dynamic performance of the LTC2224 can be influenced by the input drive circuitry, particularly the second and third harmonics. Source impedance and input reactance can influence SFDR. At the falling edge of ENC, the sample-and-hold circuit will connect the 1.6pF sampling capacitor to the input pin and start the sampling period. The sampling period ends when ENC rises, holding the sampled input on the sampling capacitor. Ideally the input circuitry should be fast enough to fully charge the sampling capacitor during the sampling period $1/(2F_{ENCODE})$; however, this is not always possible and the incomplete settling may degrade the SFDR. The sampling glitch has been designed to be as linear as possible to minimize the effects of incomplete settling.

For the best performance, it is recommended to have a source impedance of 100Ω or less for each input. The source impedance should be matched for the differential inputs. Poor matching will result in higher even order harmonics, especially the second.

Input Drive Circuits

Figure 3 shows the LTC2224 being driven by an RF transformer with a center tapped secondary. The secondary center tap is DC biased with V_{CM}, setting the ADC input



T1 = MA/COM ETC1-1T
RESISTORS, CAPACITORS
ARE 0402 PACKAGE SIZE

Figure 3. Single-Ended to Differential Conversion Using a Transformer

APPLICATIONS INFORMATION

signal at its optimum DC level. Figure 3 shows a 1:1 turns ratio transformer. Other turns ratios can be used if the source impedance seen by the ADC does not exceed 100Ω for each ADC input. A disadvantage of using a transformer is the loss of low frequency response. Most small RF transformers have poor performance at frequencies below 1MHz.

Figure 4 demonstrates the use of a differential amplifier to convert a single ended input signal into a differential input signal. The advantage of this method is that it provides low frequency input response; however, the limited gain bandwidth of most op amps will limit the SFDR at high input frequencies.

Figure 5 shows a single-ended input circuit. The impedance seen by the analog inputs should be matched. This circuit is not recommended if low distortion is required.

The 25Ω resistors and 12pF capacitor on the analog inputs serve two purposes: isolating the drive circuitry from the sample-and-hold charging glitches and limiting the wideband noise at the converter input. For input frequencies higher than 100MHz, the capacitor may need to be decreased to prevent excessive signal loss.

The A_{IN}^+ and A_{IN}^- inputs each have two pins to reduce package inductance. The two A_{IN}^+ and the two A_{IN}^- pins should be shorted together.

For input frequencies above 100MHz the input circuits of Figure 6, 7 and 8 are recommended. The balun transformer gives better high frequency response than a flux coupled center tapped transformer. The coupling capacitors allow the analog inputs to be DC biased at 1.6V. In Figure 8 the series inductors are impedance matching elements that maximize the ADC bandwidth.

Reference Operation

Figure 9 shows the LTC2224 reference circuitry consisting of a 1.6V bandgap reference, a difference amplifier and switching and control circuit. The internal voltage reference can be configured for two pin selectable input ranges of 2V (±1V differential) or 1V (±0.5V differential). Tying the SENSE pin to V_{DD} selects the 2V range; typing the SENSE pin to V_{CM} selects the 1V range.

The 1.6V bandgap reference serves two functions: its output provides a DC bias point for setting the common mode voltage of any external input circuitry; additionally, the reference is used with a difference amplifier to generate the differential reference levels needed by the internal ADC circuitry. An external bypass capacitor is required for the 1.6V reference output, V_{CM}. This provides a high frequency low impedance path to ground for internal and external circuitry.

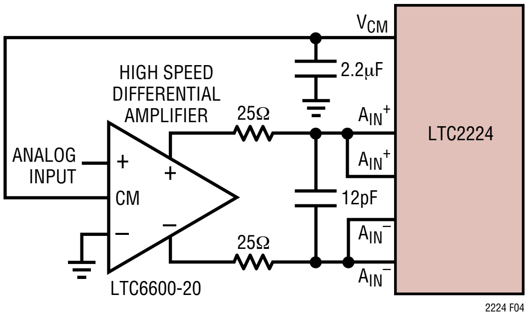


Figure 4. Differential Drive with an Amplifier

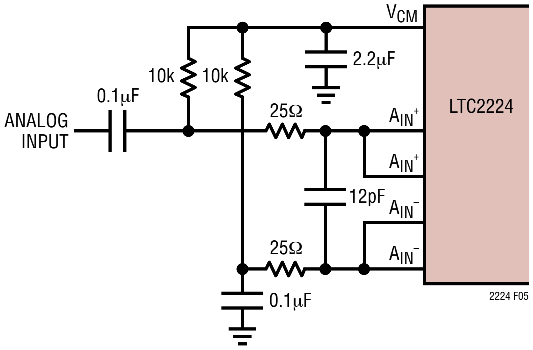


Figure 5. Single-Ended Drive

APPLICATIONS INFORMATION

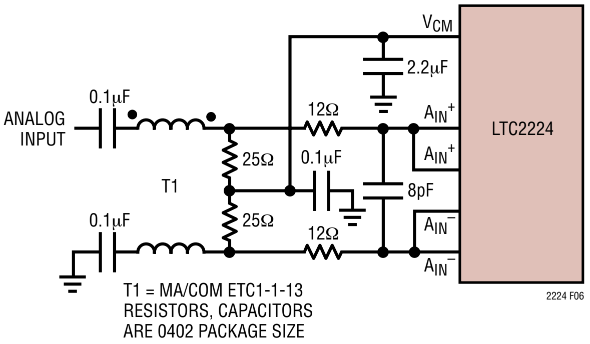


Figure 6. Recommended Front End Circuit for Input Frequencies Between 100MHz and 250MHz

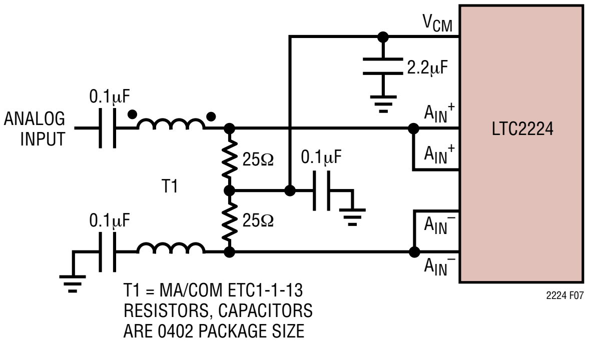


Figure 7. Recommended Front End Circuit for Input Frequencies Between 250MHz and 500MHz

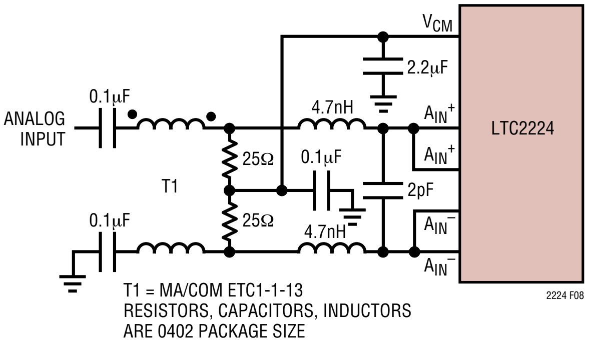


Figure 8. Recommended Front End Circuit for Input Frequencies Above 500MHz

The difference amplifier generates the high and low reference for the ADC. High speed switching circuits are connected to these outputs and they must be externally bypassed. Each output has four pins: two each of REFHA and REFHB for the high reference and two each of REFLA and REFLB for the low reference. The multiple output pins are needed to reduce package inductance. Bypass capacitors must be connected as shown in Figure 9.

Other voltage ranges in between the pin selectable ranges can be programmed with two external resistors as shown in Figure 10. An external reference can be used by applying its output directly or through a resistor divider to SENSE. It is not recommended to drive the SENSE pin with a logic device. The SENSE pin should be tied to the appropriate level as close to the converter as possible. If the SENSE pin is driven externally, it should be bypassed to ground as close to the device as possible with a 1µF ceramic capacitor.

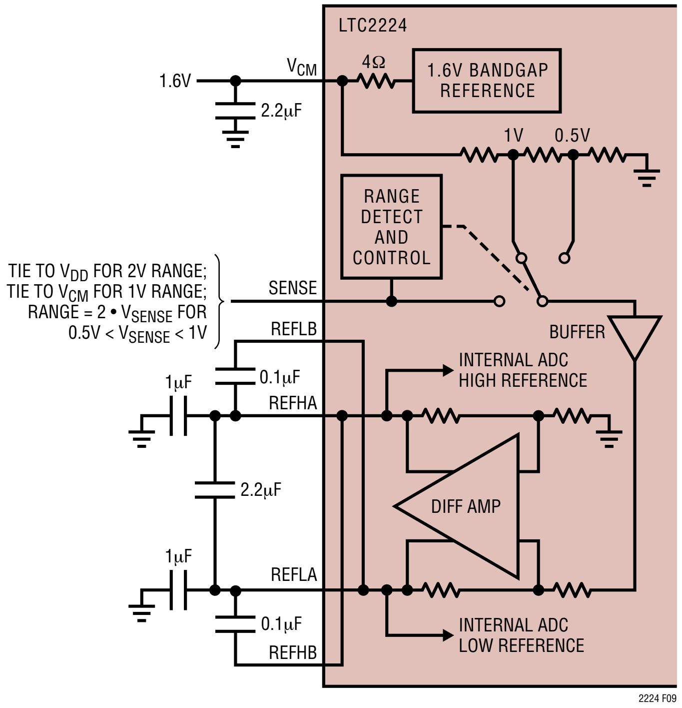


Figure 9. Equivalent Reference Circuit

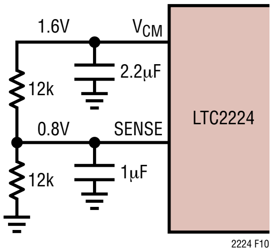


Figure 10. 1.6V Range ADC

APPLICATIONS INFORMATION

Input Range

The input range can be set based on the application. The 2V input range will provide the best signal-to-noise performance while maintaining excellent SFDR. The 1V input range will have better SFDR performance, but the SNR will degrade by 5dB. See the Typical Performance Characteristics section.

Driving the Encode Inputs

The noise performance of the LTC2224 can depend on the encode signal quality as much as on the analog input. The ENC$^+$/ENC$^-$ inputs are intended to be driven differentially, primarily for noise immunity from common mode noise sources. Each input is biased through a 6k resistor to a 1.6V bias. The bias resistors set the DC operating point for transformer coupled drive circuits and can set the logic threshold for single-ended drive circuits.

Any noise present on the encode signal will result in additional aperture jitter that will be RMS summed with the inherent ADC aperture jitter.

In applications where jitter is critical (high input frequencies) take the following into consideration:

1. Differential drive should be used.

2. Use as large an amplitude as possible; if transformer coupled use a higher turns ratio to increase the amplitude.

3. If the ADC is clocked with a sinusoidal signal, filter the encode signal to reduce wideband noise.

4. Balance the capacitance and series resistance at both encode inputs so that any coupled noise will appear at both inputs as common mode noise. The encode inputs have a common mode range of 1.1V to 2.5V. Each input may be driven from ground to V_{DD} for single-ended drive.

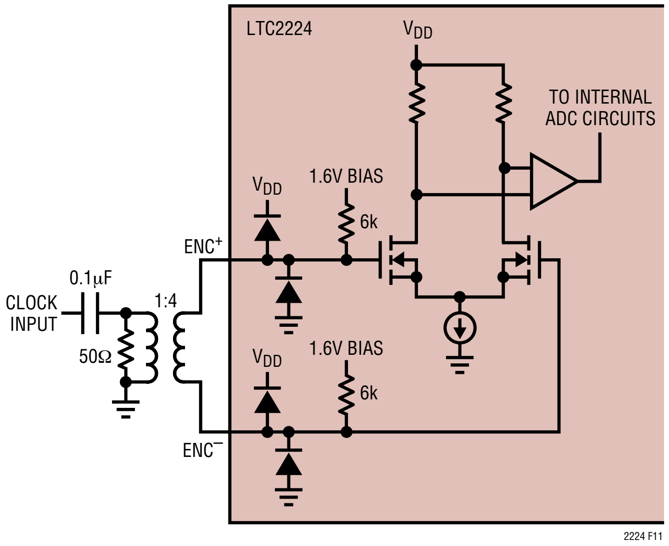


Figure 11. Transformer Driven ENC$^+$/ENC$^-$

Maximum and Minimum Encode Rates

The maximum encode rate for the LTC2224 is 135Msps. For the ADC to operate properly, the encode signal should have a 50% (±5%) duty cycle. Each half cycle must have at least 3.5ns for the ADC internal circuitry to have enough settling time for proper operation. Achieving a precise 50% duty cycle is easy with differential sinusoidal drive using a transformer or using symmetric differential logic such as PECL or LVDS.

An optional clock duty cycle stabilizer circuit can be used if the input clock has a non 50% duty cycle. This circuit uses the rising edge of the ENC$^+$ pin to sample the analog input. The falling edge of ENC$^+$ is ignored and the internal falling edge is generated by a phase-locked loop. The input clock duty cycle can vary from 30% to 70% and the clock duty cycle stabilizer will maintain a constant 50% internal duty cycle. If the clock is turned off for a long period of time, the duty cycle stabilizer circuit will require one hundred clock cycles for the PLL to lock onto the input clock. To use the clock duty cycle stabilizer, the MODE pin should be connected to $1/3V_{DD}$ or $2/3V_{DD}$ using external resistors.

The lower limit of the LTC2224 sample rate is determined by droop of the sample-and-hold circuits. The pipelined architecture of this ADC relies on storing analog signals on small valued capacitors. Junction leakage will discharge the capacitors. The specified minimum operating frequency for the LTC2224 is 1Msps.

APPLICATIONS INFORMATION

DIGITAL OUTPUTS

Digital Output Buffers

Figure 13 shows an equivalent circuit for a single output buffer. Each buffer is powered by OV_{DD} and OGND, which are isolated from the ADC power and ground. The additional N-channel transistor in the output driver allows operation down to voltages as low as 0.5V. The internal resistor in series with the output makes the output appear as 50Ω to external circuitry and may eliminate the need for external damping resistors.

As with all high speed/high resolution converters, the digital output loading can affect the performance. The digital outputs of the LTC2224 should drive a minimal capacitive load to avoid possible interaction between the digital outputs and sensitive input circuitry. For full speed operation the capacitive load should be kept under 5pF.

Lower OV_{DD} voltages will also help reduce interference from the digital outputs and improve the SNR.

Data Format

The LTC2224 parallel digital output can be selected for offset binary or 2's complement format. The format is selected with the MODE pin. Connecting MODE to GND or $1/3V_{DD}$ selects straight binary output format. Connecting MODE to $2/3V_{DD}$ or V_{DD} selects 2's complement output format. An external resistor divider can be used to set the $1/3V_{DD}$ or $2/3V_{DD}$ logic values. Table 1 shows the logic states for the MODE pin.

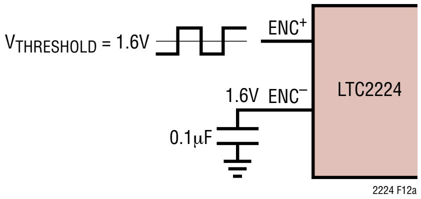


Figure 12a. Single-Ended ENC Drive, Not Recommended for Low Jitter

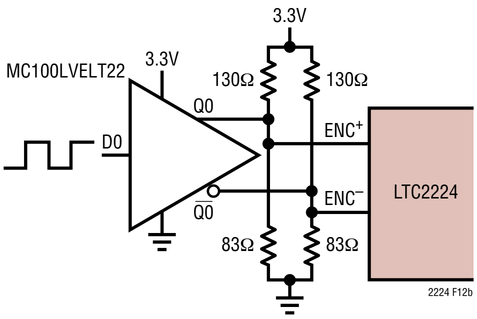


Figure 12b. ENC Drive Using a CMOS to PECL Translator

Table 1. MODE Pin Function

MODE Pin	Output Format	Clock Duty Cycle Stablizer
0	Straight Binary	Off
$1/3V_{DD}$	Straight Binary	On
$2/3V_{DD}$	2's Complement	On
V_{DD}	2's Complement	Off

Overflow Bit

The converter is either overranged or underranged when OF outputs a logic high.

Output Clock

The ADC has a delayed version of the ENC^+ input available as a digital output, CLOCKOUT. The CLOCKOUT pin can be used to synchronize the converter data to the digital system. This is necessary when using a sinusoidal encode. Data will be updated just after CLOCKOUT rises and can be latched on the falling edge of CLOCKOUT.

Output Driver Power

Separate output power and ground pins allow the output drivers to be isolated from the analog circuitry. The power supply for the digital output buffers, OV_{DD}, should be tied

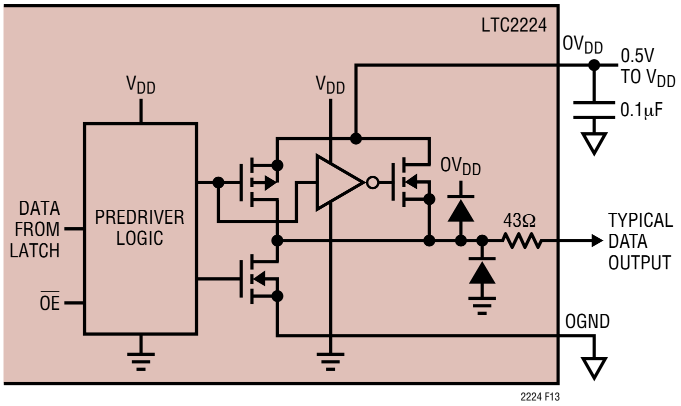


Figure 13. Digital Output Buffer

APPLICATIONS INFORMATION

to the same power supply as for the logic being driven. For example if the converter is driving a DSP powered by a 1.8V supply then OV_{DD} should be tied to that same 1.8V supply.

OV_{DD} can be powered with any voltage up to the V_{DD} of the part. OGND can be powered with any voltage from GND up to 1V and must be less than OV_{DD}. The logic outputs will swing between OGND and OV_{DD}.

Output Enable

The outputs may be disabled with the output enable pin, $\overline{\text{OE}}$. $\overline{\text{OE}}$ high disables all data outputs including OF and CLOCKOUT. The data access and bus relinquish times are too slow to allow the outputs to be enabled and disabled during full speed operation. The output Hi-Z state is intended for use during long periods of inactivity.

Sleep and Nap Modes

The converter may be placed in shutdown or nap modes to conserve power. Connecting SHDN to GND results in normal operation. Connecting SHDN to V_{DD} and $\overline{\text{OE}}$ to V_{DD} results in sleep mode, which powers down all circuitry including the reference and typically dissipates 1mW. When exiting sleep mode it will take milliseconds for the output data to become valid because the reference capacitors have to recharge and stabilize. Connecting SHDN to V_{DD} and $\overline{\text{OE}}$ to GND results in nap mode, which typically dissipates 35mW. In nap mode, the on-chip reference circuit is kept on, so that recovery from nap mode is faster than that from sleep mode, typically taking 100 clock cycles. In both sleep and nap mode all digital outputs are disabled and enter the Hi-Z state.

GROUNDING AND BYPASSING

The LTC2224 requires a printed circuit board with a clean unbroken ground plane. A multilayer board with an internal ground plane is recommended. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital signal alongside an analog signal or underneath the ADC.

High quality ceramic bypass capacitors should be used at the V_{DD}, OV_{DD}, V_{CM}, REFHA, REFHB, REFLA and REFLB pins as shown in the block diagram on the front page of this data sheet. Bypass capacitors must be located as close to the pins as possible. Of particular importance are the capacitors between REFHA and REFLB and between REFHB and REFLA. These capacitors should be as close to the device as possible (1.5mm or less). Size 0402 ceramic capacitors are recommended. The 2.2μF capacitor between REFHA and REFLA can be somewhat further away. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

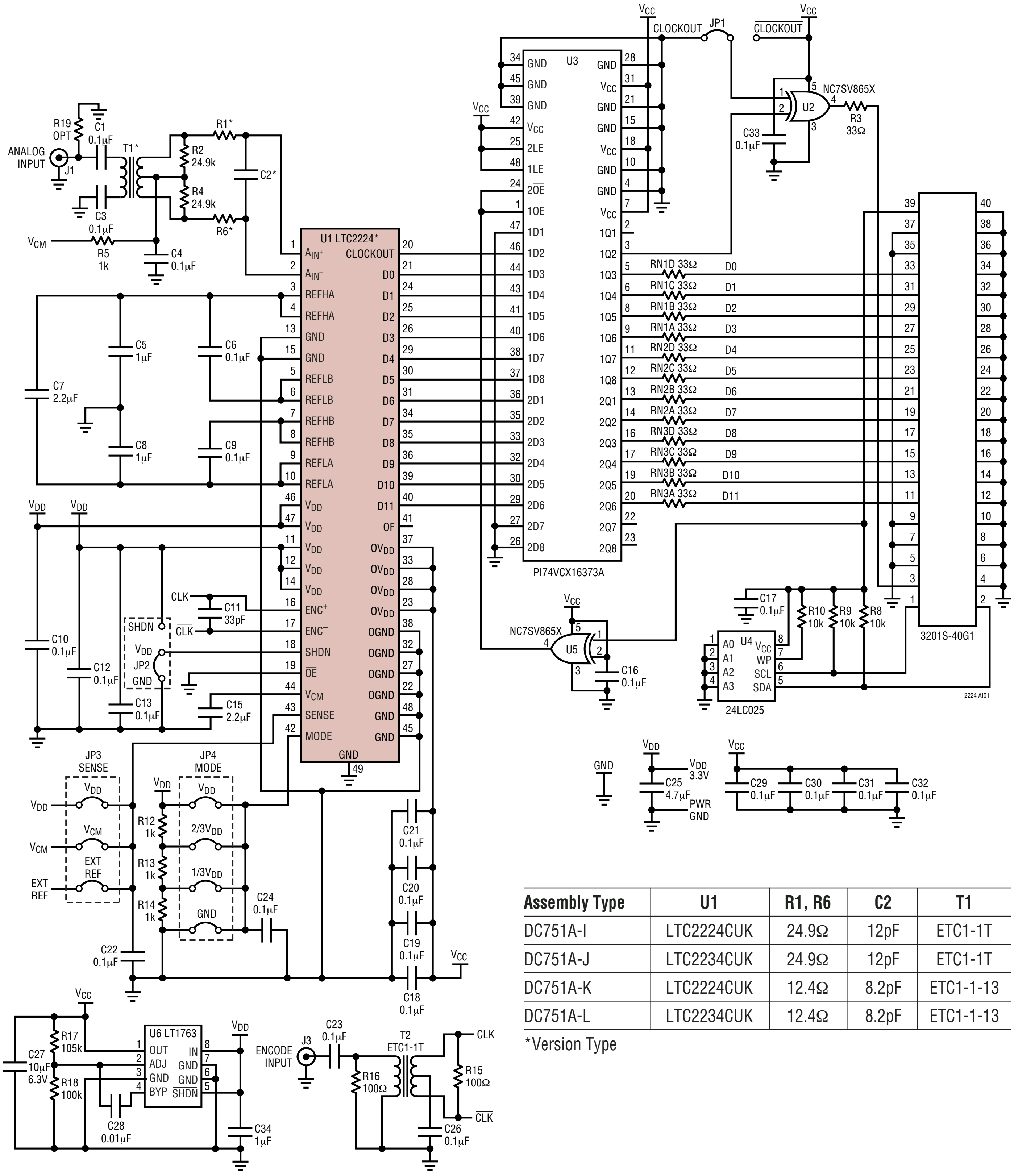
The LTC2224 differential inputs should run parallel and close to each other. The input traces should be as short as possible to minimize capacitance and to minimize noise pickup.

HEAT TRANSFER

Most of the heat generated by the LTC2224 is transferred from the die through the bottom-side exposed pad and package leads onto the printed circuit board. For good electrical and thermal performance, the exposed pad should be soldered to a large grounded pad on the PC board. It is critical that all ground pins are connected to a ground plane of sufficient area.

APPLICATIONS INFORMATION

Evaluation Circuit Schematic of the LTC2224

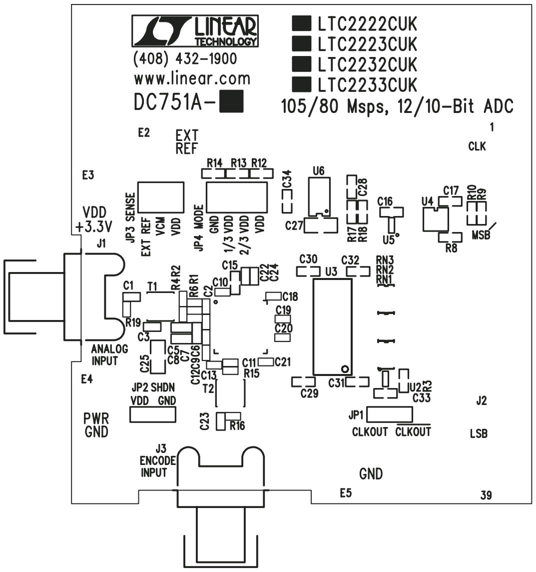


Assembly Type	U1	R1, R6	C2	T1
DC751A-I	LTC2224CUK	24.9Ω	12pF	ETC1-1T
DC751A-J	LTC2234CUK	24.9Ω	12pF	ETC1-1T
DC751A-K	LTC2224CUK	12.4Ω	8.2pF	ETC1-1-13
DC751A-L	LTC2234CUK	12.4Ω	8.2pF	ETC1-1-13

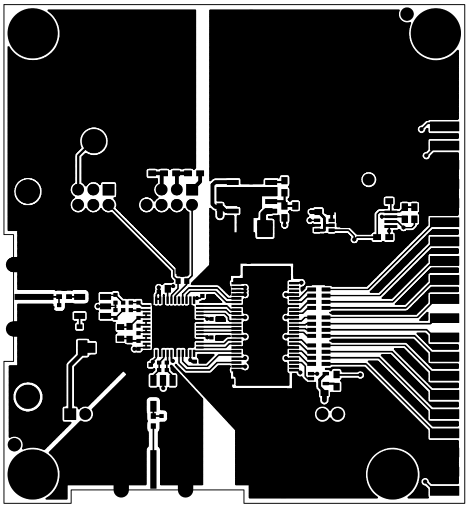
*Version Type

APPLICATIONS INFORMATION

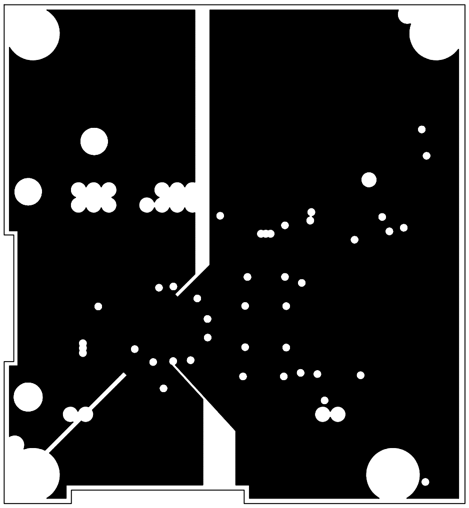
Silkscreen Top



Layer 1 Component Side

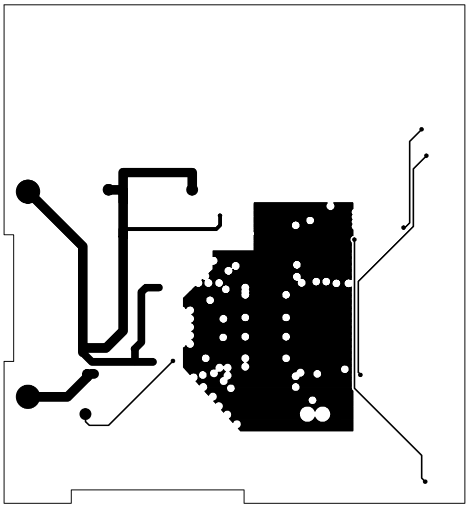


Layer 2 GND Plane

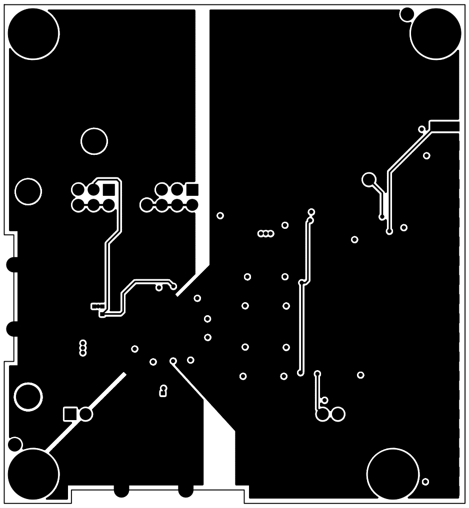


APPLICATIONS INFORMATION

Layer 3 Power Plane

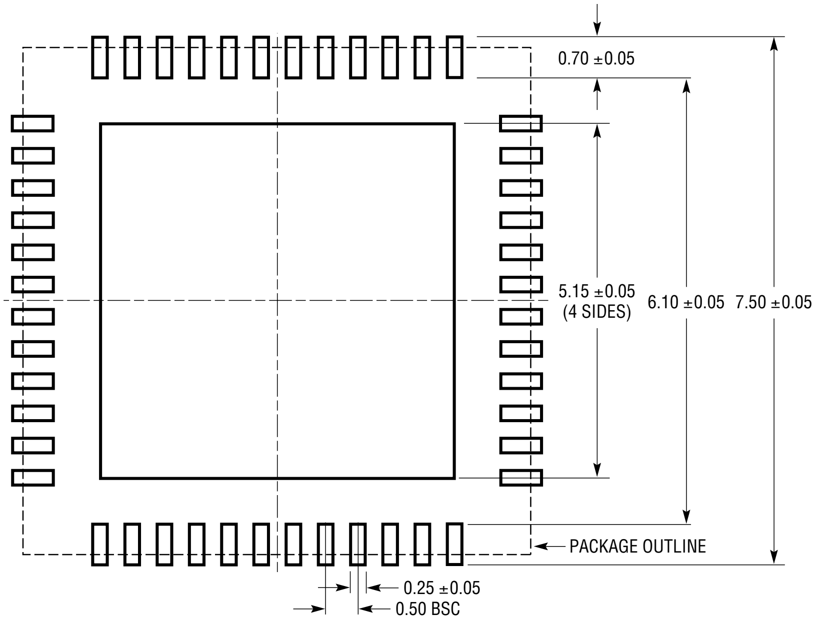


Layer 4 Bottom Side



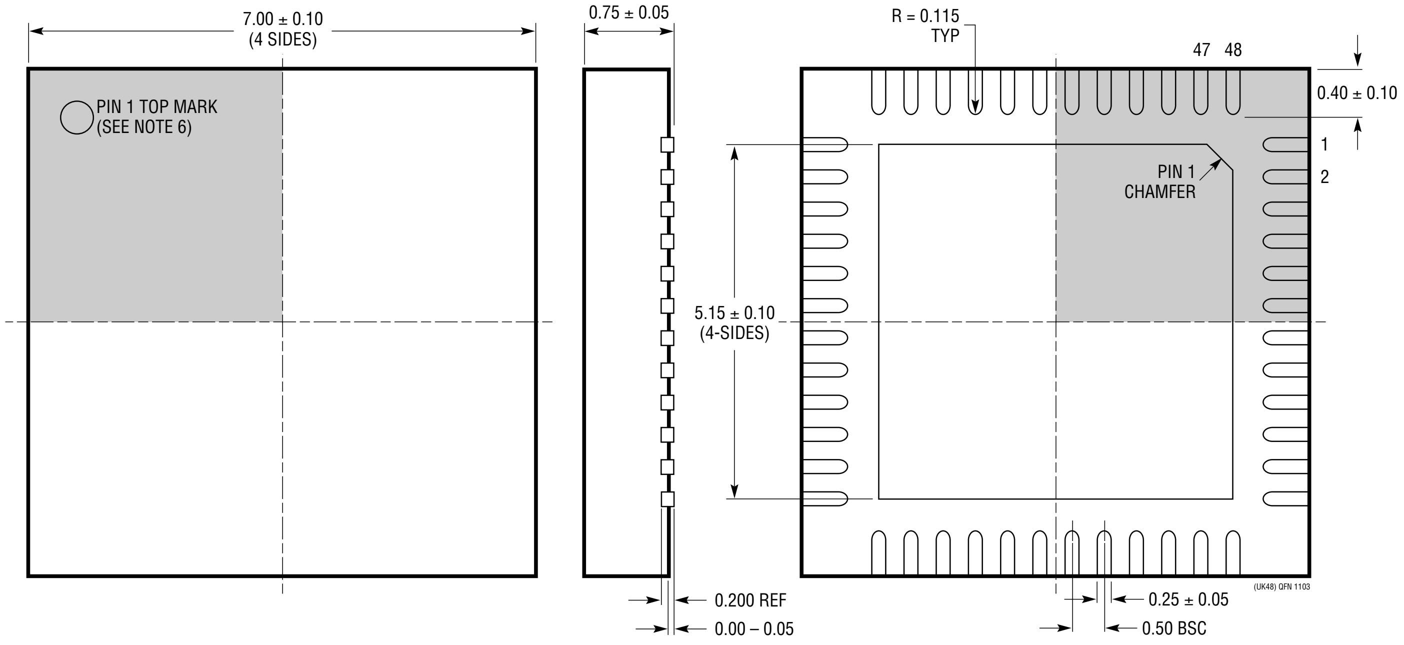
PACKAGE DESCRIPTION

UK Package
48-Lead Plastic QFN (7mm × 7mm)
(Reference LTC DWG # 05-08-1704)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WKKD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE



BOTTOM VIEW—EXPOSED PAD

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1741	12-Bit, 65Msps ADC	72dB SNR, 87dB SFDR, 48-Pin TSSOP Package
LTC1742	14-Bit, 65Msps ADC	76.5dB SNR, 90dB SFDR, 48-Pin TSSOP Package
LTC1743	12-Bit, 50Msps ADC	72.5dB SNR, 90dB SFDR, 48-Pin TSSOP Package
LTC1744	14-Bit, 50Msps ADC	77dB SNR, 90dB SFDR, 48-Pin TSSOP Package
LTC1745	12-Bit, 25Msps ADC	72.5dB SNR, 380mW, 48-Pin TSSOP Package
LTC1746	14-Bit, 25Msps ADC	77.5dB SNR, 390mW, 48-Pin TSSOP Package
LTC1747	12-Bit, 80Msps ADC	72dB SNR, 87dB SFDR, 48-Pin TSSOP Package
LTC1748	14-Bit, 80Msps ADC	76.3dB SNR, 90dB SFDR, 48-Pin TSSOP Package
LTC1749	12-Bit, 80Msps Wideband ADC	Up to 500MHz IF Undersampling, 87dB SFDR
LTC1750	14-Bit, 80Msps Wideband ADC	Up to 500MHz IF Undersampling, 90dB SFDR
LTC2220	12-Bit, 170Msps ADC	890mW, 67.5dB SNR, 9mm x 9mm QFN Package
LTC2221	12-Bit, 135Msps ADC	660mW, 67.5dB SNR, 9mm x 9mm QFN Package
LTC2230	10-Bit, 170Msps ADC	890mW, 61dB SNR, 9mm x 9mm QFN Package
LTC2231	10-Bit, 135Msps ADC	660mW, 61dB SNR, 9mm x 9mm QFN Package
LTC2232	10-Bit, 105Msps ADC	475mW, 61dB SNR, 7mm x 7mm QFN Package
LTC2233	10-Bit, 80Msps ADC	366mW, 61dB SNR, 7mm x 7mm QFN Package
LTC2234	10-Bit, 135Msps ADC	630mW, 61dB SNR, 7mm x 7mm QFN Package
LT5512	DC-3GHz High Signal Level Downconverting Mixer	DC to 3GHz, 21dBm IIP3, Integrated LO Buffer
LT5514	Ultralow Distortion IF Amplifier/ADC Driver with Digitally Controlled Gain	450MHz 1dB BW, 47dB OIP3, Digital Gain Control 10.5dB to 33dB in 1.5dB/Step
LT5515	1.5GHz to 2.5GHz Direct Conversion Quadrature Demodulator	20dBm IIP3, Integrated LO Quadrature Generator
LT5516	0.8GHz to 1.5GHz Direct Conversion Quadrature Demodulator	21.5dBm IIP3, Integrated LO Quadrature Generator
LT5517	40MHz to 900MHz Direct Conversion Quadrature Demodulator	21dBm IIP3, Integrated LO Quadrature Generator
LT5522	600MHz to 2.7GHz High Linearity Downconverting Mixer	4.5V to 5.25V Supply, 25dBm IIP3 at 900MHz, NF = 12.5dB, 500Ω Single-Ended RF and LO Ports

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