



BUK9880-55

N-channel TrenchMOS logic level FET

19 March 2014

Product data sheet

1. General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

2. Features and benefits

- AEC Q101 compliant
- Electrostatically robust due to integrated protection diodes
- Low conduction losses due to low on-state resistance

3. Applications

- Automotive and general purpose power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	-	55	V
I_D	drain current	$T_{sp} = 25\text{ °C}$	-	-	7.5	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; Fig. 4	-	-	8.3	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 5\text{ A}$; $T_j = 25\text{ °C}$	-	65	80	m Ω
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 2.5\text{ A}$; $V_{sup} \leq 25\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 5\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped	-	-	30	mJ

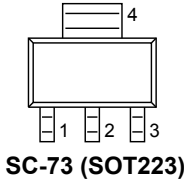
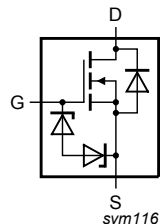


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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>SC-73 (SOT223)</p>	 <p>sym116</p>
2	D	drain		
3	S	source		
4	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9880-55	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223
BUK9880-55/CU	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9880-55	
BUK9880-55/CU	98055

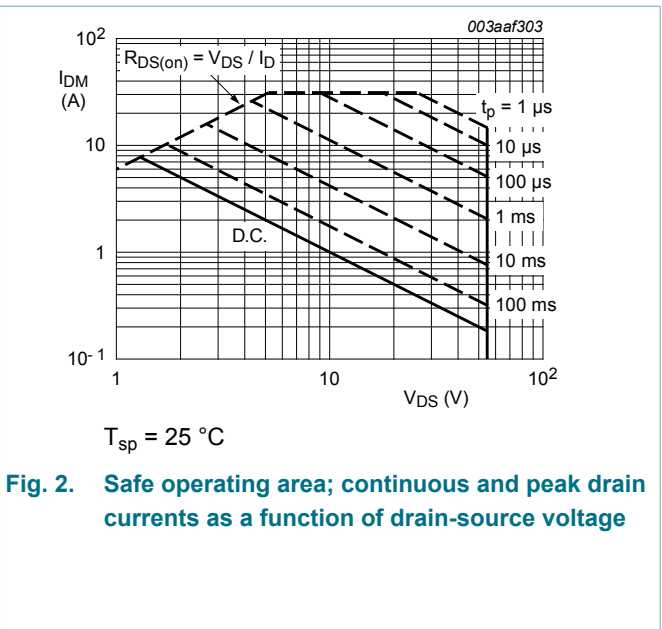
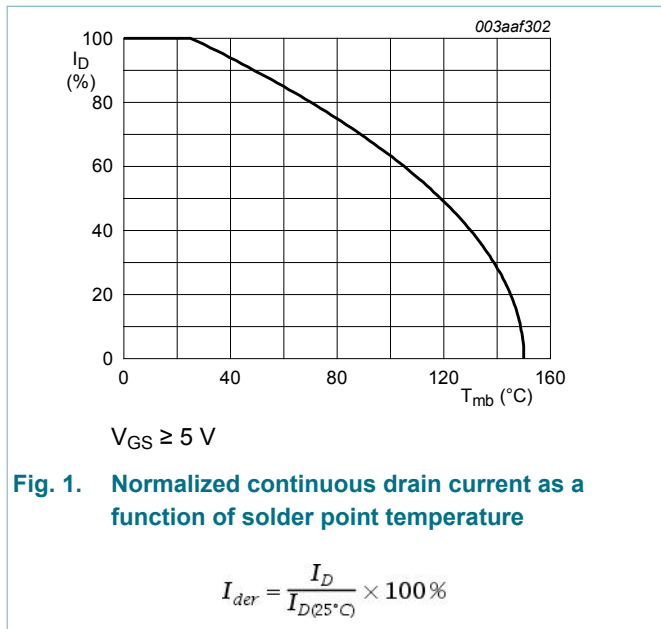
8. Limiting values

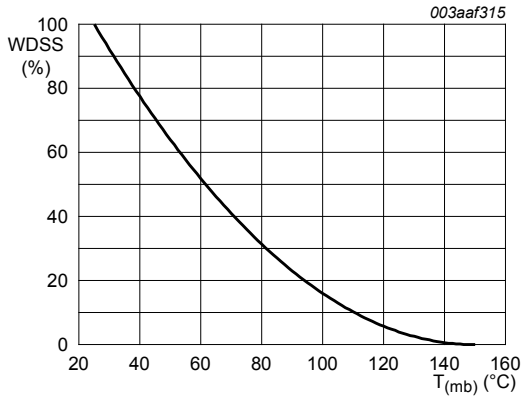
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	55	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	55	V
V_{GS}	gate-source voltage		-10	10	V
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; Fig. 4	-	8.3	W
I_D	drain current	$T_{sp} = 25\text{ °C}$	-	7.5	A
		$T_{sp} = 100\text{ °C}$	-	4.7	A

Symbol	Parameter	Conditions	Min	Max	Unit
I_{DM}	peak drain current	$T_{sp} = 25\text{ }^{\circ}\text{C}$; pulsed	-	40	A
T_{stg}	storage temperature		-55	150	$^{\circ}\text{C}$
T_j	junction temperature		-55	150	$^{\circ}\text{C}$
V_{esd}	electrostatic discharge voltage	HBM; C = 100 pF; R = 1.5 k Ω	-	2	kV
Source-drain diode					
I_S	source current	$T_{sp} = 25\text{ }^{\circ}\text{C}$	-	7.5	A
I_{SM}	peak source current	pulsed; $T_{sp} = 25\text{ }^{\circ}\text{C}$	-	40	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 2.5\text{ A}$; $V_{sup} \leq 25\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 5\text{ V}$; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; unclamped	-	30	mJ





$I_D = 2.5 \text{ A}$

Fig. 3. Normalised drain-source non-repetitive avalanche energy as a function of mounting-base temperature

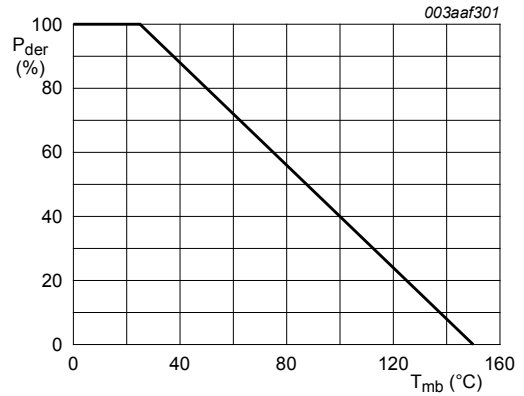


Fig. 4. Normalized total power dissipation as a function of solder point temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100 \%$$

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	mounted on any printed-circuit board	-	12	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on printed-circuit board	-	120	-	K/W

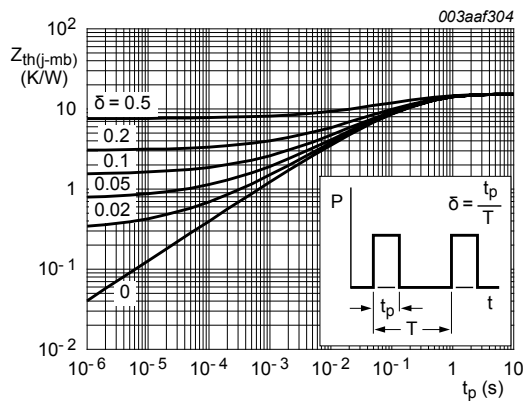


Fig. 5. Transient thermal impedance from junction to solder point as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	50	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	55	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	1	1.5	2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C}$	-	-	2.3	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C}$	0.6	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.05	10	μA
		$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	1	μA
		$V_{GS} = -5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	1	μA
		$V_{GS} = 5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	5	μA
		$V_{GS} = -5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	5	μA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 150 \text{ }^\circ\text{C}$	-	-	148	$\text{m}\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	65	80	$\text{m}\Omega$
$V_{(BR)GSS}$	gate-source breakdown voltage	$V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}; I_G = 1 \text{ mA}$	10	-	-	V
		$V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}; I_G = -1 \text{ mA}$	10	-	-	V
Dynamic characteristics						
C_{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$	-	500	650	pF
C_{oss}	output capacitance		-	110	135	pF
C_{rss}	reverse transfer capacitance		-	60	85	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 4.29 \text{ } \Omega; V_{GS} = 5 \text{ V}; R_{G(ext)} = 10 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}; I_D = 7 \text{ A}$	-	10	15	ns
t_r	rise time		-	30	50	ns
$t_{d(off)}$	turn-off delay time		-	30	45	ns
t_f	fall time		-	30	40	ns
g_{fs}	transfer conductance	$V_{DS} = 25 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	4	8	-	S
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 5 \text{ A}; V_{GS} = 0 \text{ V}; T_j \geq -55 \text{ }^\circ\text{C}; T_j \leq 175 \text{ }^\circ\text{C}$	-	0.85	1.1	V
t_{rr}	reverse recovery time	$I_S = 5 \text{ A}; di_S/dt = -100 \text{ A}/\mu\text{s};$	-	38	-	ns
Q_r	recovered charge	$V_{GS} = -10 \text{ V}; V_{DS} = 30 \text{ V}; T_j \leq 175 \text{ }^\circ\text{C}$	-	0.2	-	μC

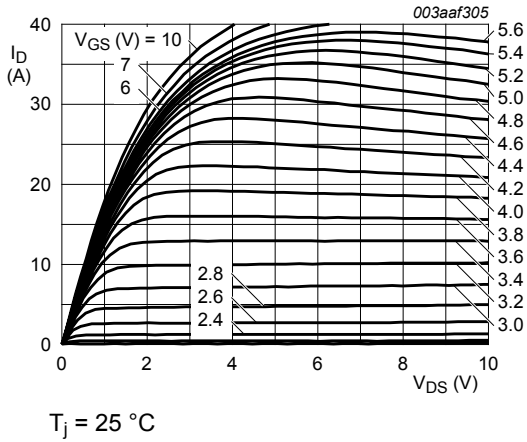


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

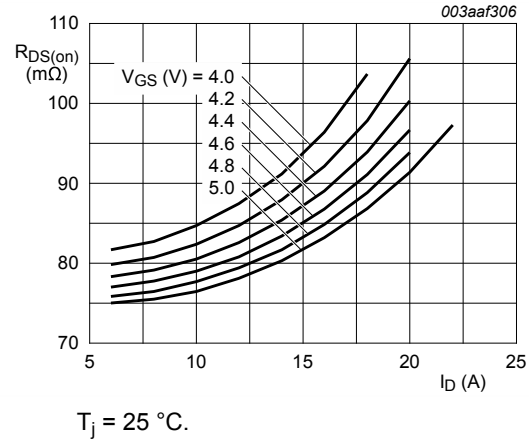


Fig. 7. Drain-source on-state resistance as a function of drain current; typical values

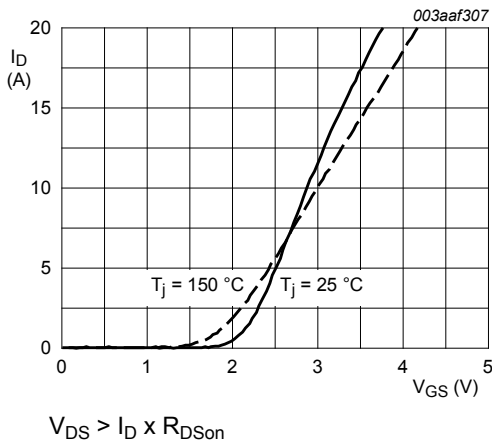


Fig. 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values

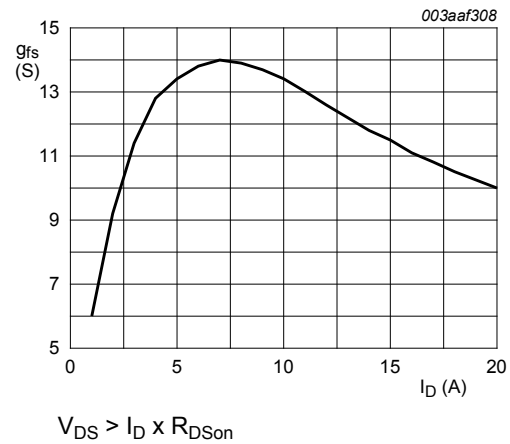


Fig. 9. Forward transconductance as a function of drain current; typical values

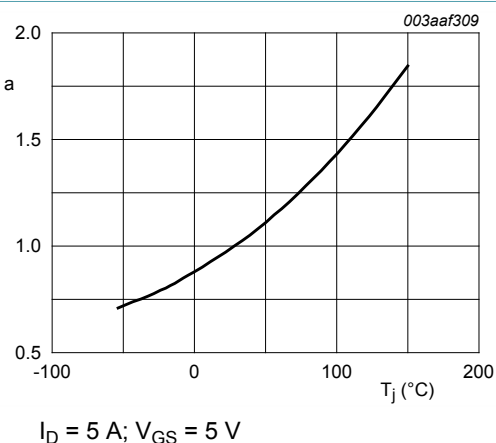


Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon@25^{\circ}C}}$$

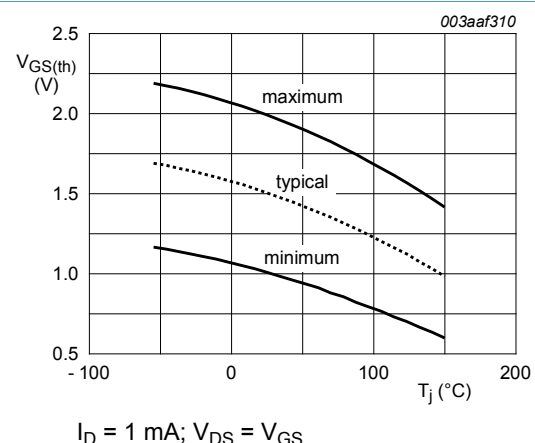


Fig. 11. Gate-source threshold voltage as a function of junction temperature

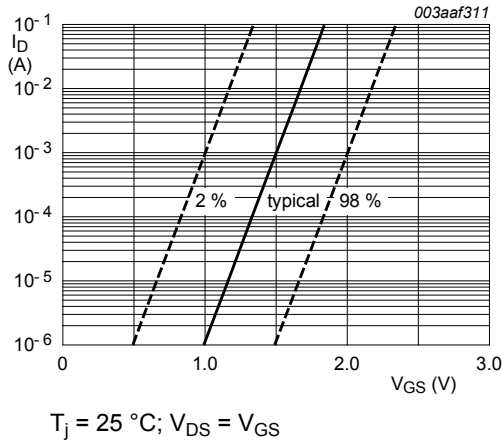


Fig. 12. Sub-threshold drain current as a function of gate-source voltage

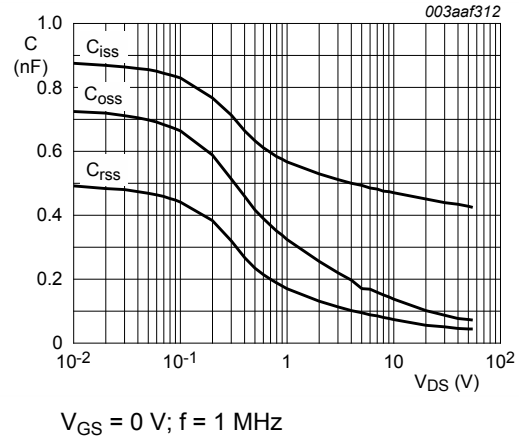


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

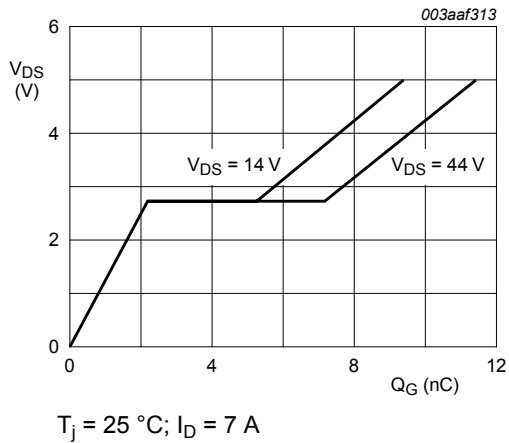


Fig. 14. Gate-source voltage as a function of gate charge; typical values

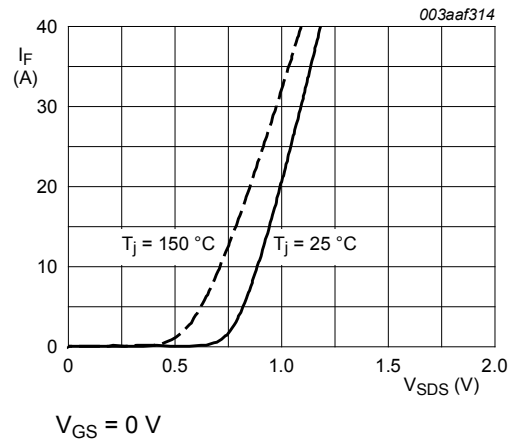


Fig. 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

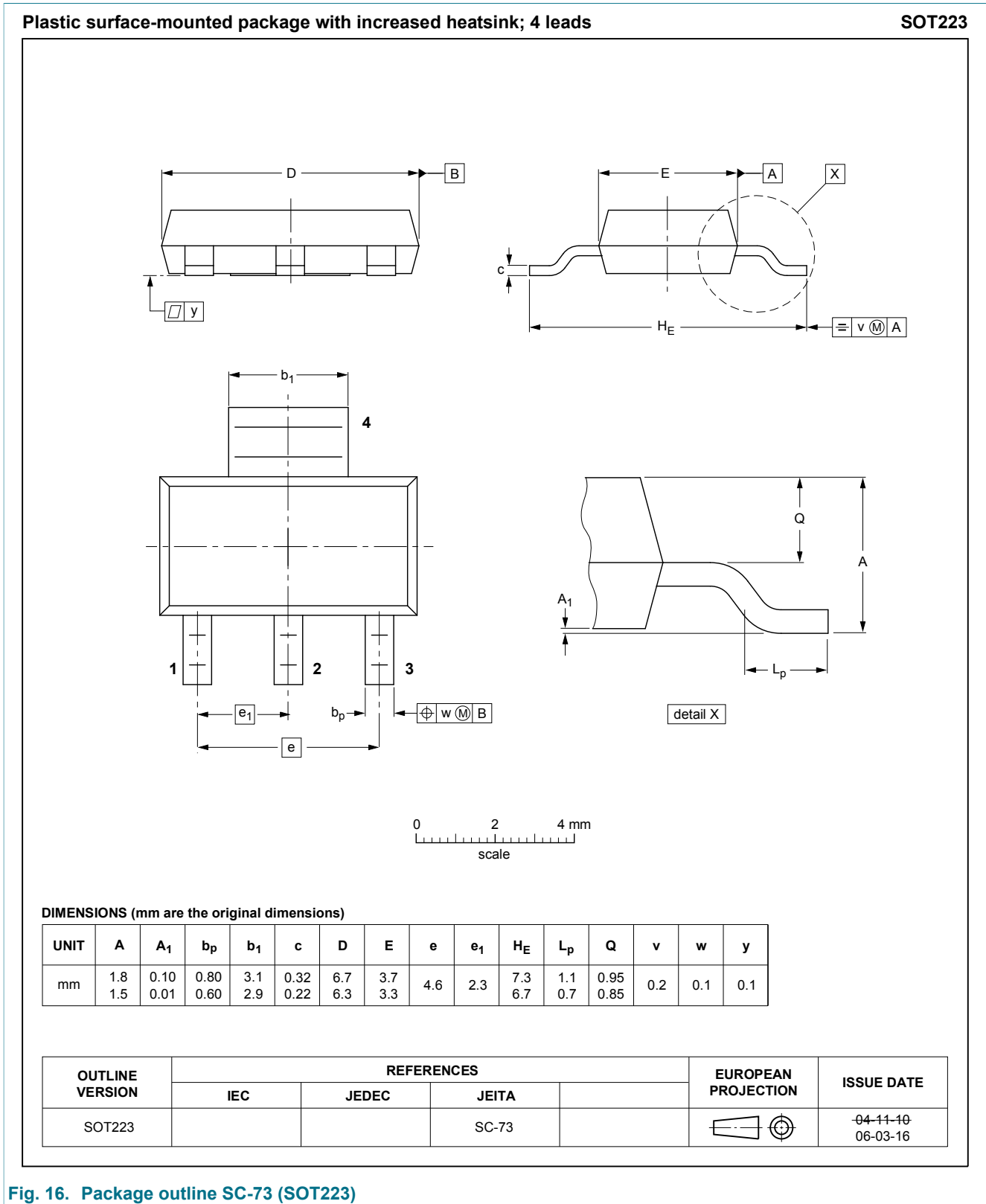


Fig. 16. Package outline SC-73 (SOT223)

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