

# EC103D1

Thyristor, sensitive gate

Rev. 02 — 31 July 2008

Product data sheet

## 1. Product profile

### 1.1 General description

Passivated ultra sensitive gate thyristor in a SOT54 plastic package.

### 1.2 Features

- Ultra sensitive gate
- Direct interfacing to low power gate trigger circuits

### 1.3 Applications

- Earth leakage circuit breakers or Ground Fault Circuit Interrupters (GFCI)
- Solid state relays
- General purpose switching
- Small engine ignition

### 1.4 Quick reference data

- $V_{DRM} \leq 400 \text{ V}$
- $V_{RRM} \leq 400 \text{ V}$
- $I_{TSM} \leq 8 \text{ A}$  ( $t = 10 \text{ ms}$ )
- $I_{T(RMS)} \leq 0.8 \text{ A}$
- $I_{GT} \leq 12 \mu\text{A}$

## 2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	anode (A)		
2	gate (G)		
3	cathode (K)		

**SOT54 (TO-92)**

### 3. Ordering information

**Table 2. Ordering information**

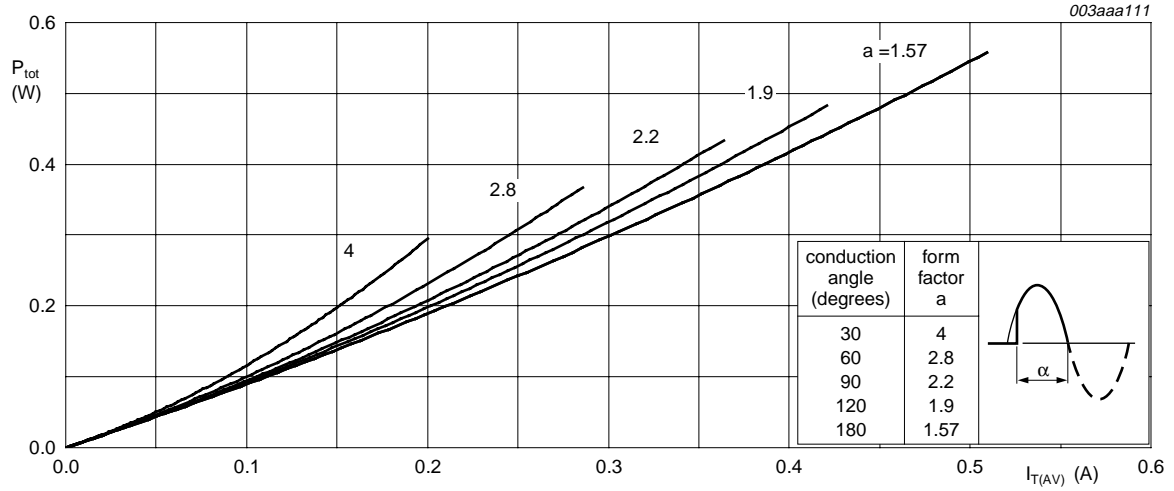
Type number	Package		Version
	Name	Description	
EC103D1	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

### 4. Limiting values

**Table 3. Limiting values**

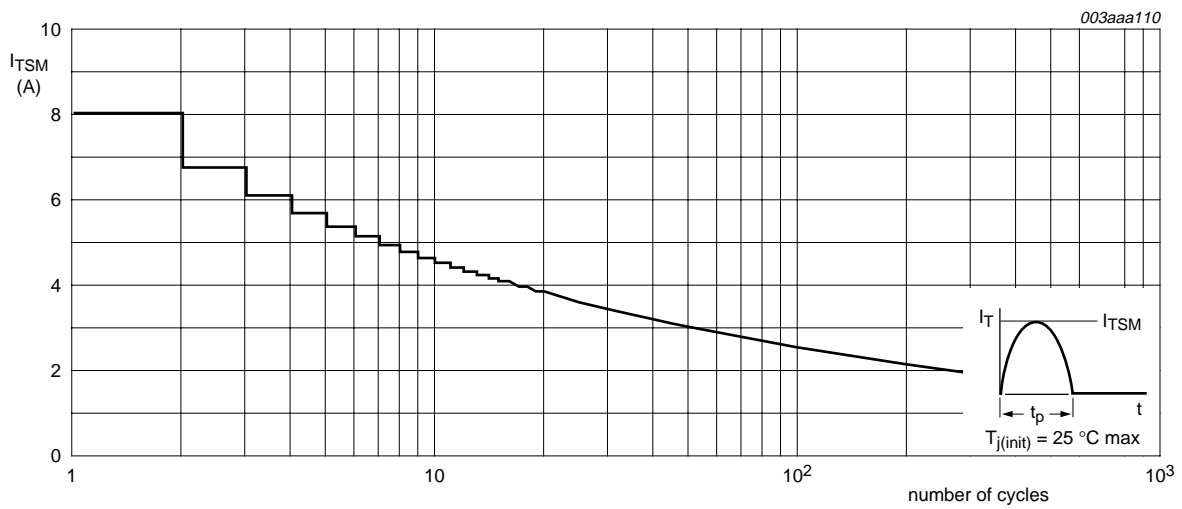
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	400	V
$V_{RRM}$	repetitive peak reverse voltage		-	400	V
$V_{DSM}$	non-repetitive peak off-state voltage		-	450	V
$V_{RSM}$	non-repetitive peak reverse voltage		-	450	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{lead} \leq 92\text{ °C}$ ; see <a href="#">Figure 1</a>	-	0.5	A
$I_{T(RMS)}$	RMS on-state current	all conduction angles; see <a href="#">Figure 4</a> and <a href="#">5</a>	-	0.8	A
$I_{TSM}$	non-repetitive peak on-state current	half sine wave; $T_j = 25\text{ °C}$ prior to surge; see <a href="#">Figure 2</a> and <a href="#">3</a>			
		$t = 10\text{ ms}$	-	8	A
		$t = 8.3\text{ ms}$	-	9	A
$I^2t$	$I^2t$ for fusing	$t_p = 10\text{ ms}$	-	0.32	A <sup>2</sup> s
$di_T/dt$	rate of rise of on-state current	$I_{TM} = 2\text{ A}$ ; $I_G = 10\text{ mA}$ ; $di_G/dt = 0.1\text{ A}/\mu\text{s}$	-	50	A/ $\mu\text{s}$
$I_{GM}$	peak gate current		-	1	A
$V_{RGM}$	peak reverse gate voltage		-	5	V
$P_{GM}$	peak gate power		-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
$T_{stg}$	storage temperature		-40	+150	°C
$T_j$	junction temperature		-	125	°C



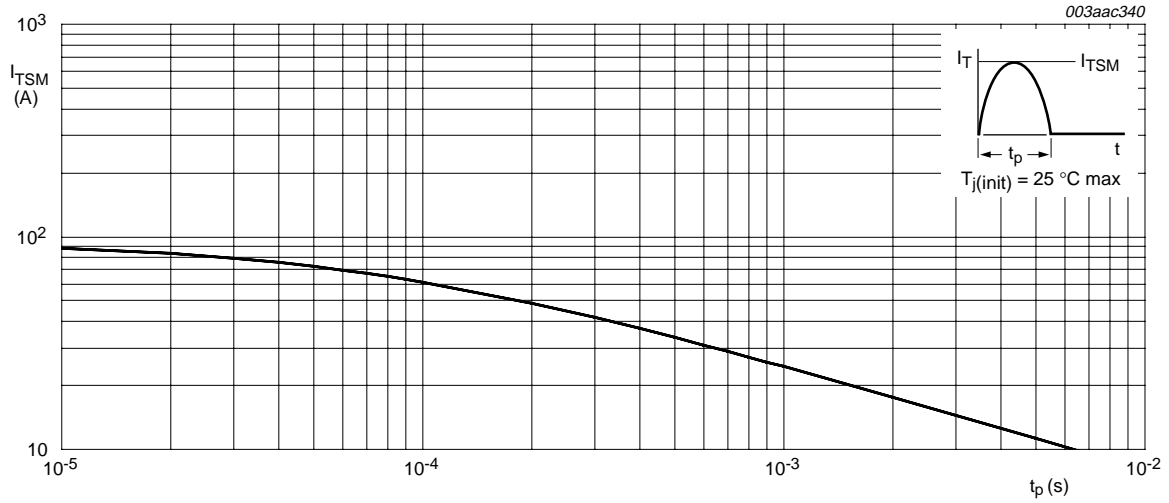
Form factor  $a = I_{T(RMS)} / I_{T(AV)}$

Fig 1. Total power dissipation as a function of average on-state current; maximum values



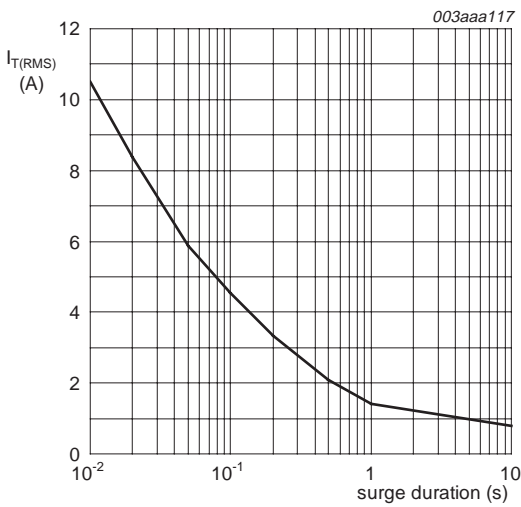
f = 50 Hz

Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



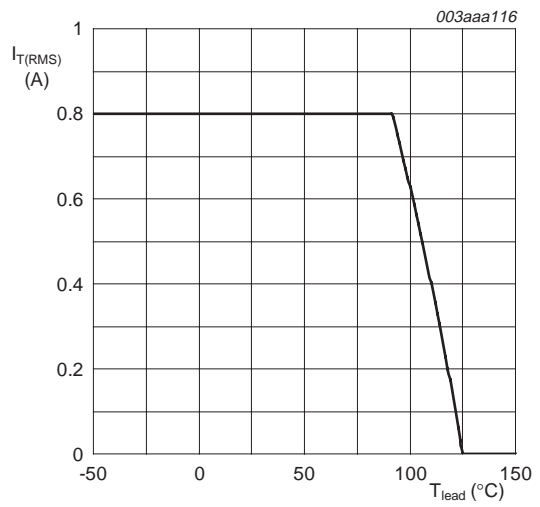
$t_p \leq 10\text{ ms}$

**Fig 3. Non-repetitive peak on-state current as a function of pulse duration; maximum values**



$f = 50\text{ Hz}$   
 $T_{lead} = 92\text{ °C}$

**Fig 4. RMS on-state current as a function of surge duration; maximum values**



**Fig 5. RMS on-state current as a function of lead temperature; maximum values**

### 5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	see <a href="#">Figure 6</a>	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	printed-circuit board mounted; lead length 4 mm	-	150	-	K/W

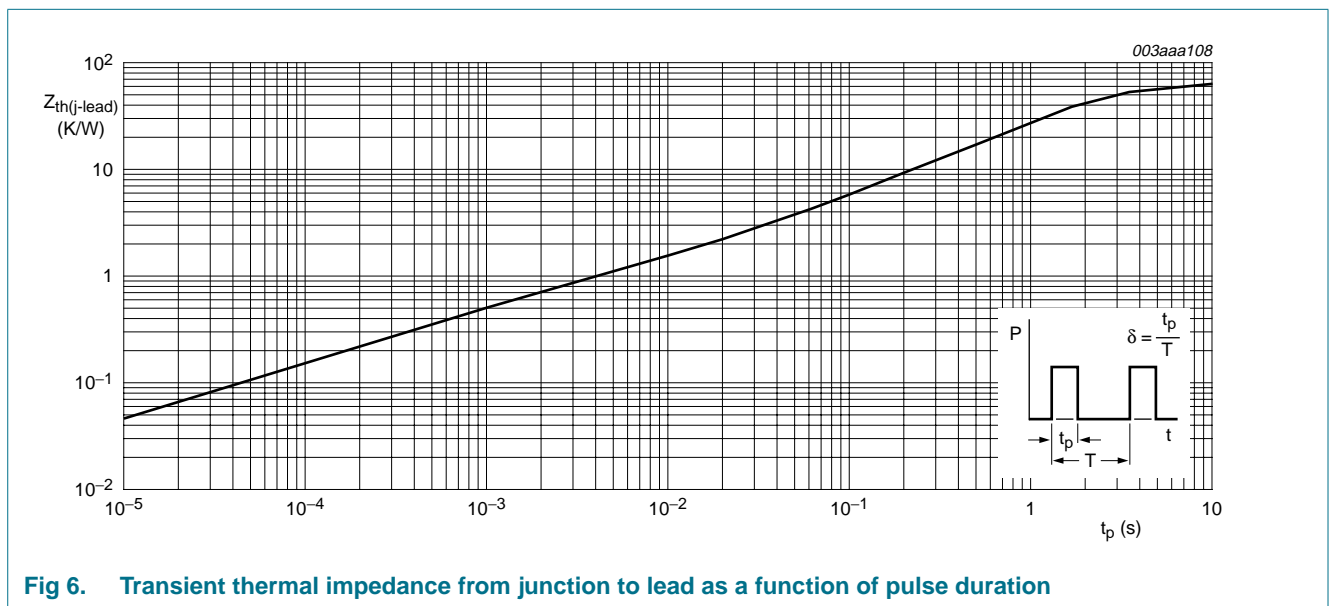


Fig 6. Transient thermal impedance from junction to lead as a function of pulse duration

## 6. Characteristics

**Table 5. Characteristics**

$T_j = 25\text{ °C}$  unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; see <a href="#">Figure 8</a>	-	3	12	$\mu\text{A}$
$I_L$	latching current	$V_D = 12\text{ V}$ ; $I_{GT} = 0.5\text{ mA}$ ; $R_{GK} = 1\text{ k}\Omega$ ; see <a href="#">Figure 10</a>	-	2	6	$\text{mA}$
$I_H$	holding current	$V_D = 12\text{ V}$ ; $I_{GT} = 0.5\text{ mA}$ ; $R_{GK} = 1\text{ k}\Omega$ ; see <a href="#">Figure 11</a>	-	2	5	$\text{mA}$
$V_T$	on-state voltage	$I_T = 1\text{ A}$	-	1.2	1.35	$\text{V}$
$V_{GT}$	gate trigger voltage	$I_T = 10\text{ mA}$ ; see <a href="#">Figure 7</a>				
		$V_D = 12\text{ V}$	-	0.5	0.8	$\text{V}$
		$V_D = V_{DRM(max)}$ ; $T_j = 125\text{ °C}$	0.2	0.3	-	$\text{V}$
$I_D$	off-state current	$V_D = V_{DRM(max)}$ ; $T_j = 125\text{ °C}$ ; $R_{GK} = 1\text{ k}\Omega$	-	0.05	0.1	$\text{mA}$
$I_R$	reverse current	$V_R = V_{RRM(max)}$ ; $T_j = 125\text{ °C}$ ; $R_{GK} = 1\text{ k}\Omega$	-	0.05	0.1	$\text{mA}$
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 0.67 \times V_{DRM(max)}$ ; $T_j = 125\text{ °C}$ ; exponential waveform; $R_{GK} = 1\text{ k}\Omega$ ; see <a href="#">Figure 12</a>	-	150	-	$\text{V}/\mu\text{s}$
$t_{gt}$	gate-controlled turn-on time	$I_{TM} = 2\text{ A}$ ; $V_D = V_{DRM(max)}$ ; $I_G = 10\text{ mA}$ ; $dI_G/dt = 0.1\text{ A}/\mu\text{s}$	-	2	-	$\mu\text{s}$
$t_q$	commutated turn-off time	$V_{DM} = 0.67 \times V_{DRM(max)}$ ; $T_j = 125\text{ °C}$ ; $I_{TM} = 1.6\text{ A}$ ; $V_R = 35\text{ V}$ ; $(dI_T/dt)_M = 30\text{ A}/\mu\text{s}$ ; $dV_D/dt = 2\text{ V}/\mu\text{s}$ ; $R_{GK} = 1\text{ k}\Omega$	-	100	-	$\mu\text{s}$

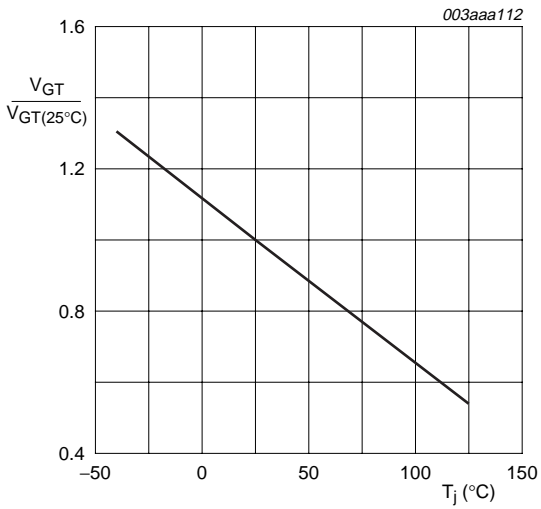


Fig 7. Normalized gate trigger voltage as a function of junction temperature

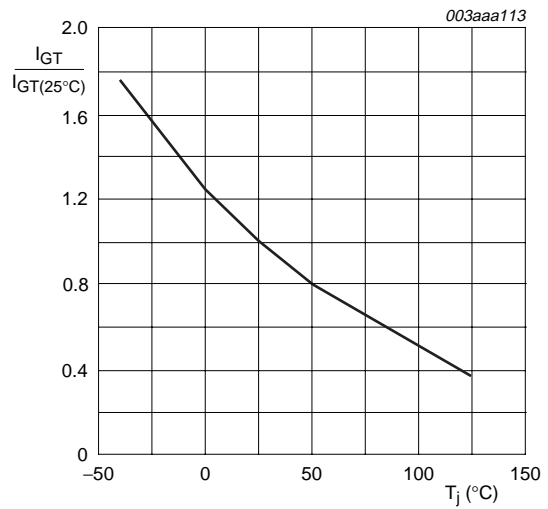
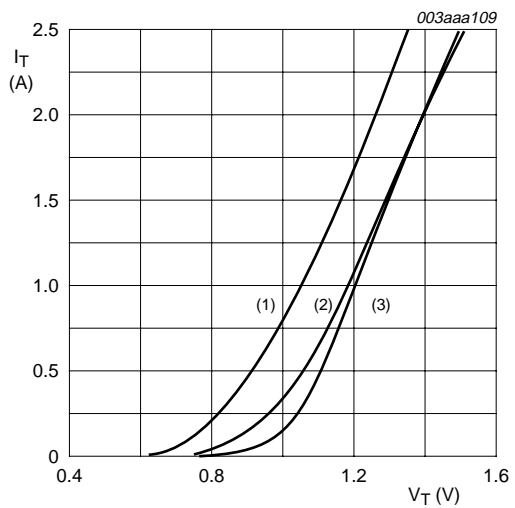
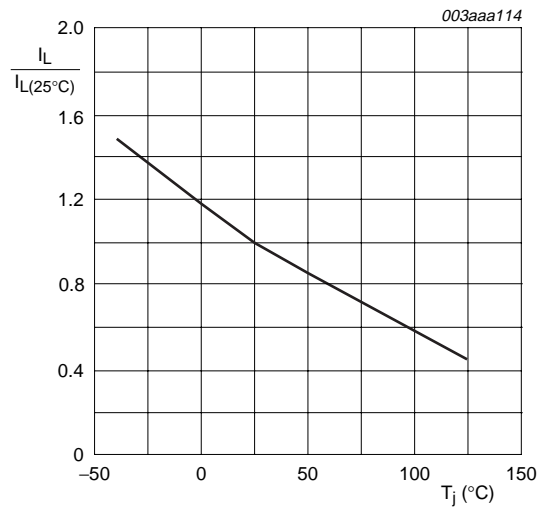


Fig 8. Normalized gate trigger current as a function of junction temperature



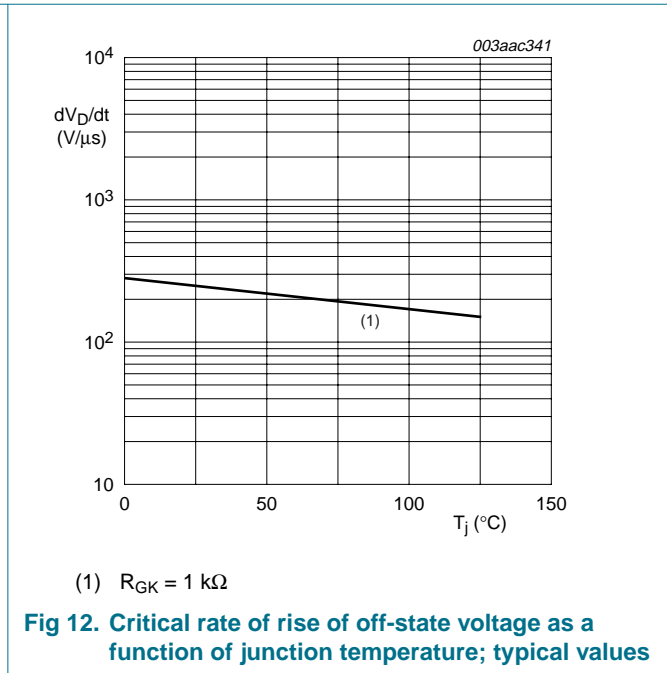
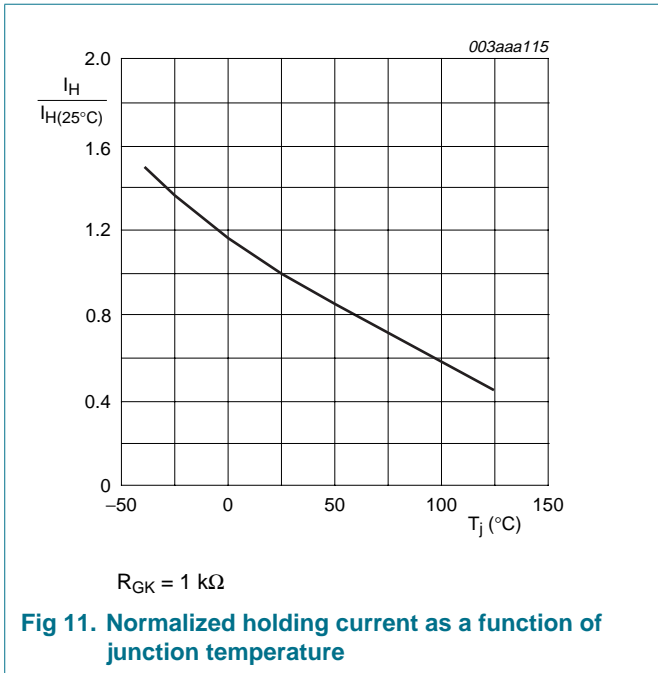
$V_o = 0.895 \text{ V}$   
 $R_s = 0.195 \text{ } \Omega$   
 (1)  $T_j = 125 \text{ } ^\circ\text{C}$ ; typical values  
 (2)  $T_j = 125 \text{ } ^\circ\text{C}$ ; maximum values  
 (3)  $T_j = 25 \text{ } ^\circ\text{C}$ ; typical values

Fig 9. On-state current as a function of on-state voltage



$R_{GK} = 1 \text{ k}\Omega$

Fig 10. Normalized latching current as a function of junction temperature



## 7. Package information

Epoxy meets requirements of UL 94 V-0 at 3.175 mm



## 8. Package outline

Plastic single-ended leaded (through hole) package; 3 leads

SOT54

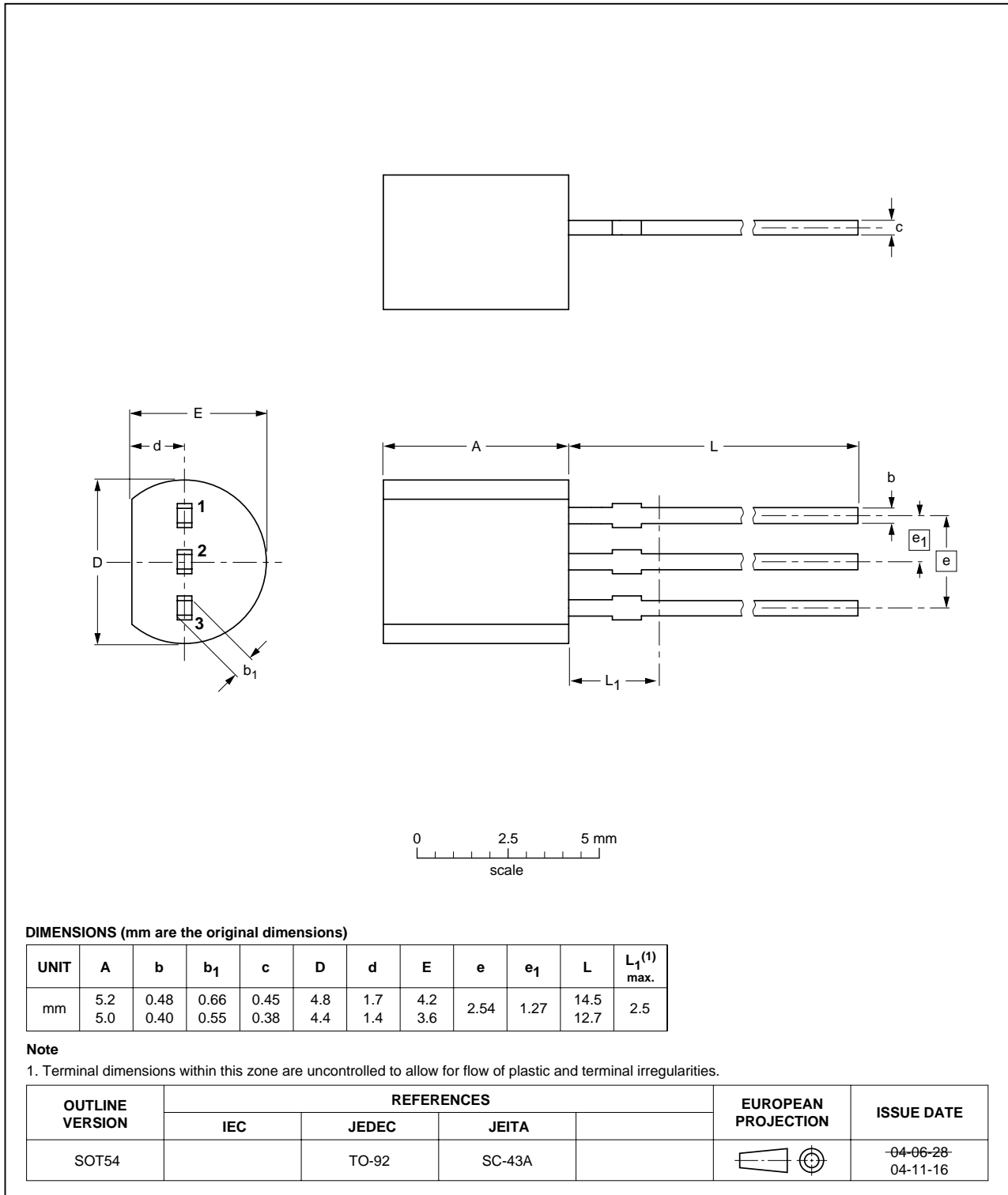


Fig 13. Package outline SOT54 (TO-92)

## 9. Revision history

**Table 6. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
EC103D1_2	20080731	Product data sheet	-	EC103D1-01
Modifications:		<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• <a href="#">Table 3 “Limiting values” on page 2</a>; <math>V_{DSM}</math> and <math>V_{RSM}</math> added.</li><li>• <a href="#">Table 5 “Characteristics” on page 6</a>; <math>dV_D/dt</math> updated.</li><li>• <a href="#">Figure 4 on page 4</a>; graph redrawn.</li><li>• <a href="#">Figure 6 on page 5</a>; graph redrawn.</li><li>• <a href="#">Figure 11</a>; graph added.</li><li>• <a href="#">Figure 12</a>; graph added.</li></ul>		
EC103D1-01 (9397 750 08574)	20011101	Product data	-	-

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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**12. Contents**

**1 Product profile . . . . . 1**

1.1 General description . . . . . 1

1.2 Features . . . . . 1

1.3 Applications . . . . . 1

1.4 Quick reference data . . . . . 1

**2 Pinning information . . . . . 1**

**3 Ordering information . . . . . 2**

**4 Limiting values . . . . . 2**

**5 Thermal characteristics . . . . . 5**

**6 Characteristics . . . . . 6**

**7 Package information . . . . . 8**

**8 Package outline . . . . . 9**

**9 Revision history . . . . . 10**

**10 Legal information . . . . . 11**

10.1 Data sheet status . . . . . 11

10.2 Definitions . . . . . 11

10.3 Disclaimers . . . . . 11

10.4 Trademarks . . . . . 11

**11 Contact information . . . . . 11**

**12 Contents . . . . . 12**

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