

HEF4069UB-Q100

Hex inverter

Rev. 1 — 28 February 2013

Product data sheet

1. General description

The HEF4069UB-Q100 is a general-purpose hex inverter. Each inverter has a single stage.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- ESD protection:
 - ◆ MIL-STD-883C, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V ($C = 200\text{ pF}$, $R = 0\text{ }\Omega$)
- Complies with JEDEC standard JESD 13-B

3. Applications

- Oscillator

4. Ordering information

Table 1. Ordering information

All types operate from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$.

Type number	Package		Version
	Name	Description	
HEF4069UBT-Q100	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
HEF4069UBTT-Q100	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1



5. Functional diagram

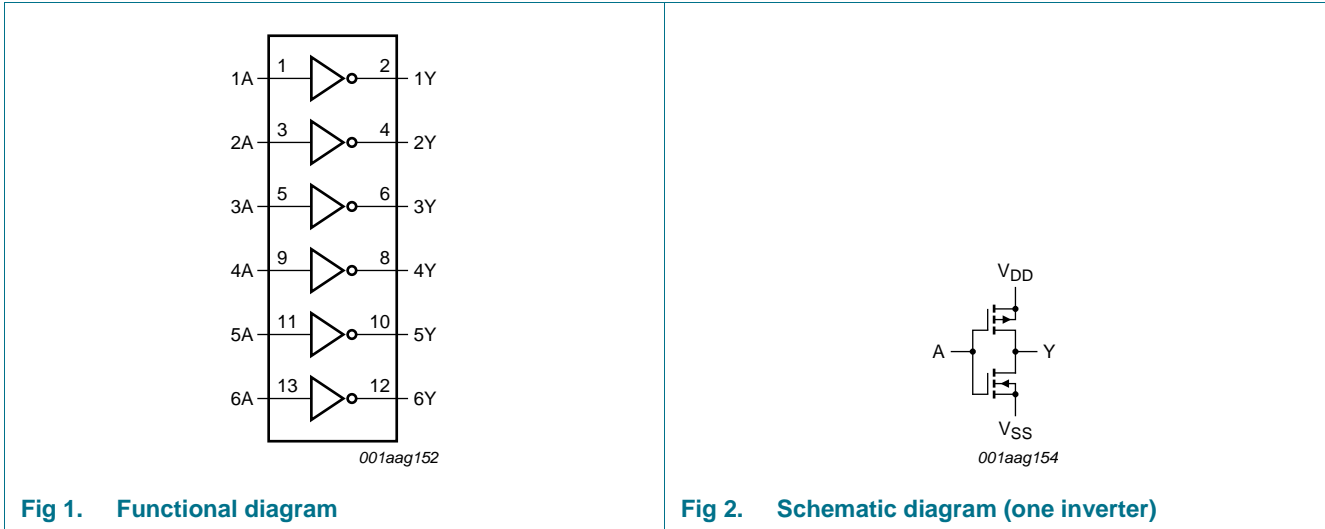


Fig 1. Functional diagram

Fig 2. Schematic diagram (one inverter)

6. Pinning information

6.1 Pinning

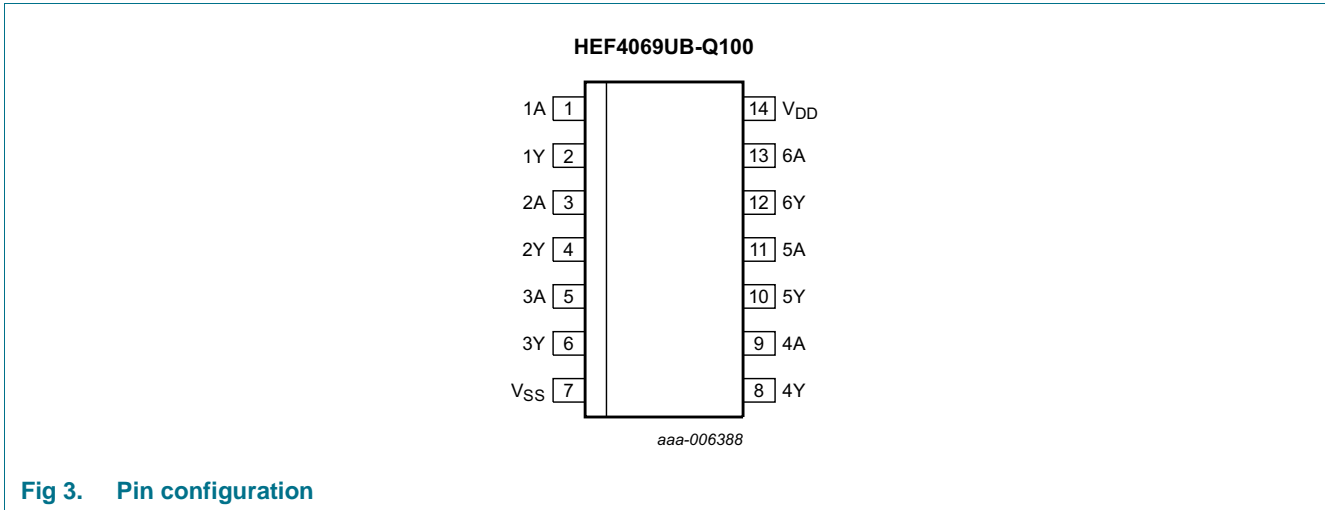


Fig 3. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 6A	1, 3, 5, 9, 11, 13	input
1Y to 6Y	2, 4, 6, 8, 10, 12	output
V _{SS}	7	ground (0 V)
V _{DD}	14	supply voltage

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V_{DD}	supply voltage		-0.5	+18	V	
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$	-	± 10	mA	
V_I	input voltage		-0.5	$V_{DD} + 0.5$	V	
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$	-	± 10	mA	
$I_{I/O}$	input/output current		-	± 10	mA	
I_{DD}	supply current		-	50	mA	
T_{stg}	storage temperature		-65	+150	°C	
T_{amb}	ambient temperature		-40	+125	°C	
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$				
		SO14	[1]	-	500	mW
		TSSOP14	[2]	-	500	mW
P	power dissipation	per output	-	100	mW	

[1] For SO14 packages: above $T_{amb} = 70\text{ °C}$, P_{tot} derates linearly with 8 mW/K.

[2] For TSSOP14 packages: above $T_{amb} = 60\text{ °C}$, P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	-	+125	°C

9. Static characteristics

Table 5. Static characteristics
 $V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} ; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	$T_{amb} = -40\text{ °C}$		$T_{amb} = +25\text{ °C}$		$T_{amb} = +85\text{ °C}$		$T_{amb} = +125\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	4	-	4	-	4	-	4	-	V
			10 V	8	-	8	-	8	-	8	-	V
			15 V	12.5	-	12.5	-	12.5	-	12.5	-	V
V_{IL}	LOW-level input voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	-	1	-	1	-	1	-	1	V
			10 V	-	2	-	2	-	2	-	2	V
			15 V	-	2.5	-	2.5	-	2.5	-	2.5	V
V_{OH}	HIGH-level output voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$ I_O < 1\text{ }\mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
		$V_O = 4.6\text{ V}$	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
		$V_O = 9.5\text{ V}$	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
		$V_O = 13.5\text{ V}$	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
I_{OL}	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
I_I	input leakage current		15 V	-	± 0.1	-	± 0.1	-	± 1.0	-	± 1.0	μA
I_{DD}	supply current	all valid input combinations; $I_O = 0\text{ A}$	5 V	-	0.25	-	0.25	-	7.5	-	7.5	μA
			10 V	-	0.5	-	0.5	-	15.0	-	15.0	μA
			15 V	-	1.0	-	1.0	-	30.0	-	30.0	μA
C_I	input capacitance	digital inputs		-	-	-	7.5	-	-	-	pF	

10. Dynamic characteristics

Table 6. Dynamic characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$; for waveforms see [Figure 4](#); for test circuit see [Figure 5](#).

Symbol	Parameter	Conditions	V _{DD}	Extrapolation formula ^[1]	Min	Typ	Max	Unit
t _{PHL}	HIGH to LOW propagation delay	nA to nY;	5 V	$18\text{ ns} + (0.55\text{ ns/pF})C_L$	-	45	90	ns
			10 V	$9\text{ ns} + (0.23\text{ ns/pF})C_L$	-	20	40	ns
			15 V	$7\text{ ns} + (0.16\text{ ns/pF})C_L$	-	15	25	ns
t _{PLH}	LOW to HIGH propagation delay	nA to nY	5 V	$13\text{ ns} + (0.55\text{ ns/pF})C_L$	-	40	80	ns
			10 V	$9\text{ ns} + (0.23\text{ ns/pF})C_L$	-	20	40	ns
			15 V	$7\text{ ns} + (0.16\text{ ns/pF})C_L$	-	15	30	ns
t _{THL}	HIGH to LOW output transition time	output nY	5 V	$10\text{ ns} + (1.00\text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns
t _{TLH}	LOW to HIGH output transition time	output nY	5 V	$10\text{ ns} + (1.00\text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns

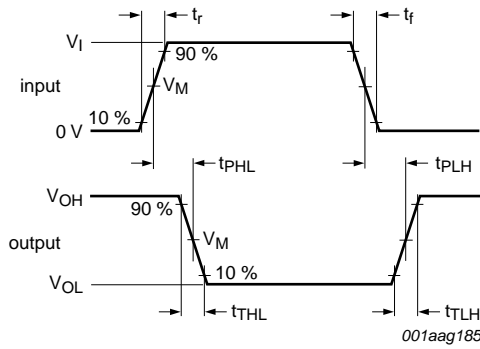
[1] The typical value of the propagation delay and output transition time can be calculated with the extrapolation formula (C_L in pF).

Table 7. Dynamic power dissipation

$V_{SS} = 0\text{ V}$; $t_r = t_f \leq 20\text{ ns}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

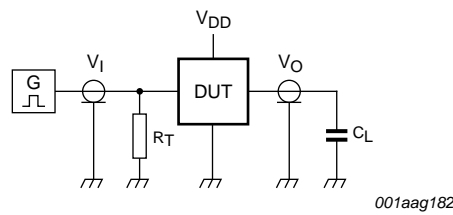
Symbol	Parameter	V _{DD}	Typical formula	Where
P _D	dynamic power dissipation	5 V	$P_D = 600 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2\ (\mu\text{W})$	f_i = input frequency in MHz;
		10 V	$P_D = 4000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2\ (\mu\text{W})$	f_o = output frequency in MHz;
		15 V	$P_D = 22000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2\ (\mu\text{W})$	C_L = output load capacitance in pF; $\Sigma(f_o \times C_L)$ = sum of the outputs; V_{DD} = supply voltage in V.

11. Waveforms



Measurement points: $V_M = 0.5V_{DD}$.
 Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 4. Propagation delay and transition times



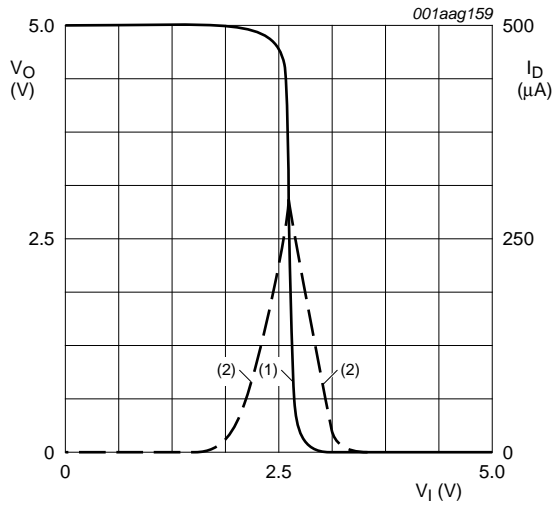
Definitions for test circuit:
 C_L = load capacitance including jig and probe capacitance;
 R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator;
 For test data, refer to [Table 8](#).

Fig 5. Test circuit for measuring switching times

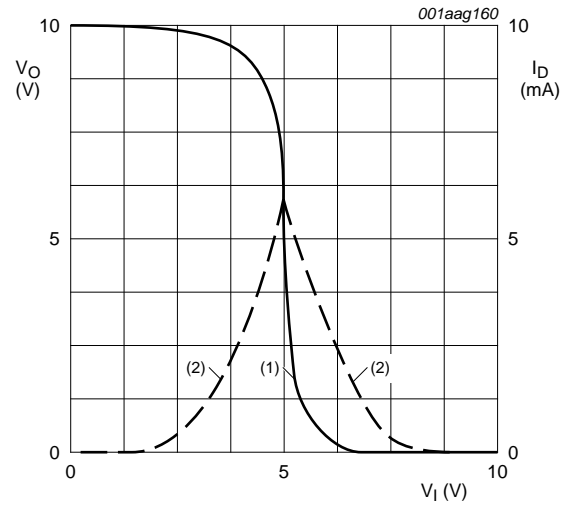
Table 8. Test data

Supply voltage	Input	Load
V_{DD}	V_I	C_L
5 V to 15 V	V_{SS} or V_{DD}	50 pF

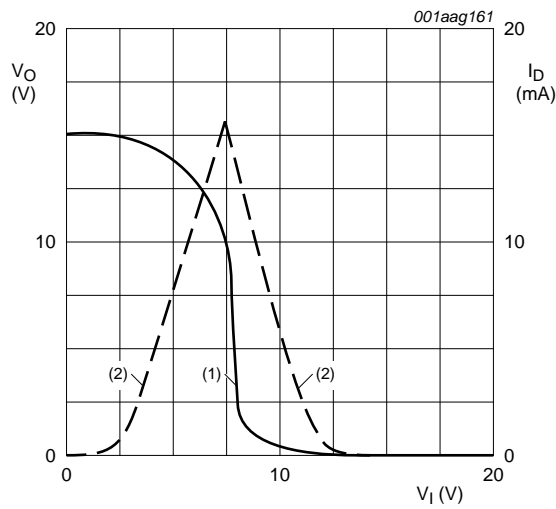
11.1 Transfer characteristics



a. $V_{DD} = 5\text{ V}; I_O = 0\text{ A}$



b. $V_{DD} = 10\text{ V}; I_O = 0\text{ A}$



c. $V_{DD} = 15\text{ V}; I_O = 0\text{ A}$

- (1) V_O = output voltage.
- (2) I_D = drain current.

Fig 6. Typical transfer characteristics

12. Application information

Some examples of applications for the HEF4069UB-Q100.

[Figure 7](#) shows an astable relaxation oscillator using two HEF4069UB-Q100 inverters and 2 BAW62 diodes. The oscillation frequency is mainly determined by $R1 \times C1$, provided $R1 \ll R2$ and $R2 \times C2 \ll R1 \times C1$.

The function of R2 is to minimize the influence of the forward voltage across the protection diodes on the frequency; C2 is a stray (parasitic) capacitance.

The period T_p is given by $T_p = T_1 + T_2$,

where:

$$T_1 = R1C1 \ln \frac{V_{DD} + V_{ST}}{V_{ST}}$$

$$T_2 = R1C1 \ln \frac{2V_{DD} - V_{ST}}{V_{DD} - V_{ST}}$$

V_{ST} = the signal threshold level of the inverter.

The period is fairly independent of V_{DD} , V_{ST} and temperature. The duty factor, however, is influenced by V_{ST} .

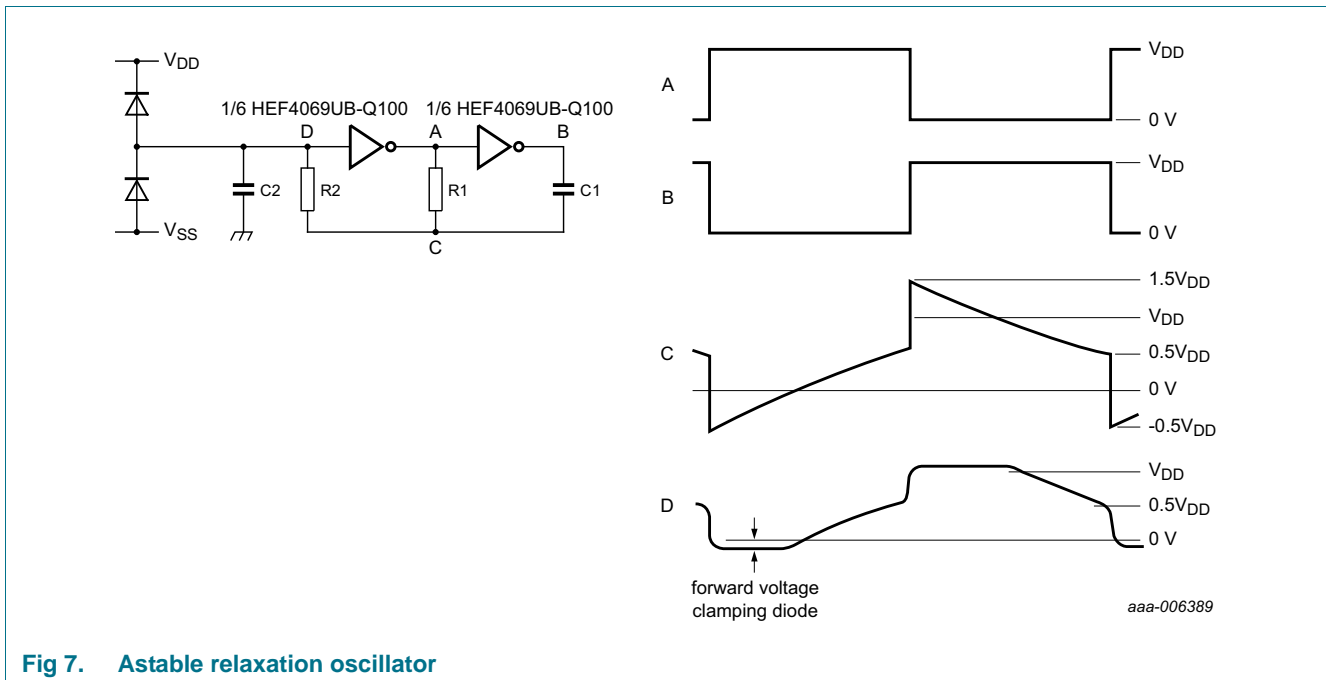
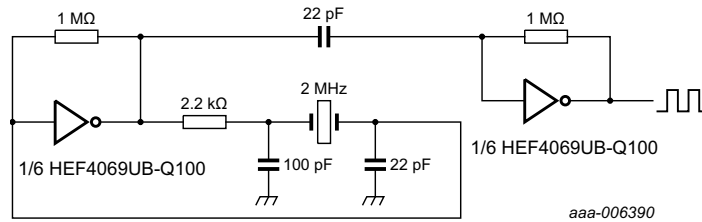


Fig 7. Astable relaxation oscillator

Figure 8 shows a crystal oscillator for frequencies up to 10 MHz using two HEF4069UB-Q100 inverters. The second inverter amplifies the oscillator output voltage to a level sufficient to drive other Local Oxidation CMOS (LOCMOS) circuits.



The output inverter is used to amplify the oscillator output voltage to a level sufficient to drive other LOCMOS circuits.

Fig 8. Crystal oscillator

Figure 9 and Figure 10 show voltage gain and supply current. Figure 11 shows the test set-up and an example of an analog amplifier using one HEF4069UB-Q100.

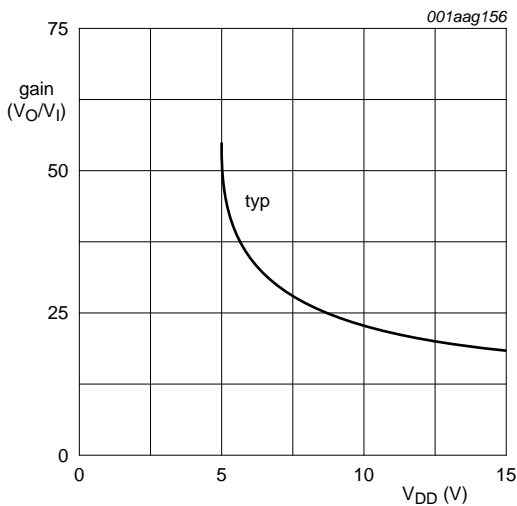


Fig 9. Typical voltage gain as a function of supply voltage

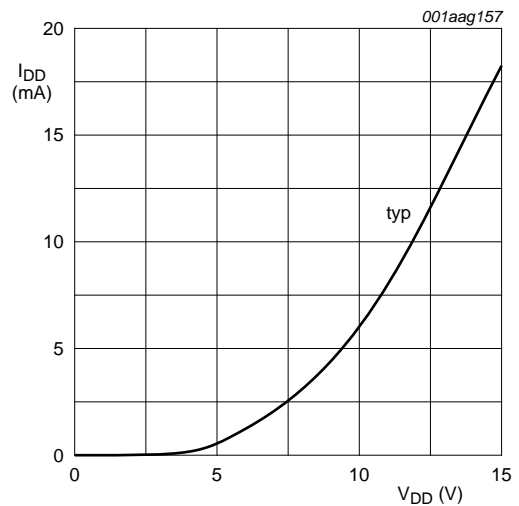


Fig 10. Typical supply current as a function of supply voltage

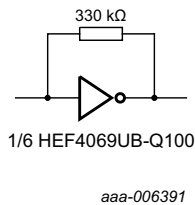
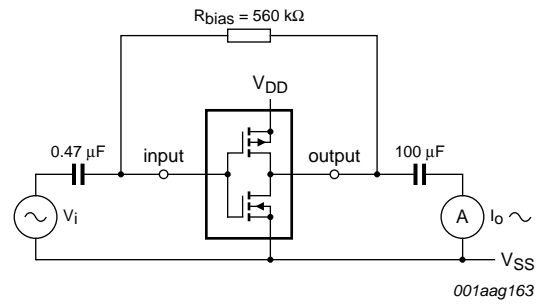
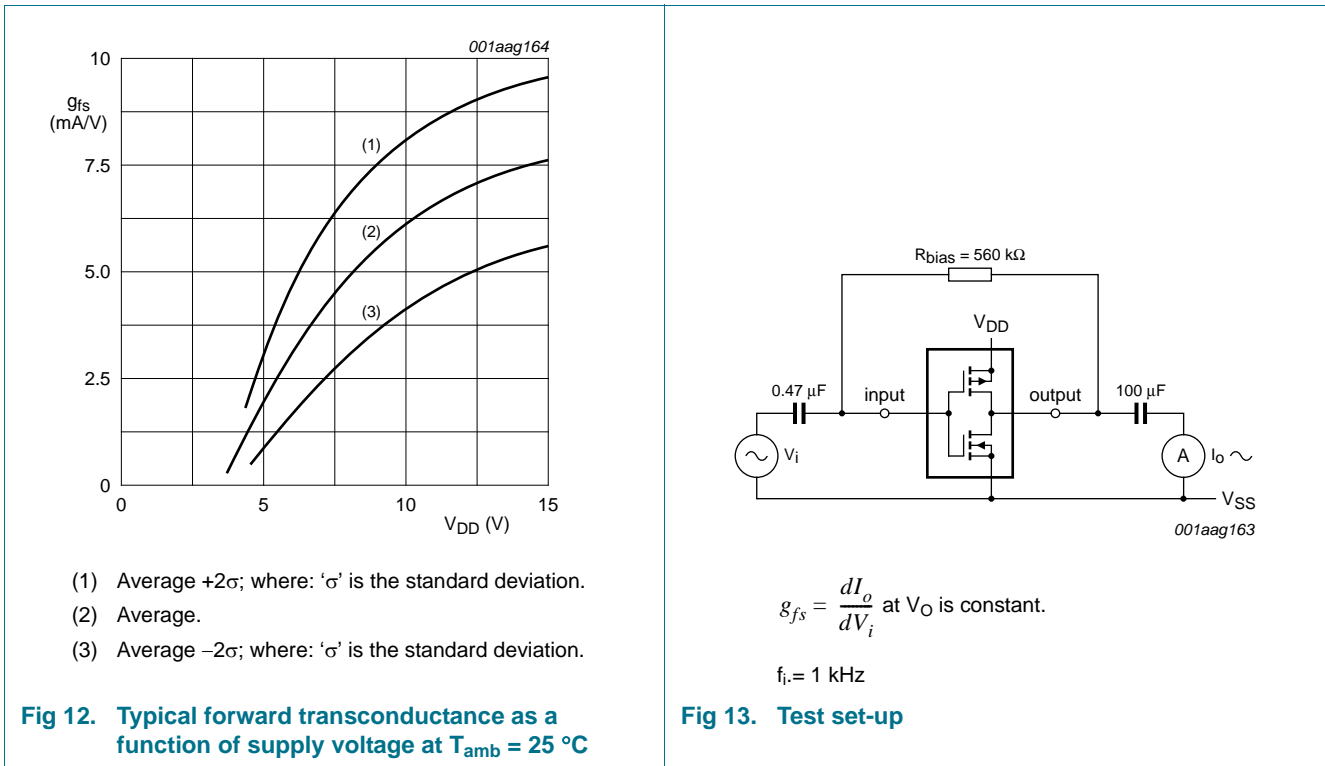


Fig 11. Test set-up

Figure 12 shows typical forward transconductance and Figure 13 shows the test set-up.



$$g_{fs} = \frac{dI_o}{dV_i} \text{ at } V_O \text{ is constant.}$$

f_i = 1 kHz

Fig 13. Test set-up

13. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

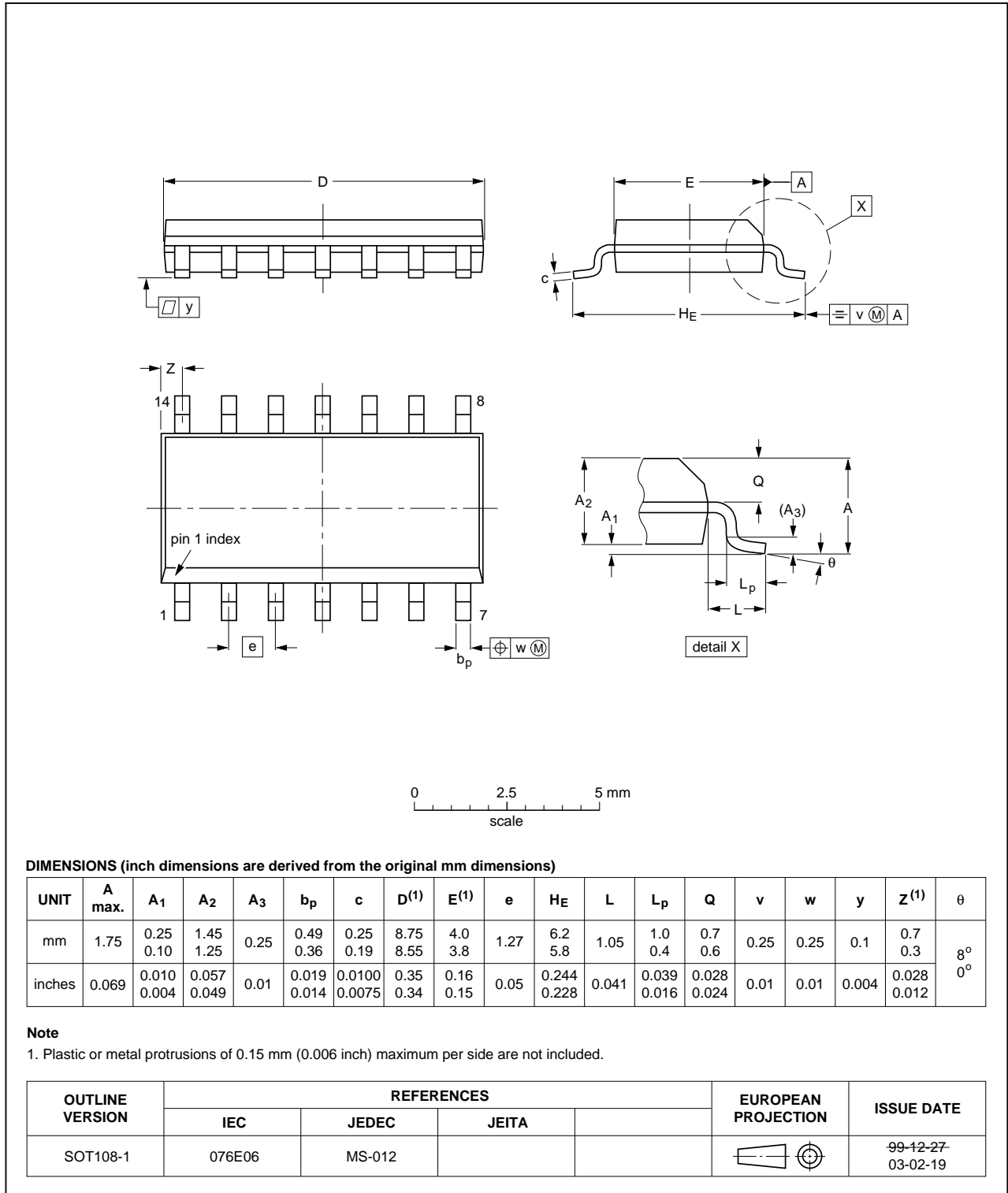


Fig 14. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

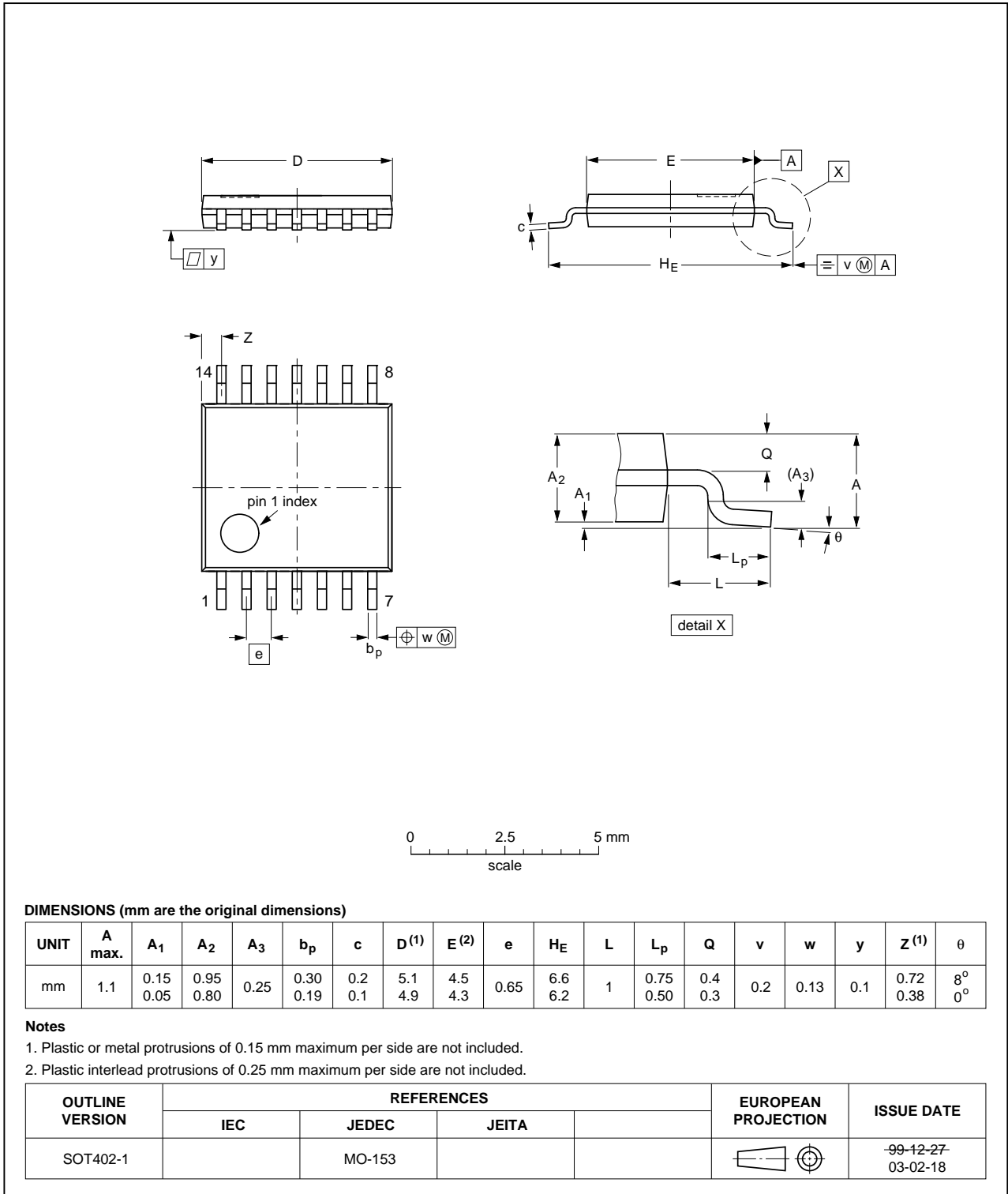


Fig 15. Package outline SOT402-1 (TSSOP14)

14. Abbreviations

Table 9. Abbreviations

Acronym	Description
HBM	Human Body Model
ESD	ElectroStatic Discharge
MM	Machine Model
MIL	Military

15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4069UB_Q100 v.1	20130228	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
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Date of release: 28 February 2013

Document identifier: HEF4069UB_Q100