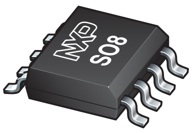


PHP225

Dual P-channel intermediate level FET

Rev. 04 — 17 March 2011 | Product data sheet

1. Product profile

1.1 General description

Dual intermediate level P-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using vertical D-MOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for high frequency applications due to fast switching characteristics

1.3 Applications

- Motor and actuator drivers
- Power management
- Synchronized rectification

1.4 Quick reference data

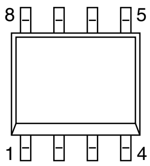
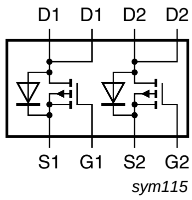
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C		-	-	-30	V
I_D	drain current	$T_{sp} \leq 80$ °C		-	-	-2.3	A
P_{tot}	total power dissipation	$T_{sp} = 80$ °C	[1]	-	-	2	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = -10$ V; $I_D = -1$ A; $T_j = 25$ °C		-	0.22	0.25	Ω
Dynamic characteristics							
Q_{GD}	gate-drain charge	$V_{GS} = -10$ V; $I_D = -2.3$ A; $V_{DS} = -15$ V; $T_j = 25$ °C		-	3	-	nC

[1] Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 2 W at the same time.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 SOT96-1 (SO8)	
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PHP225	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C		-	-30	V
V_{GS}	gate-source voltage			-	-	V
V_{GSO}	gate-source voltage	open drain		-20	20	V
I_D	drain current	$T_{sp} \leq 80$ °C		-	-2.3	A
I_{DM}	peak drain current	$T_{sp} = 25$ °C; pulsed	[1]	-	-10	A
P_{tot}	total power dissipation	$T_{amb} = 25$ °C	[2]	-	1	W
		$T_{sp} = 80$ °C	[3]	-	2	W
		$T_{amb} = 25$ °C	[4]	-	1.3	W
			[5]	-	2	W
T_{stg}	storage temperature			-65	150	°C
T_j	junction temperature			-	150	°C
Source-drain diode						
I_S	source current	$T_{sp} \leq 80$ °C		-	-1.25	A
I_{SM}	peak source current	$T_{sp} = 25$ °C; pulsed	[1]	-	-5	A

[1] Pulse width and duty cycle limited by maximum junction temperature.

[2] Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with a thermal resistance from ambient to tie-point of 90 K/W.

[3] Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 2 W at the same time.

[4] Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with a thermal resistance from ambient to tie-point of 90 K/W.

[5] Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with a thermal resistance from ambient to tie-point of 27.5 K/W.

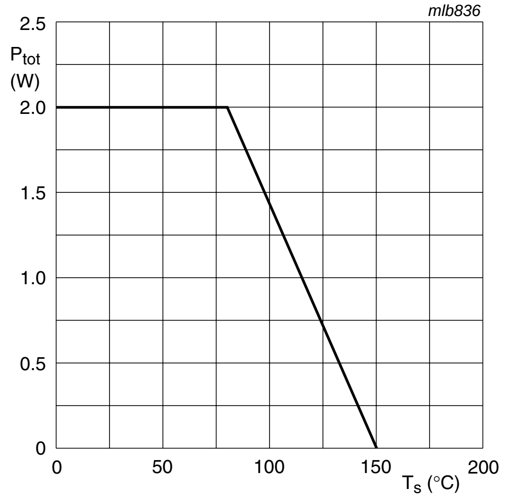
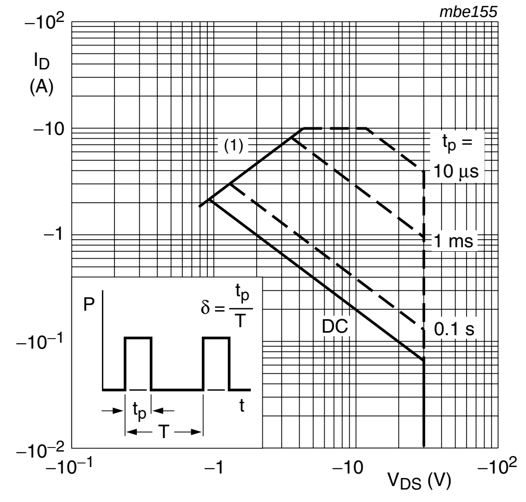


Fig 1. Power derating curve



δ = 0.01

T_s = 80 °C.

(1) R_{DSon} limitation.

Fig 2. SOAR; P-channel

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see Figure 3	-	-	35	K/W

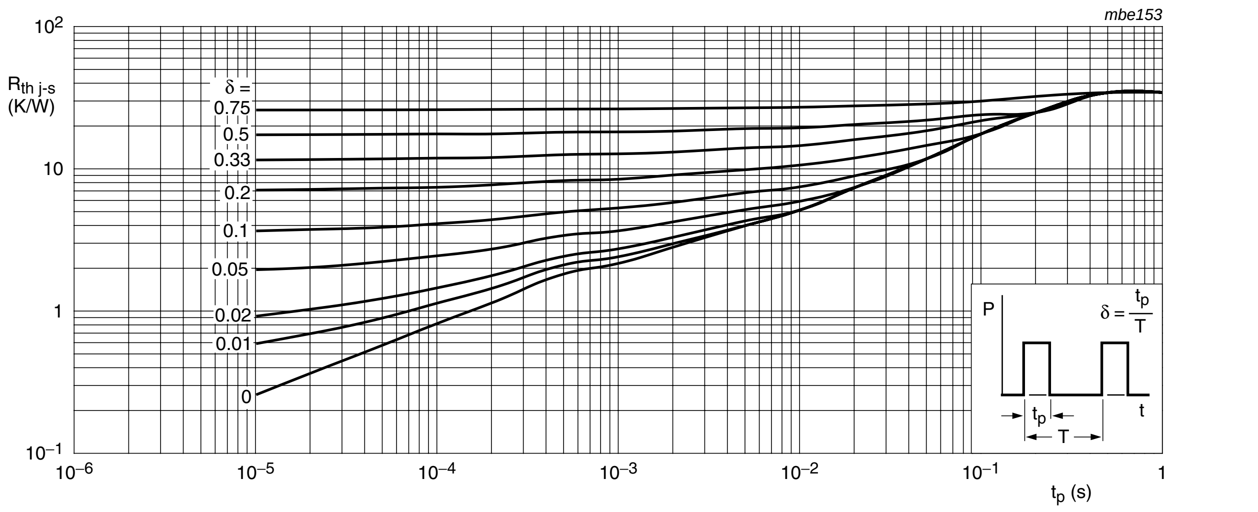
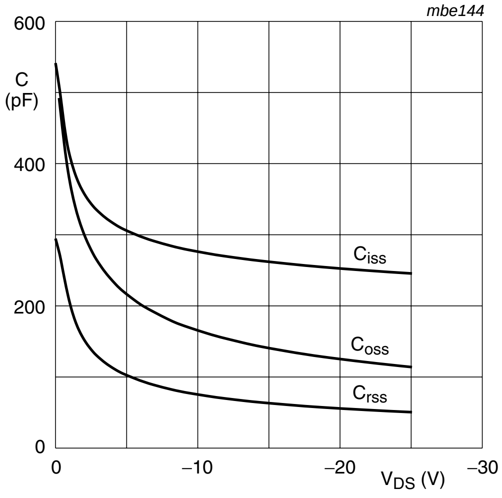


Fig 3. Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

6. Characteristics

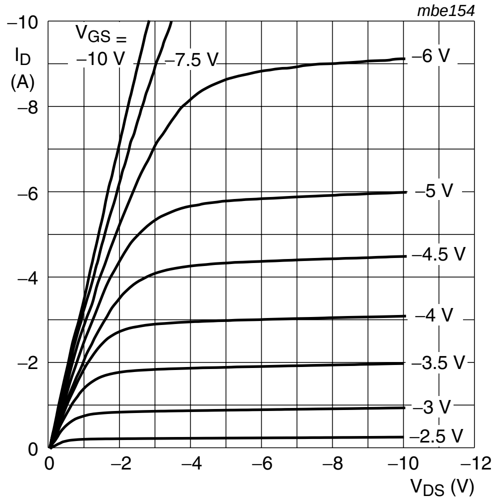
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = -10 µA; V_{GS} = 0 V; T_j = 25 °C	-30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = -1 mA; V_{DS} = V_{GS}; T_j = 25 °C	-1	-	-2.8	V
I_{DSS}	drain leakage current	V_{DS} = -24 V; V_{GS} = 0 V; T_j = 25 °C	-	-	-100	nA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = -10 V; I_D = -1 A; T_j = 25 °C	-	0.22	0.25	Ω
		V_{GS} = -4.5 V; I_D = -0.5 A; T_j = 25 °C	-	0.33	0.4	Ω
I_{DSon}	on-state drain current	V_{DS} = -1 V; V_{GS} = -10 V	-2.3	-	-	A
		V_{DS} = -5 V; V_{GS} = -4.5 V	-1	-	-	A
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = -2.3 A; V_{DS} = -15 V; V_{GS} = -10 V; T_j = 25 °C	-	10	25	nC
Q_{GS}	gate-source charge		-	1	-	nC
Q_{GD}	gate-drain charge		-	3	-	nC
C_{iss}	input capacitance	V_{DS} = -20 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C	-	250	-	pF
C_{oss}	output capacitance		-	140	-	pF
C_{rss}	reverse transfer capacitance		-	50	-	pF
g_{fs}	transfer conductance	V_{DS} = -20 V; I_D = -1 A; T_j = 25 °C	1	2	-	S
t_{off}	turn-off time	V_{DS} = -20 V; V_{GS} = -10 V; $R_{G(ext)}$ = 4.7 Ω; R_L = 20 Ω; T_j = 25 °C; I_D = -1 A	-	50	140	ns
t_{on}	turn-on time		-	20	80	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = -1.25 A; V_{GS} = 0 V; T_j = 25 °C	-	-	-1.6	V
t_{rr}	reverse recovery time	I_S = -1.25 A; dI_S/dt = 100 A/µs; V_{GS} = 0 V; V_{DS} = 25 V; T_j = 25 °C	-	150	200	ns



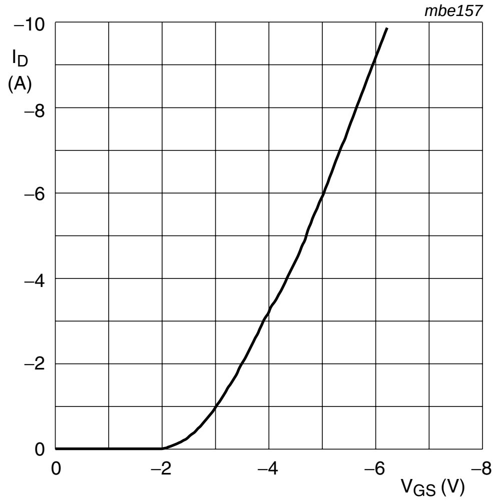
$T_j = 25°C; V_{GS} = 0V$

Fig 4. Capacitance as a function of drain-source voltage; P-channel; typical values



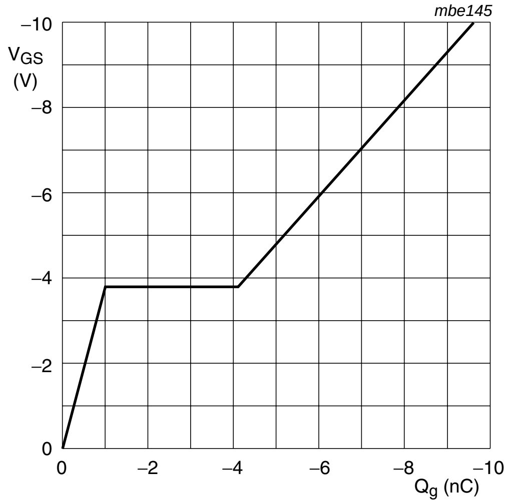
$T_j = 25°C$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; P-channel; typical values



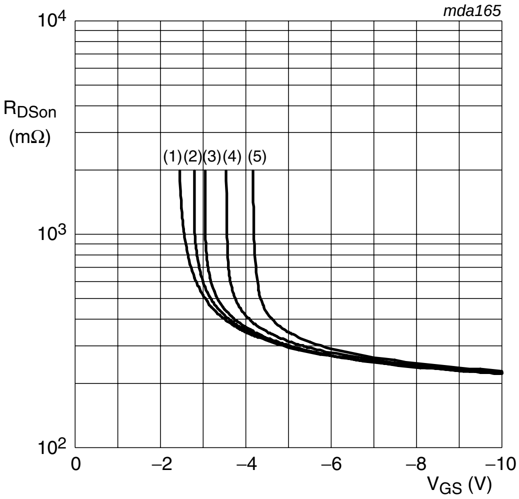
$T_j = 25°C; V_{DS} = -10V$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; P-channel; typical values



$I_D = -2.3A; V_{DS} = -15V$

Fig 7. Gate-source voltage as a function of gate charge; P-channel; typical values



$-V_{DS} \geq -I_D \times R_{DSon}$; T_j = 25 °C.

(1) I_D = -0.1 A.

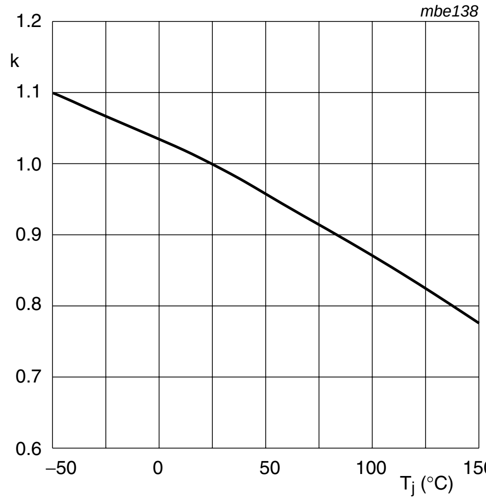
(2) I_D = -0.5 A.

(3) I_D = -1 A.

(4) I_D = -2.3 A.

(5) I_D= -4.5 A.

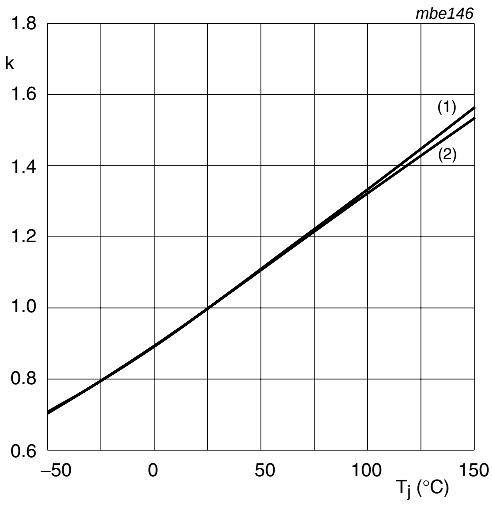
Fig 8. Drain-source on-state resistance as a function of drain current; typical values



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at I_D = 1 mA; $V_{DS} = V_{GS} = V_{GSth}$.

Fig 9. Temperature coefficient of gate-source threshold voltage



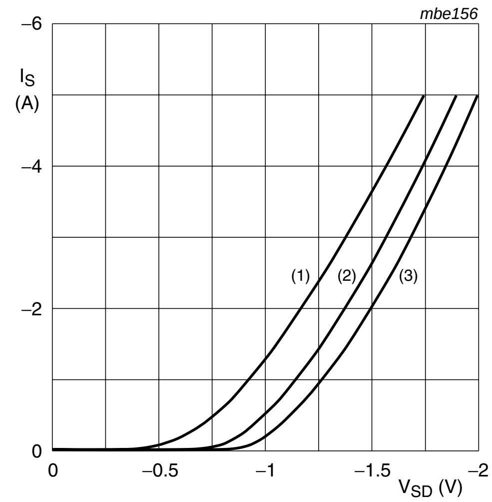
$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25°C}$$

Typical R_{DSon} at:

(1) I_D = -1 A; V_{GS} = -10 V.

(2) I_D = -0.5 A; V_{GS} = -4.5 V.

Fig 10. Temperature coefficient of drain-source on-state resistance; P-channel

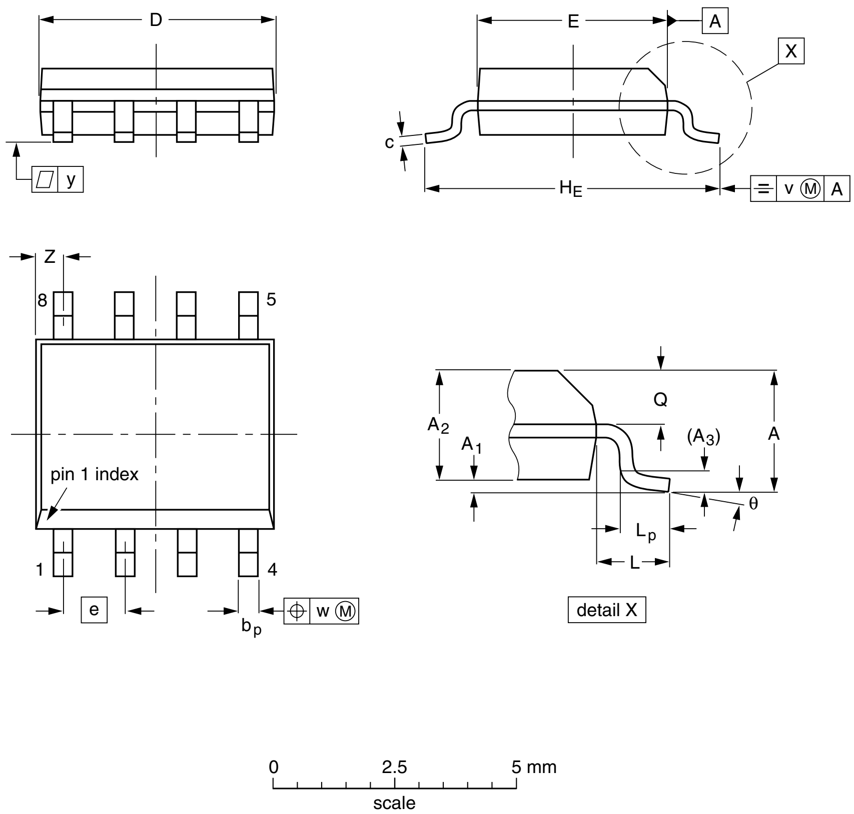


$$V_{GD} = 0V (1) T_j = 150°C (2) T_j = 25°C (3) T_j = -55°C$$

Fig 11. Source current as a function of source-drain voltage

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 12. Package outline SOT96-1 (SO8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHP225 v.4	20110317	Product data sheet	-	PHP225 v.3
Modifications:	• Various changes to content.			
PHP225 v.3	20110104	Product data sheet	-	PHP225 v.2

9. Legal information

9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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11. Contents

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