SI4410DY

N-channel TrenchMOS logic level FET

Rev. 03 — 4 December 2009

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for high frequency applications due to fast switching characteristics

1.3 Applications

- DC motor control
- DC-to-DC convertors
- Lithium-ion battery applications
- Notebook computers
- Portable equipment

1.4 Quick reference data

Table 1. Quick reference

		6 IIII		_		
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DS}	drain-source voltage	$T_j \ge 25 \text{ °C}; T_j \le 150 \text{ °C}$	-	-	30	V
I _D	drain current	T _{amb} = 25 °C; pulsed; see <u>Figure 1</u> and <u>3</u>	-	-	10	Α
P _{tot}	total power dissipation	T _{amb} = 25 °C; pulsed; see <u>Figure 2</u>	-	-	2.5	W
Dynamic	characteristics					
Q _{GD} gate-drain charge		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A};$ $V_{DS} = 15 \text{ V}; T_j = 25 \text{ °C};$ see Figure 12	-	7	-	nC
Static ch	aracteristics					
R _{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 5 \text{ A};$ $T_j = 25 \text{ °C};$ see <u>Figure 10</u> and <u>11</u>	-	15	20	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A};$ $T_j = 25 \text{ °C};$ see Figure 10 and 11	-	11	13.5	mΩ



N-channel TrenchMOS logic level FET

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		_
2	S	source	8 7 7 7 75	D
3	S	source		G (FX)
4	G	gate		
5	D	drain	1	mbb076 S
6	D	drain	SOT96-1 (SO8)	
7	D	drain		
8	D	drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
SI4410DY	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Limiting values

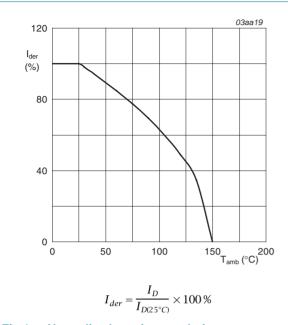
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 150 °C	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I _D	drain current	T _{amb} = 70 °C; pulsed; see <u>Figure 1</u>	-	8	Α
		T _{amb} = 25 °C; pulsed; see <u>Figure 1</u> and <u>3</u>	-	10	Α
I_{DM}	peak drain current	$t_p \le 10 \ \mu s; T_{amb} = 25 \ ^{\circ}C; pulsed;$ see Figure 3	-	50	Α
P _{tot}	total power dissipation	T _{amb} = 70 °C; pulsed; see <u>Figure 2</u>	-	1.6	W
		T _{amb} = 25 °C; pulsed; see <u>Figure 2</u>	-	2.5	W
T _{stg}	storage temperature		-55	150	°C
Tj	junction temperature		-55	150	°C
Source-dr	ain diode				
Is	source current	T _{amb} = 25 °C; pulsed	-	2.3	Α

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N-channel TrenchMOS logic level FET



Normalized continuous drain current as a function of ambient temperature

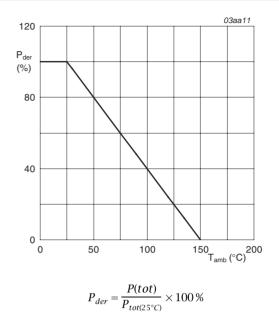
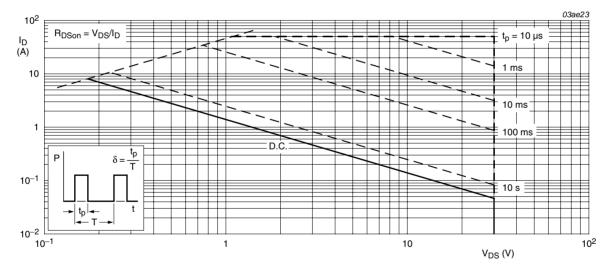


Fig 2. Normalized total power dissipation as a function of ambient temperature



 $T_{amb} = 25$ °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

3 of 12

N-channel TrenchMOS logic level FET

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	-	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint; tp ≤ 10 s; see <u>Figure 4</u>	-	-	50	K/W

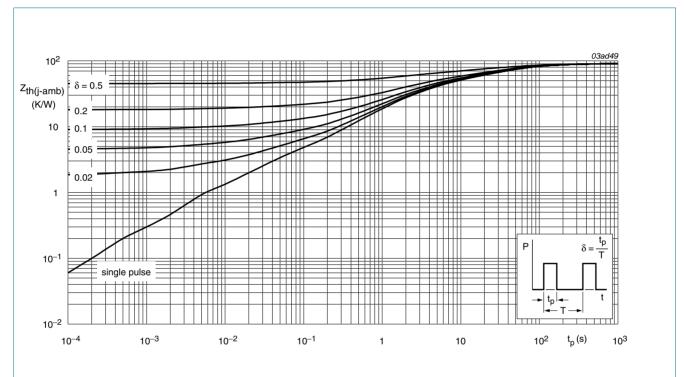


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

N-channel TrenchMOS logic level FET

6. Characteristics

Table 6. Characteristics

Table 0.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	aracteristics					
$V_{GS(th)}$	gate-source threshold voltage	I_D = 250 μ A; V_{DS} = V_{GS} ; T_j = 25 °C; see <u>Figure 9</u>	1	-	-	V
I _{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	1	μΑ
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 55 \text{ °C}$	-	-	25	μΑ
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nΑ
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nΑ
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see <u>Figure 10</u> and <u>11</u>	-	15	20	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see Figure 10 and 11	-	11	13.5	mΩ
I _{DSon}	on-state drain-source current	$V_{DS} \ge 5 \text{ V}; V_{GS} = 10 \text{ V}$	20	-	-	Α
Dynamic	characteristics					
Q _{G(tot)}	total gate charge	$I_D = 10 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 5 \text{ V};$ $T_j = 25 ^{\circ}\text{C}; \text{ see } \frac{\text{Figure } 12}{\text{ Composition}}$	-	21.5	34	nC
		$I_D = 10 \text{ A}$; $V_{DS} = 15 \text{ V}$; $V_{GS} = 10 \text{ V}$;	-	40	60	nC
Q_{GS}	gate-source charge	T _j = 25 °C; see <u>Figure 12</u>	-	8	-	nC
Q_{GD}	gate-drain charge		-	7	-	nC
t _{d(on)}	turn-on delay time	$V_{DS} = 25 \text{ V}; R_L = 25 \Omega; V_{GS} = 10 \text{ V};$	-	13.5	30	ns
t _r	rise time	$R_{G(ext)} = 6 \Omega$; $T_j = 25 °C$	-	9	20	ns
t _{d(off)}	turn-off delay time		-	70	100	ns
t _f	fall time		-	30	80	ns
g _{fs}	transfer conductance	$V_{DS} = 15 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ °C};$ see <u>Figure 13</u>	-	34	-	S
Source-d	rain diode					
V_{SD}	source-drain voltage	$I_S = 2.3 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ °C}$; see <u>Figure 14</u>	-	0.7	1.1	V
t _{rr}	reverse recovery time	$I_S = 2.3 \text{ A}$; $dI_S/dt = -100 \text{ A/}\mu\text{s}$; $V_{GS} = 0 \text{ V}$; $V_{DS} = 25 \text{ V}$; $T_i = 25 \text{ °C}$	-	50	80	ns

N-channel TrenchMOS logic level FET

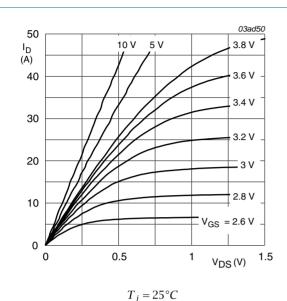


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

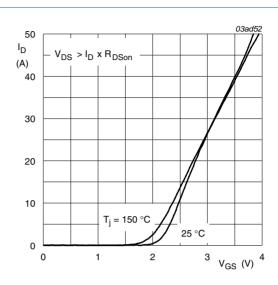


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

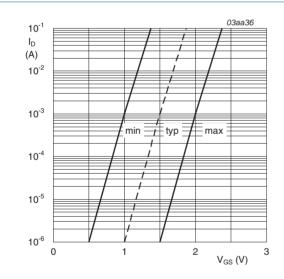
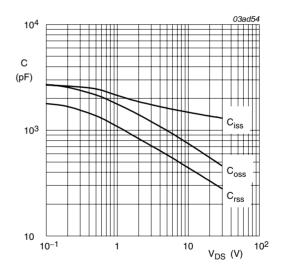


Fig 7. Sub-threshold drain current as a function of gate-source voltage

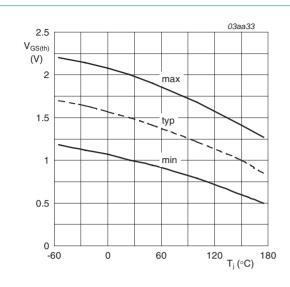
 $T_i = 25 \, {}^{\circ}C; V_{DS} = 5 \, V$



 $V_{GS} = 0V; f = 1MHz$

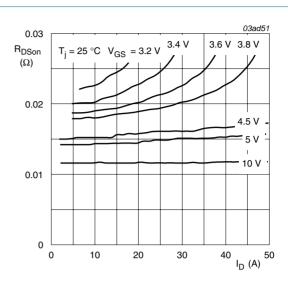
Fig 8. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

N-channel TrenchMOS logic level FET



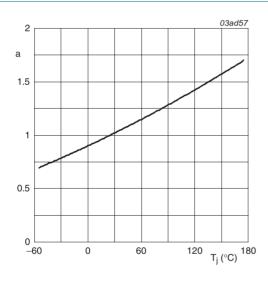
$$I_D = 1 \, mA; V_{DS} = V_{GS}$$

Fig 9. Gate-source threshold voltage as a function of junction temperature



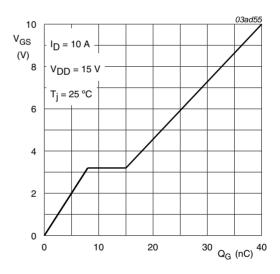
 $T_j = 25^{\circ}C$

Fig 10. Drain-source on-state resistance as a function of drain current; typical values



 $a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$

Fig 11. Normalized drain-source on-state resistance factor as a function of junction temperature



$$I_D = 10A; V_{DD} = 15V$$

Fig 12. Gate-source voltage as a function of gate charge; typical values

N-channel TrenchMOS logic level FET

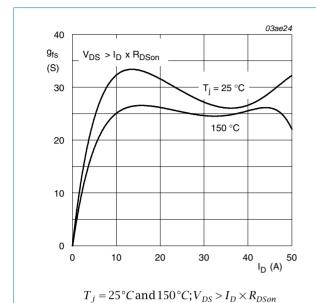


Fig 13. Forward transconductance as a function of drain current; typical values

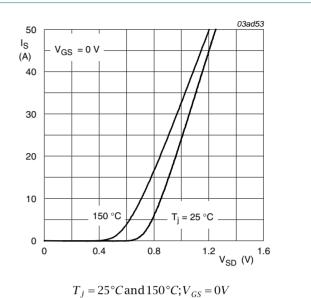
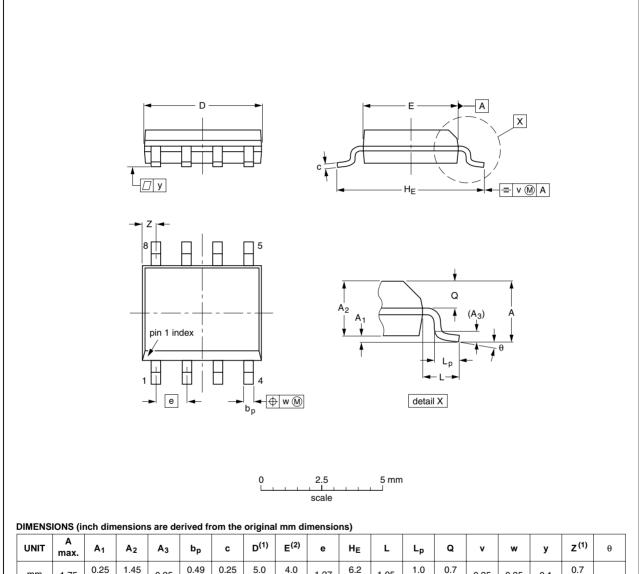


Fig 14. Source current as a function of source-drain voltage; typical values

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Q	v	w	у	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016		0.01	0.01	0.004	0.028 0.012	0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
- 2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT96-1	076E03	MS-012			99-12-27 03-02-18

Fig 15. Package outline SOT96-1 (SO8)

N-channel TrenchMOS logic level FET

10 of 12

8. Revision history

Table 7. Revision history

	-									
Document ID	Release date	Data sheet status	Change notice	Supersedes						
SI4410DY_3	20091204	Product data sheet	-	SI4410DY-02						
Modifications:	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. 									
 Legal texts have been adapted to the new company name where appropriate. 										
SI4410DY-02	20010705	Product specification	-	SI4410DY-01						
SI4410DY-01	20010220	Product specification	-	-						

N-channel TrenchMOS logic level FET

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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SI4410DY_3

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N-channel TrenchMOS logic level FET

11. Contents

1	Product profile	.1
1.1	General description	. 1
1.2	Features and benefits	. 1
1.3	Applications	. 1
1.4	Quick reference data	. 1
2	Pinning information	.2
3	Ordering information	.2
4	Limiting values	.2
5	Thermal characteristics	.4
6	Characteristics	.5
7	Package outline	.9
8	Revision history1	0
9	Legal information1	11
9.1	Data sheet status	11
9.2	Definitions	11
9.3	Disclaimers	11
9.4	Trademarks	
10	Contact information	14

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