MOSPEC

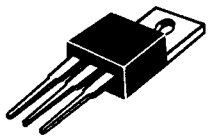
PNP SILICON POWER TRANSISTORS

.... designed for use in general purpose Power amplifier,vertical output application

FEATURES:
* Collector-Emitter Voltage
  V_{CEO}= 150V(Min)
* DC Current Gain
  hFE= 40-200@I_C= 400mA
* Complementary to PNP 2SB546A

NPN
2SD401A

2 AMPERE
POWER
TRANASISTORS
150 VOLTS
25 WATTS



TO-220

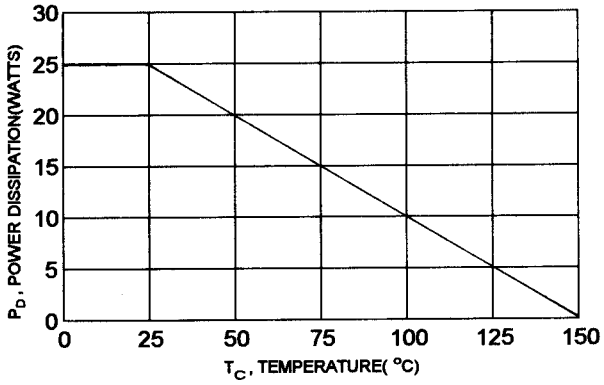
MAXIMUM RATINGS

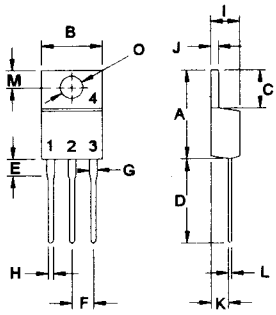
Characteristic	Symbol	2SD401A	Unit
Collector-Emitter Voltage	V_{CEO}	150	V
Collector-Base Voltage	V_{CBO}	200	V
Emitter-Base Voltage	V_{EBO}	5.0	V
Collector Current - Continuous - Peak	I_C I_{CM}	2.0 3.0	A
Total Power Dissipation @T_C = 25°C Derate above 25°C	P_D	25 0.2	W W/°C
Operating and Storage Junction Temperature Range	T_J , T_{STG}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Case	Rθjc	5.0	°C/W

FIGURE -1 POWER DERATING





PIN 1.BASE
2.COLLECTOR
3.EMITTER
4.COLLECTOR(CASE)

DIM	MILLIMETERS	
	MIN	MAX
A	14.68	15.31
B	9.78	10.42
C	5.01	6.52
D	13.06	14.62
E	3.57	4.07
F	2.42	3.66
G	1.12	1.36
H	0.72	0.96
I	4.22	4.98
J	1.14	1.38
K	2.20	2.97
L	0.33	0.55
M	2.48	2.98
O	3.70	3.90

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

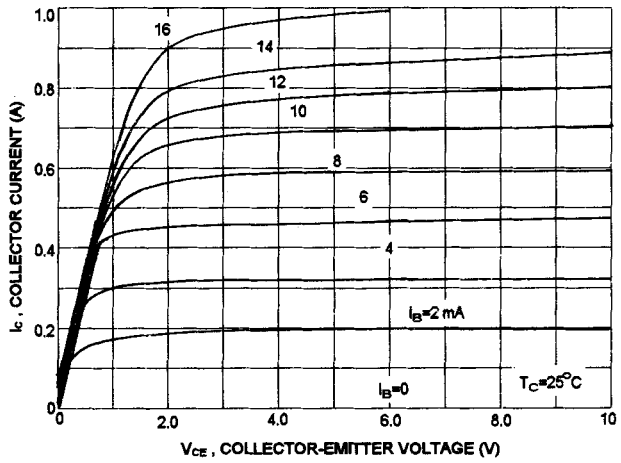
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector Cutoff Current (V_{CB}= 150 V, I_E= 0)	I_{CBO}		50	uA
Emitter Cutoff Current (V_{EB}= 4.0 V, I_C= 0)	I_{EBO}		50	uA
ON CHARACTERISTICS (1)				
DC Current Gain * (I_C= 0.4 A, V_{CE}= 10 V)	hFE(2)	40	200	
Collector-Emitter Saturation Voltage (I_C= 0.5 A, I_B= 50 mA)	$V_{CE(sat)}$		1.0	V
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product (I_C = 0.4 A, V_{CE} = 10 V, f = 1.0 MHz)	f_T	5.0(typ)		MHz

(1) Pulse Test: Pulse Width =300 us,Duty Cycle ≦ 2.0%

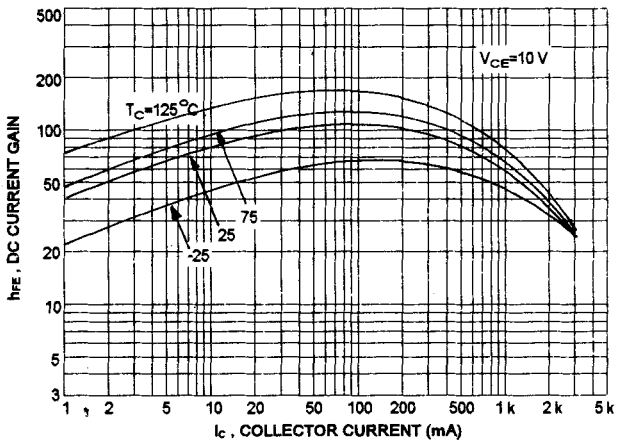
* hFE(2) Classification:

40	M	80	60	L	120	100	K	200

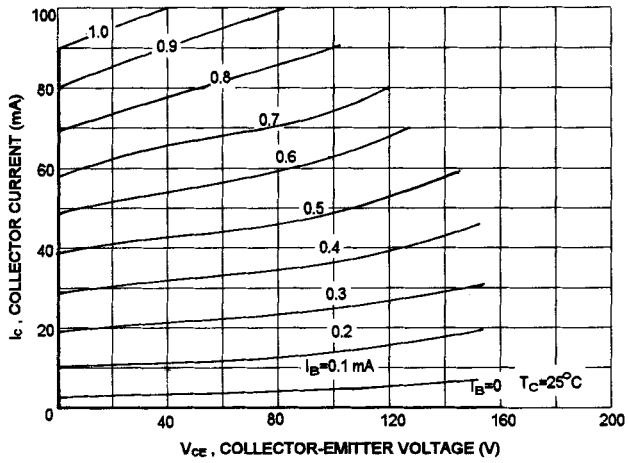
Ic - Vce



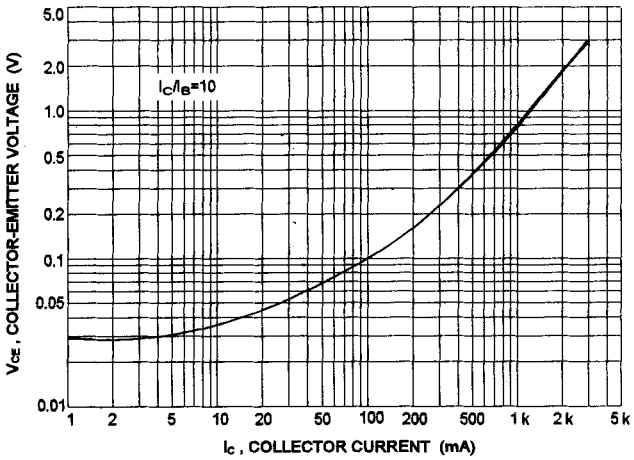
DC CURRENT GAIN



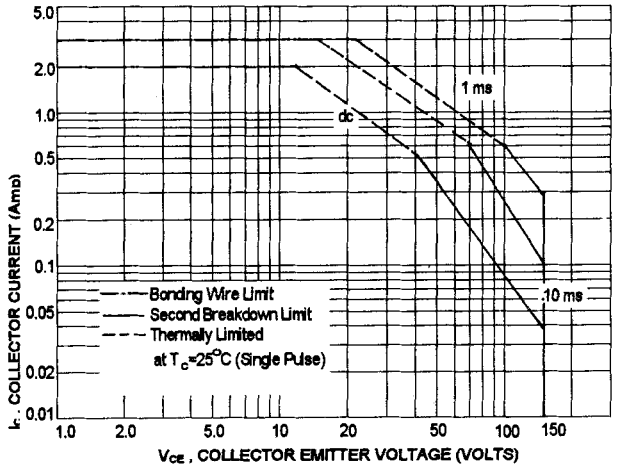
Ic - Vce



Vce-Ic



ACTIVE-REGION SAFE OPERATING AREA (SOA)



There are two limitation on the power handling ability of a transistor:average junction temperature and second breakdown safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than curves indicate.

The data of SOA curve is base on $T_{J(PK)}$=150 °C;T_C is variable depending on conditions. second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(PK)}$≤150°C,At high case temperatures, thermal limita - tion will reduce the power that can be handled to values less than the limitations imposed by second breakdown.