

### SWITCHING P-CHANNEL POWER MOS FET INDUSTRIAL USE

#### DESCRIPTION

This product is P-Channel MOS Field Effect Transistor designed for high current switching applications.

#### ORDERING INFORMATION

PART NUMBER	PACKAGE
2SJ493	Isolated TO-220

#### FEATURES

- Super low on-state resistance  
 $R_{DS(on)1} = 100 \text{ m}\Omega$  (MAX.) ( $V_{GS} = -10 \text{ V}$ ,  $I_D = -8 \text{ A}$ )  
 $R_{DS(on)2} = 185 \text{ m}\Omega$  (MAX.) ( $V_{GS} = -4 \text{ V}$ ,  $I_D = -8 \text{ A}$ )
- Low  $C_{iss}$ :  $C_{iss} = 1210 \text{ pF}$  (TYP.)
- Built-in gate protection diode

#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	-60	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS(AC)}$	$\mp 20$	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ ) <sup>Note1</sup>	$V_{GSS(DC)}$	-20, 0	V
Drain Current (DC)	$I_{D(DC)}$	$\mp 16$	A
Drain Current (pulse) <sup>Note2</sup>	$I_{D(pulse)}$	$\mp 64$	A
Total Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_T$	30	W
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ )	$P_T$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$
Single Avalanche Current <sup>Note3</sup>	$I_{AS}$	-16	A
Single Avalanche Energy <sup>Note3</sup>	$E_{AS}$	25.6	mJ

- Notes**
1.  $f = 20 \text{ kHz}$ , Duty Cycle  $\leq 10\%$  (+Side)
  2.  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$
  3. Starting  $T_{ch} = 25^\circ\text{C}$ ,  $R_A = 25 \Omega$ ,  $V_{GS} = -20 \text{ V} \rightarrow 0$

#### THERMAL RESISTANCE

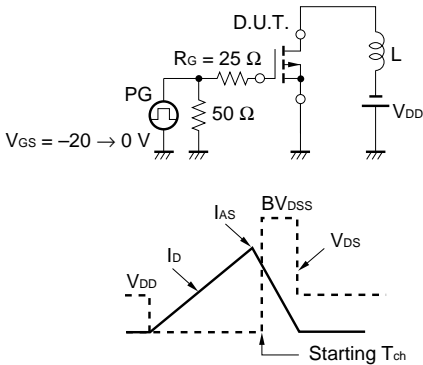
Channel to Case	$R_{th(ch-C)}$	4.17	$^\circ\text{C/W}$
Channel to Ambient	$R_{th(ch-A)}$	62.5	$^\circ\text{C/W}$

The information in this document is subject to change without notice.

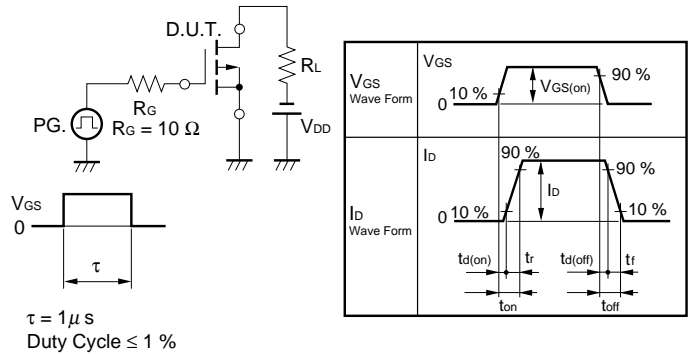
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -8 A		70	100	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = -4 V, I <sub>D</sub> = -8 A		120	185	mΩ
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 mA	-1.0	-1.5	-2.0	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -8 A	5.0	11		S
Drain Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0 V			-10	μA
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V, V <sub>DS</sub> = 0 V			± 10	μA
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -10 V		1210		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		520		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		180		pF
Turn-on Delay Time	t <sub>d(on)</sub>	I <sub>D</sub> = -8 A		15		ns
Rise Time	t <sub>r</sub>	V <sub>GS(on)</sub> = -10 V		130		ns
Turn-off Delay Time	t <sub>d(off)</sub>	V <sub>DD</sub> = -30 V		95		ns
Fall Time	t <sub>f</sub>	R <sub>G</sub> = 10 Ω		80		ns
Total Gate Charge	Q <sub>G</sub>	I <sub>D</sub> = -16 A		42		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>DD</sub> = -48 V		8.0		nC
Gate to Drain Charge	Q <sub>GD</sub>	V <sub>GS</sub> = -10 V		10		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 16 A, V <sub>GS</sub> = 0 V		1.0		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 16 A, V <sub>GS</sub> = 0 V		120		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 50 A/μs		230		nC

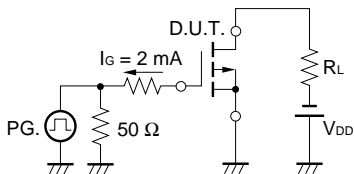
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



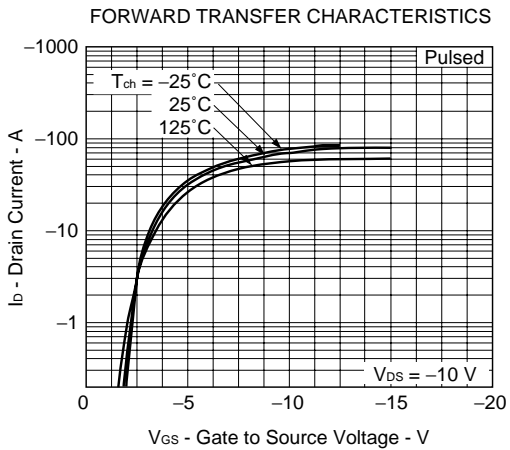
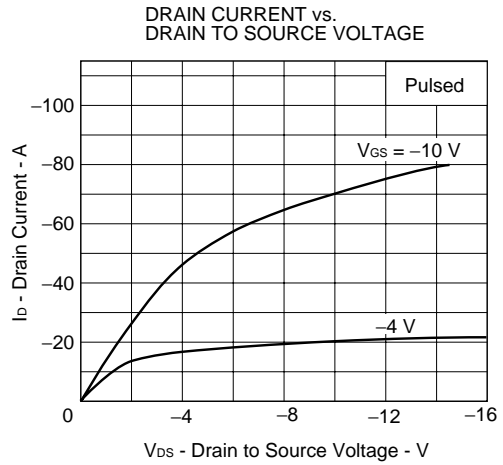
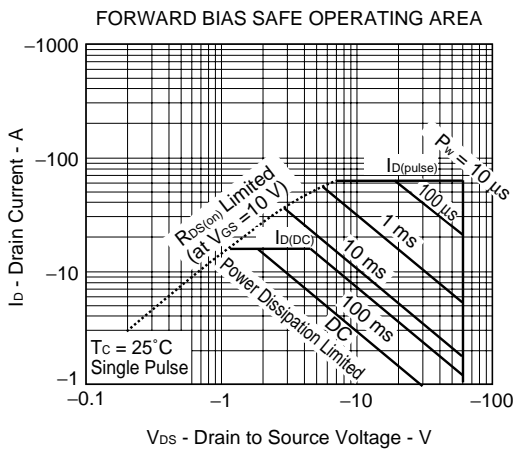
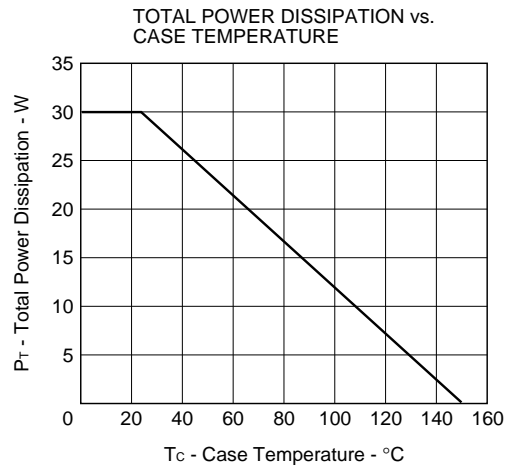
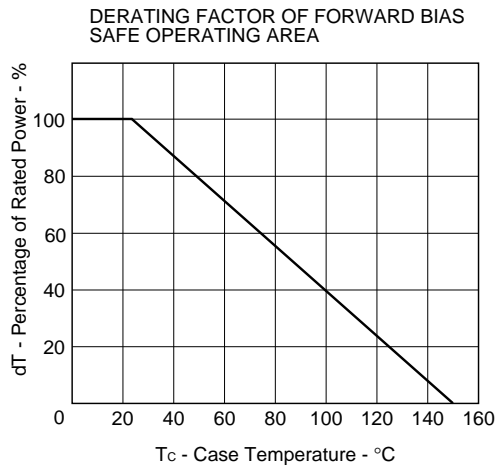
**TEST CIRCUIT 2 SWITCHING TIME**



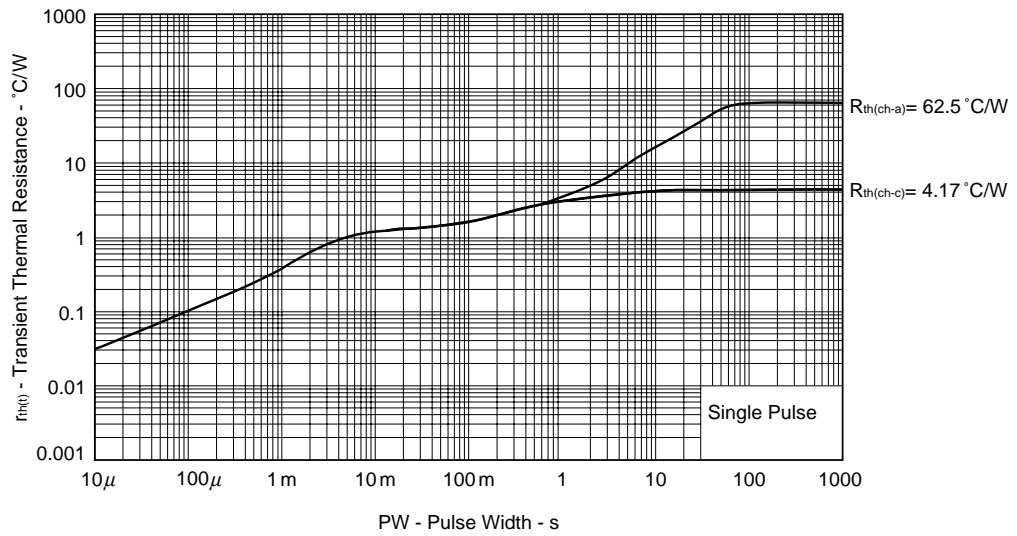
**TEST CIRCUIT 3 GATE CHARGE**



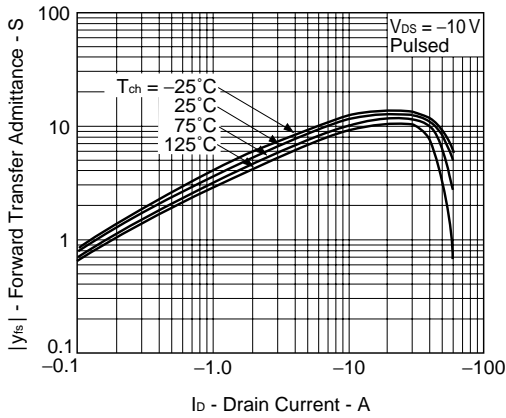
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)



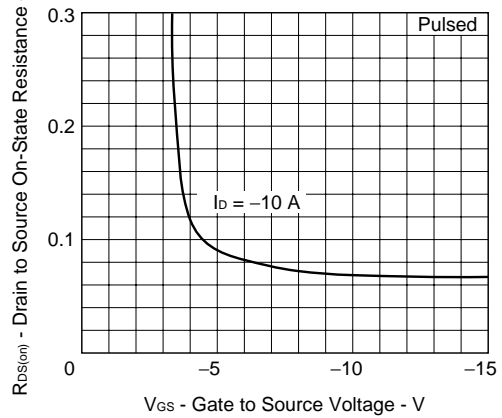
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



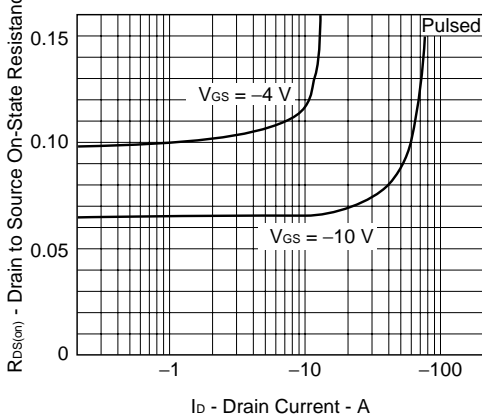
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



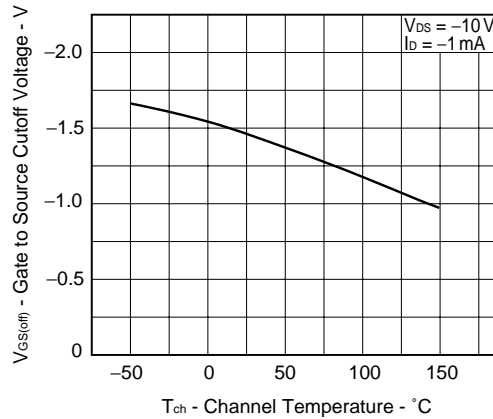
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



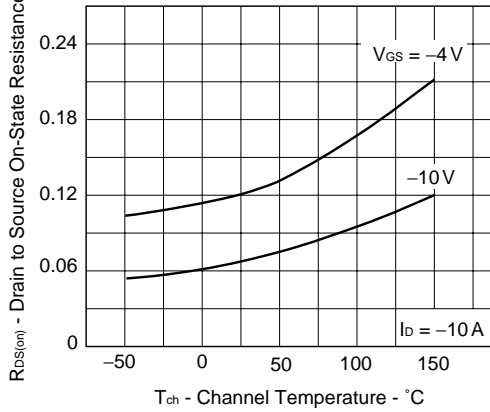
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



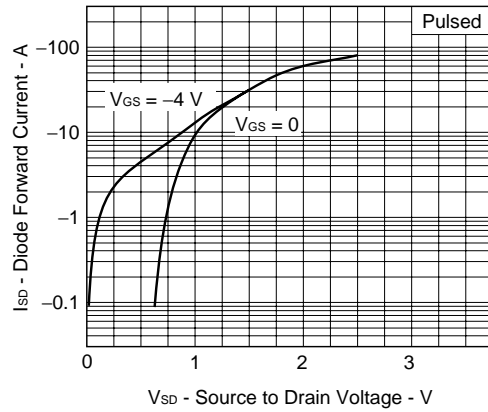
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



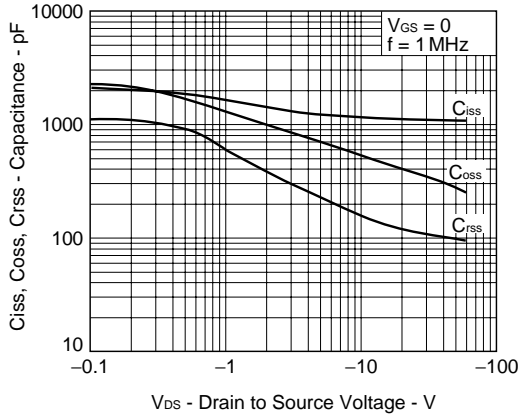
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



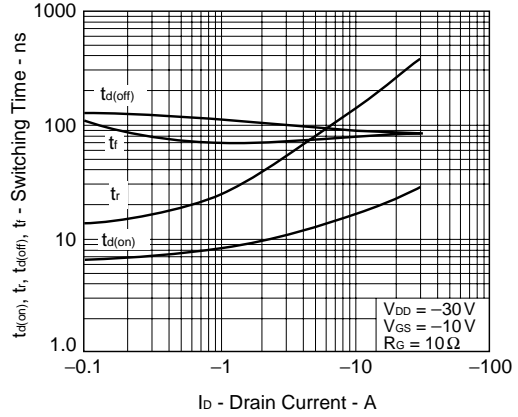
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



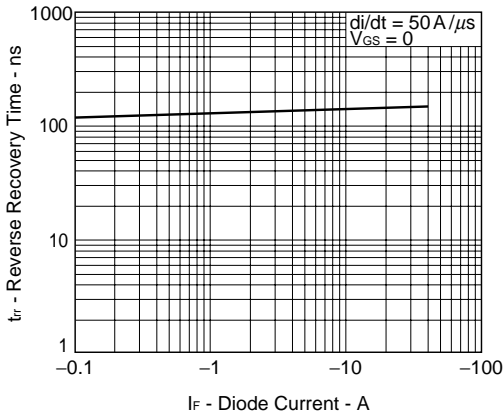
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



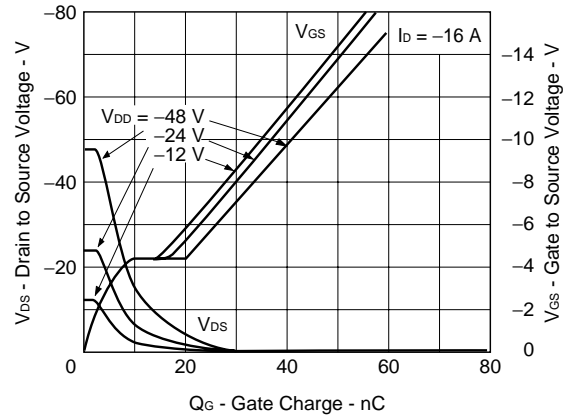
SWITCHING CHARACTERISTICS

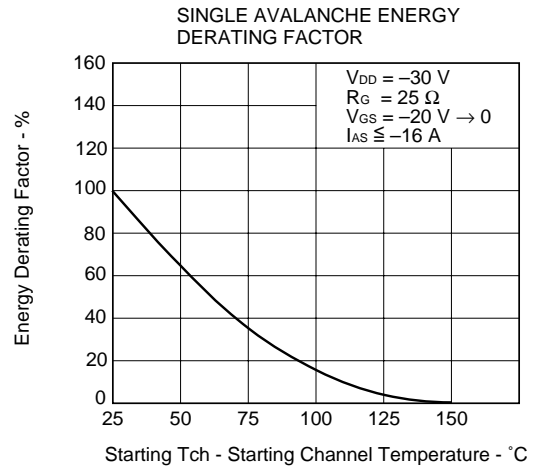
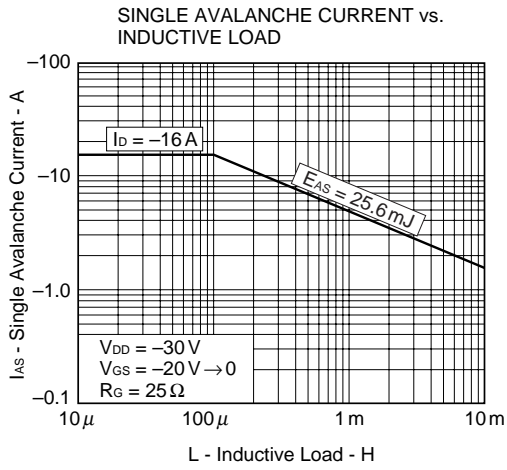


REVERSE RECOVERY TIME vs. DRAIN CURRENT



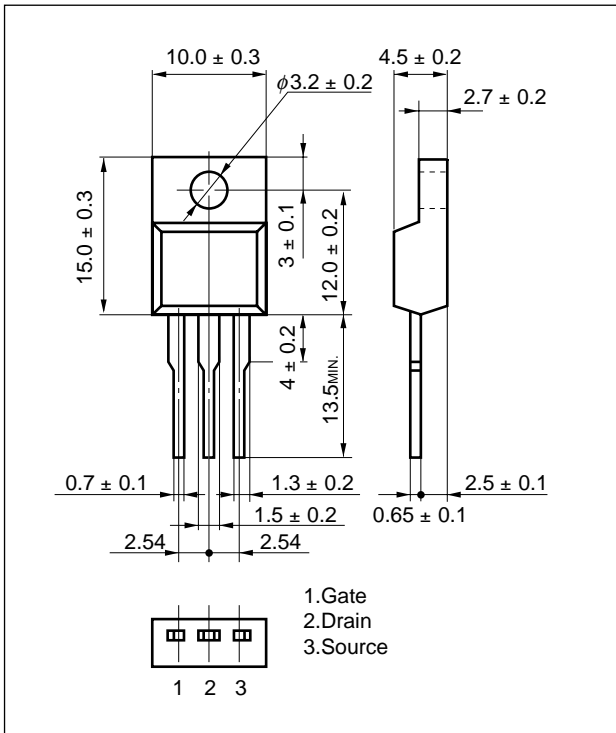
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



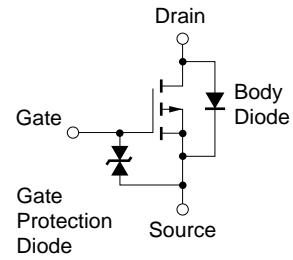


PACKAGE DRAWING (Unit: mm)

Isolated TO-220(MP-45F)



EQUIVALENT CIRCUIT



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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