

SWITCHING P-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

This product is P-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Super Low On-State Resistance
 $R_{DS(on)1} = 30 \text{ m}\Omega \text{ MAX. (} V_{GS} = -10 \text{ V, } I_D = -15 \text{ A)}$
 $R_{DS(on)2} = 56 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4 \text{ V, } I_D = -15 \text{ A)}$
- Low C_{iss} $C_{iss} = 4120 \text{ pF TYP.}$
- Built-in Gate Protection Diode

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage	V_{DSS}	-60	V
Gate to Source Voltage*	$V_{GSS(AC)}$	± 20	V
Gate to Source Voltage	$V_{GSS(DC)}$	-20, 0	V
Drain Current (DC)	$I_{D(DC)}$	± 30	A
Drain Current (pulse)**	$I_{D(pulse)}$	± 120	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_T	35	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_T	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

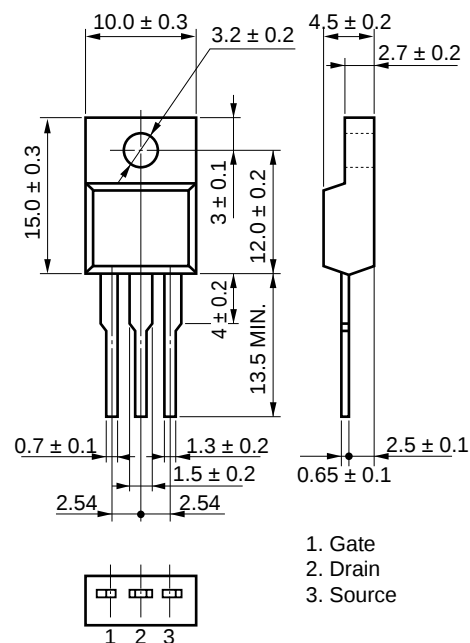
*f = 20 kHz, Duty Cycle $\leq 10\%$ (+Side)

**PW $\leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

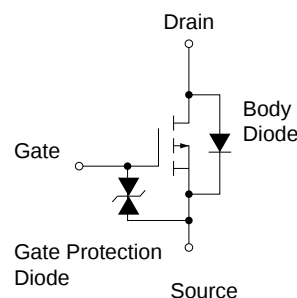
THERMAL RESISTANCE

Channel to Case	$R_{th(ch-c)}$	3.57	$^\circ\text{C/W}$
Channel to Ambient	$R_{th(ch-A)}$	62.5	$^\circ\text{C/W}$

PACKAGE DIMENSIONS (in millimeter)



MP-45F (ISOLATED TO-220)

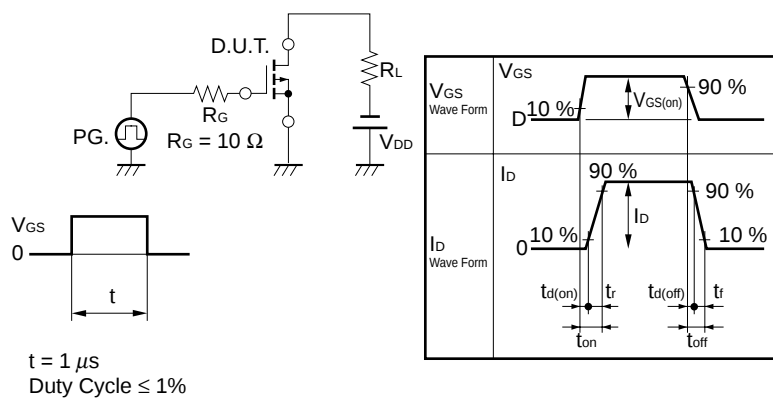


The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device acutally used, an additional protection circiut is externally required if a voltage exceeding the rated voltage may be applied to this device.

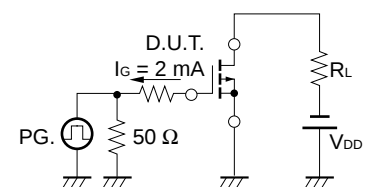
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

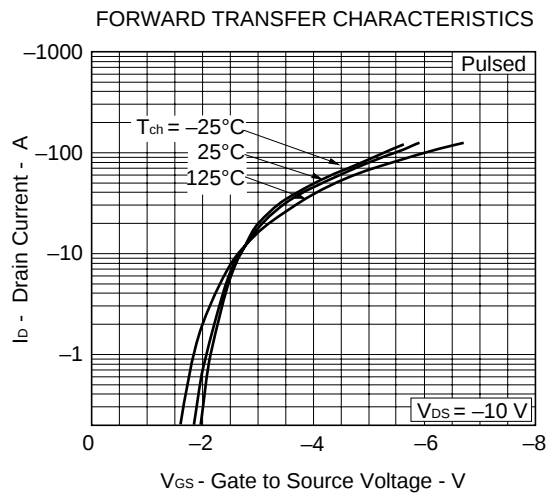
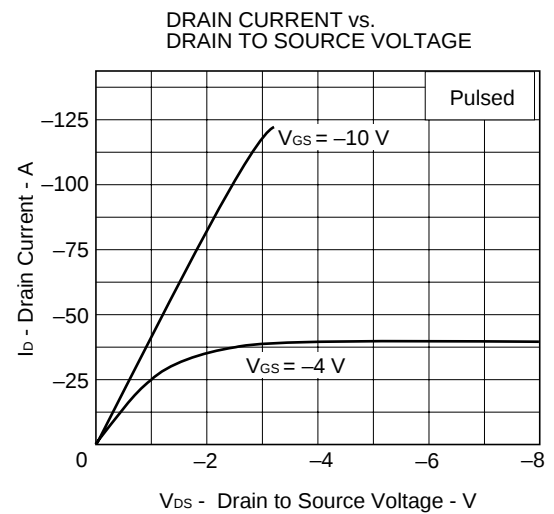
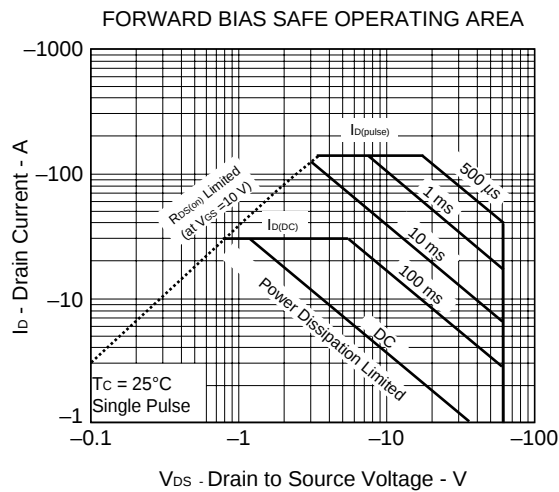
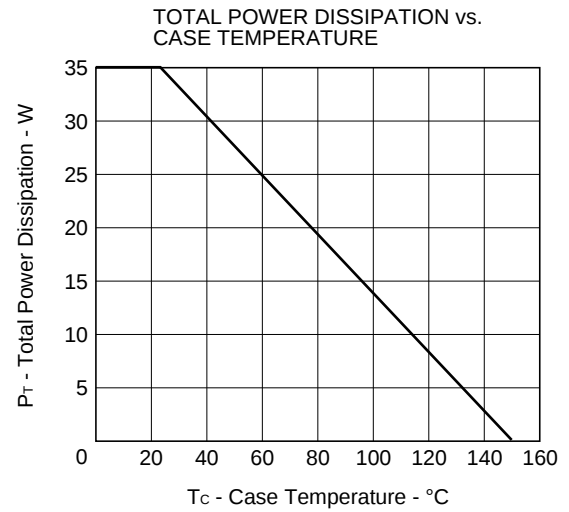
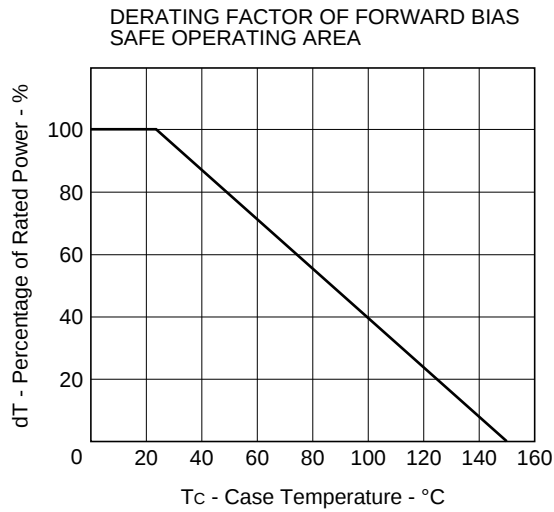
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = -10 V, I _D = -15 A		24	30	mΩ
	R _{DS(on)2}	V _{GS} = -4 V, I _D = -15 A		38	56	mΩ
Gate to Source Cutoff Voltage	V _{GS(off)}	V _{DS} = -10 V, I _D = -1 mA	-1.0	-1.5	-2.0	V
Forward Transfer Admittance	y _{fs}	V _{DS} = -10 V, I _D = -15 A	12	24		S
Drain Leakage Current	I _{DSS}	V _{DS} = -60 V, V _{GS} = 0			-10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0			±10	μA
Input Capacitance	C _{iss}	V _{DS} = -10 V		4120		pF
Output Capacitance	C _{oss}	V _{GS} = 0		1750		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		580		pF
Turn-On Delay Time	t _{d(on)}	I _D = -15 A		40		ns
Rise Time	t _r	V _{GS(on)} = -10 V		220		ns
Turn-Off Delay Time	t _{d(off)}	V _{DD} = -30 V		600		ns
Fall Time	t _f	R _G = 10 Ω		380		ns
Total Gate Charge	Q _G	I _D = -30 A		140		nC
Gate to Source Charge	Q _{GS}	V _{DD} = -48 V		12		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = -10 V		46		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 30 A, V _{GS} = 0		0.8	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 30 A, V _{GS} = 0		160		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		400		nC

Test Circuit 1 Switching Time

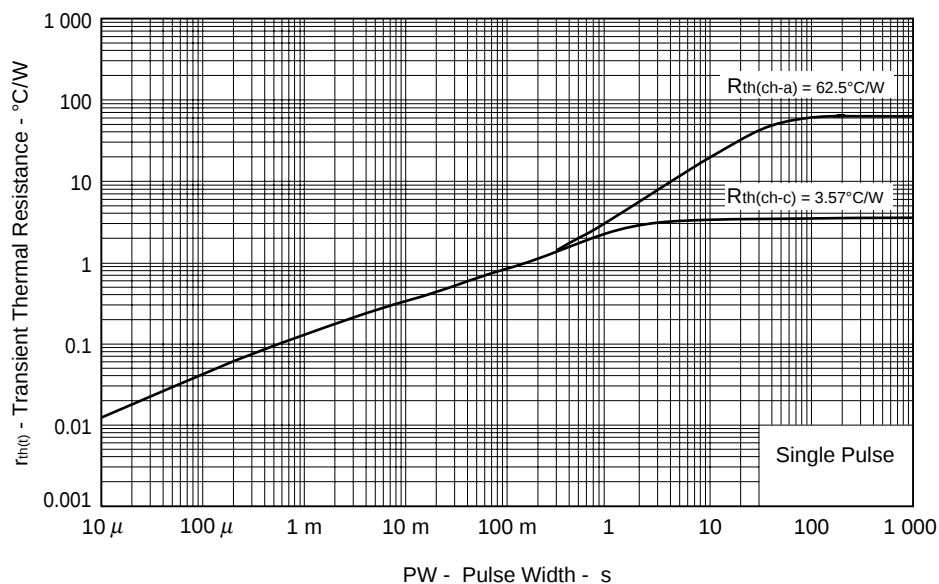


Test Circuit 2 Gate Charge

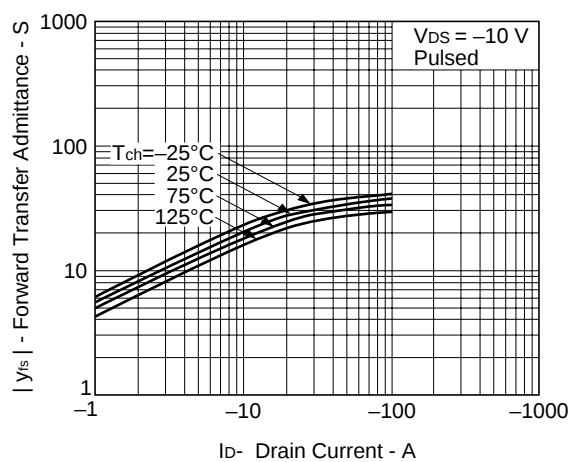




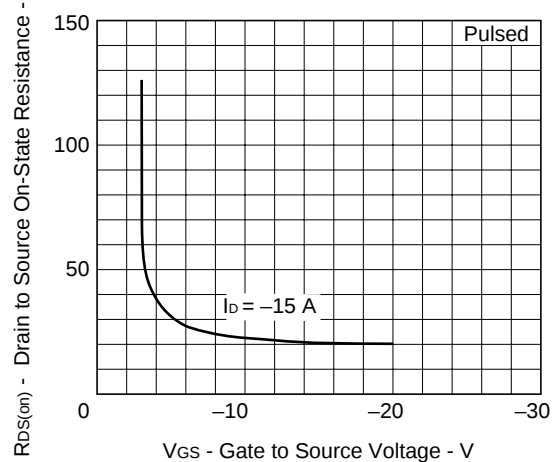
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



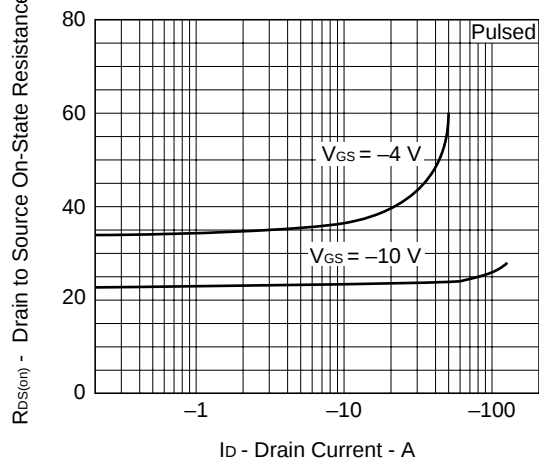
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



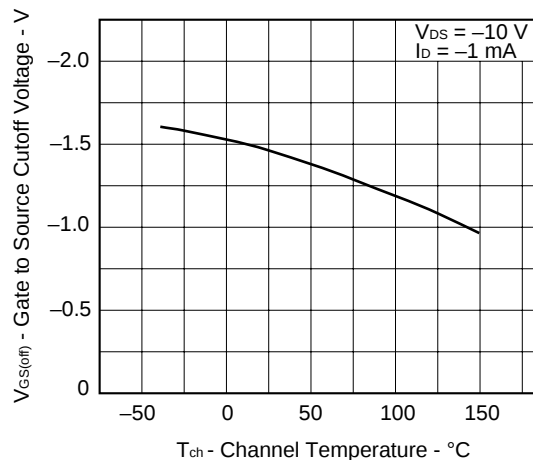
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

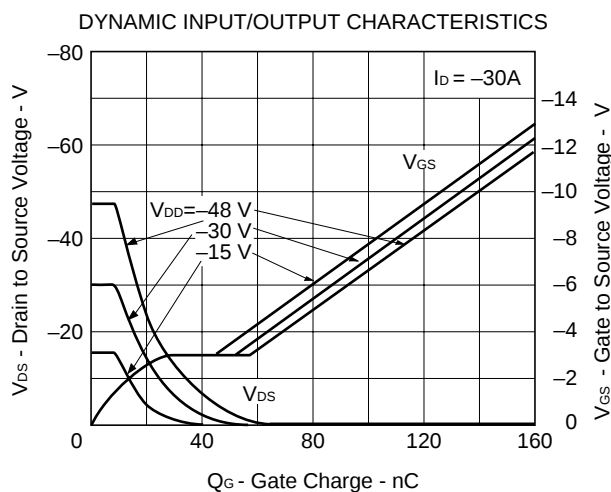
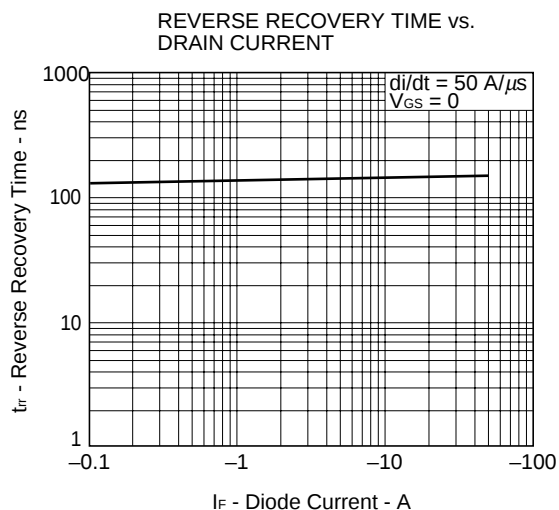
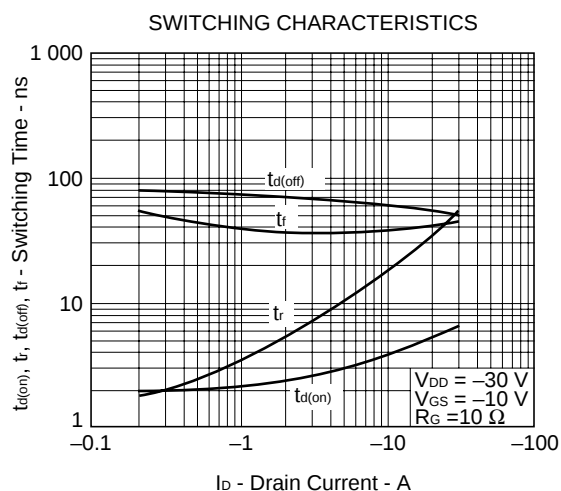
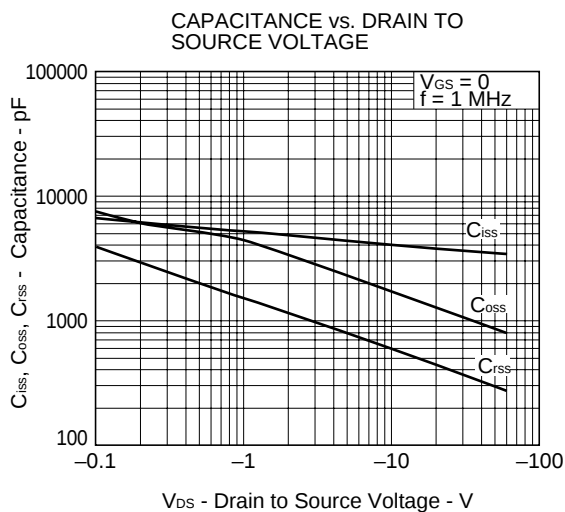
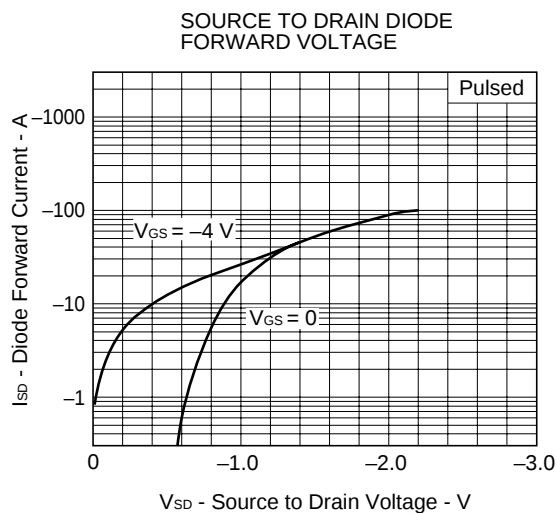
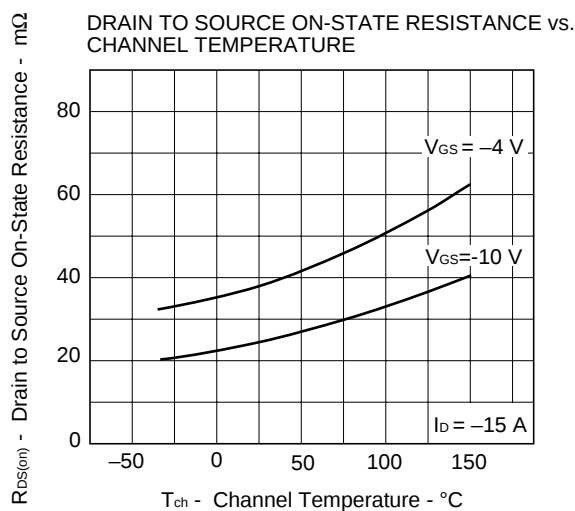


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





Document Name	Document No.
NEC semiconductor device reliability/quality control system	C11745E
Power MOS FET features and application to switching power supply	D12971E
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037
Guide to prevent damage for semiconductor devices by electrostatic discharge (EDS)	C11892E

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Anti-radioactive design is not implemented in this product.