

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR

2SK1285

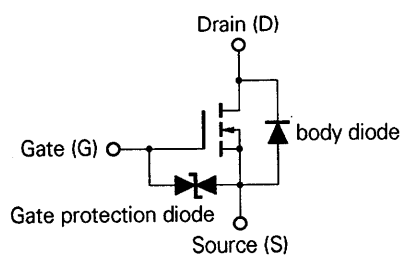
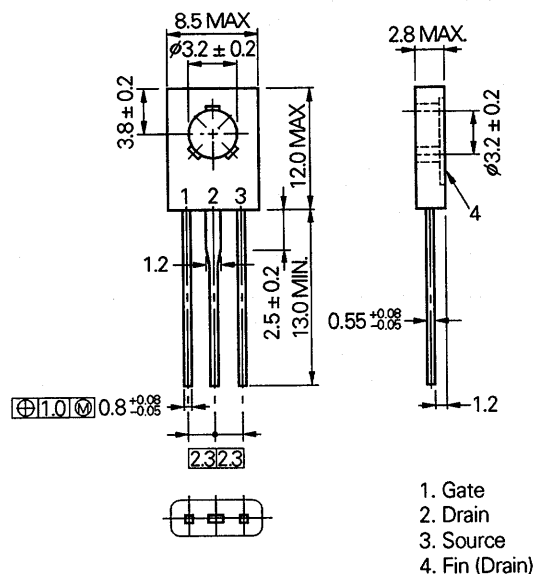
SWITCHING

N-CHANNEL POWER MOS FET

INDUSTRIAL USE

PACKAGE DIMENSIONS

(in millimeters)



DESCRIPTION

The 2SK1285 is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} \leq 0.32 \Omega$ MAX. ($V_{GS} = 10 V$, $I_D = 2 A$)
 $R_{DS(on)} \leq 0.40 \Omega$ MAX. ($V_{GS} = 4 V$, $I_D = 2 A$)
- Low C_{iss} $C_{iss} = 500 pF$ TYP.
- Built-in G-S Gate Protection Diodes

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature	-55 to +150 °C
Channel Temperature	150 °C MAX.

Maximum Power Dissipation

Total Power Dissipation ($T_a = 25 °C$)	1.3	W
Total Power Dissipation ($T_c = 25 °C$)	20	W

Maximum Voltages and Currents ($T_a = 25 °C$)

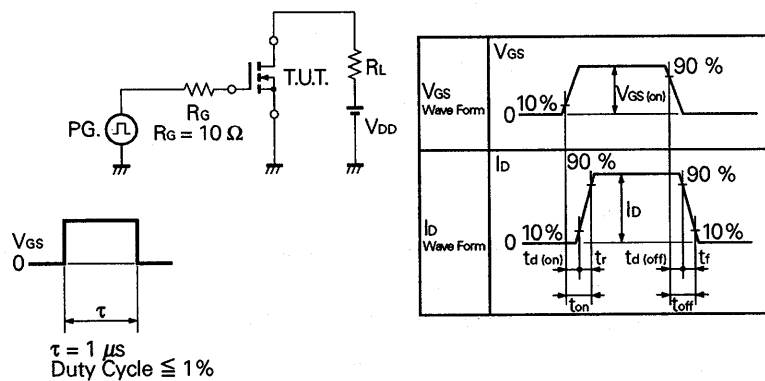
V_{DSS}	Drain to Source Voltage	100	V
$V_{GSS(AC)}$	Gate to Source Voltage	±20	V
$I_{D(DC)}$	Drain Current (DC)	±3.0	A
$I_{D(pulse)*}$	Drain Current (pulse)	±12	A

* $PW \leq 10 \mu s$, Duty Cycle $\leq 1 \%$

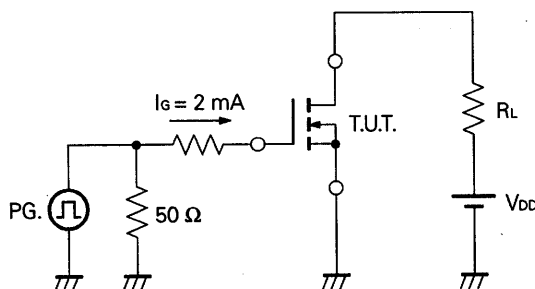
ELECTRICAL CHARACTERISTICS ($T_a = 25\text{ }^{\circ}\text{C}$)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		0.26	0.32	Ω	$V_{GS} = 10\text{ V}$, $I_D = 2\text{ A}$
Drain to Source On-state Resistance	$R_{DS(on)}$		0.32	0.40	Ω	$V_{GS} = 4.0\text{ V}$, $I_D = 2\text{ A}$
Gate to Source Cutoff Voltage	$V_{GS(off)}$	1.0		2.5	V	$V_{DS} = 10\text{ V}$, $I_D = 1\text{ mA}$
Forward Transfer Admittance	$ y_{fs} $	2.4			S	$V_{DS} = 10\text{ V}$, $I_D = 2\text{ A}$
Drain Leakage Current	I_{DSS}			10	μA	$V_{DS} = 100\text{ V}$, $V_{GS} = 0$
Gate to Source Leakage Current	I_{GSS}			± 10	μA	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0$
Input Capacitance	C_{iss}		500		pF	$V_{DS} = 10\text{ V}$ $V_{GS} = 0$ $f = 1\text{ MHz}$
Output Capacitance	C_{oss}		160		pF	
Reverse Transfer Capacitance	C_{rss}		20		pF	
Turn-On Delay Time	$t_{d(on)}$		40		ns	$V_{GS(on)} = 10\text{ V}$ $V_{DD} = 50\text{ V}$ $I_D = 2\text{ A}$, $R_G = 10\text{ }\Omega$ $R_L = 25\text{ }\Omega$
Rise Time	t_r		55		ns	
Turn-Off Delay Time	$t_{d(off)}$		500		ns	
Fall Time	t_f		120		ns	
Total Gate Charge	Q_G		13		nC	$V_{GS} = 10\text{ V}$ $I_D = 3\text{ A}$ $V_{DD} = 80\text{ V}$
Gate to Source Charge	Q_{GS}		3		nC	
Gate to Drain Charge	Q_{GD}		2		nC	
Diode Forward Voltage	V_{SD}		0.9		V	$I_{SD} = 3\text{ A}$, $V_{GS} = 0$
Reverse Recovery Time	t_{rr}		140		ns	$I_F = 3\text{ A}$, $V_{GS} = 0$
Reverse Recovery Charge	Q_{rr}		250		nC	$di/dt = 50\text{ A}/\mu\text{s}$

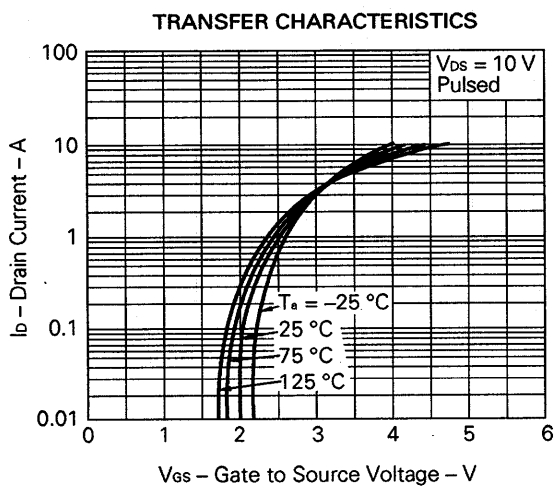
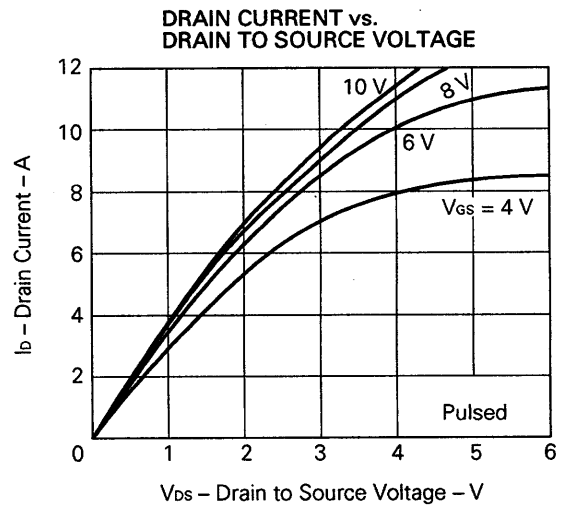
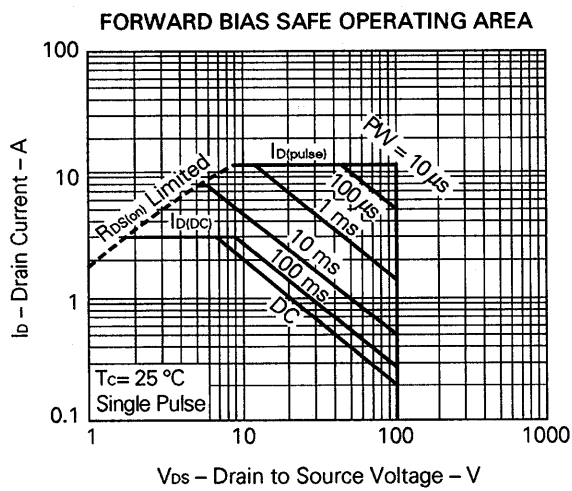
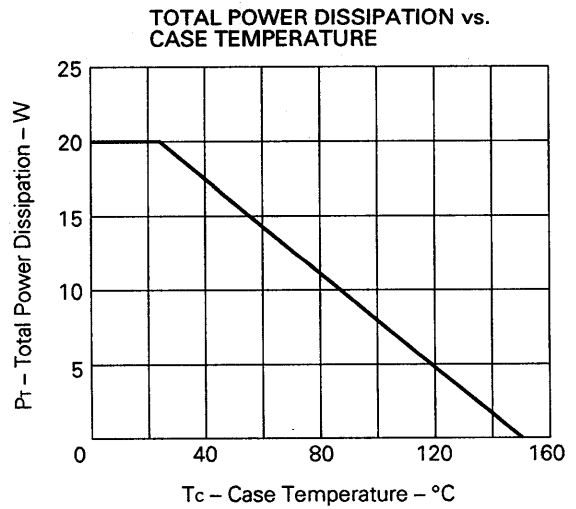
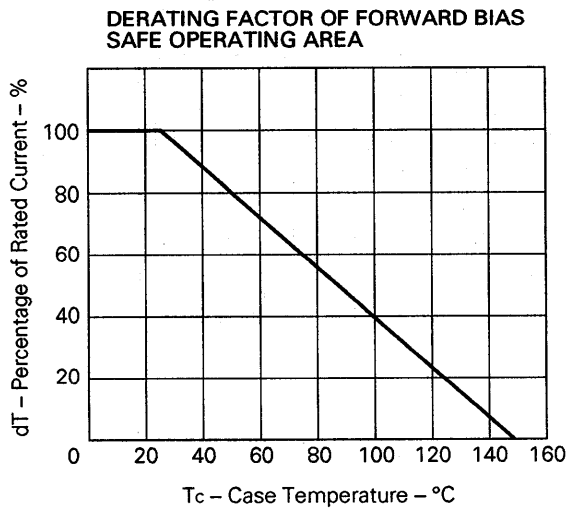
Test Circuit 1: Switching Time

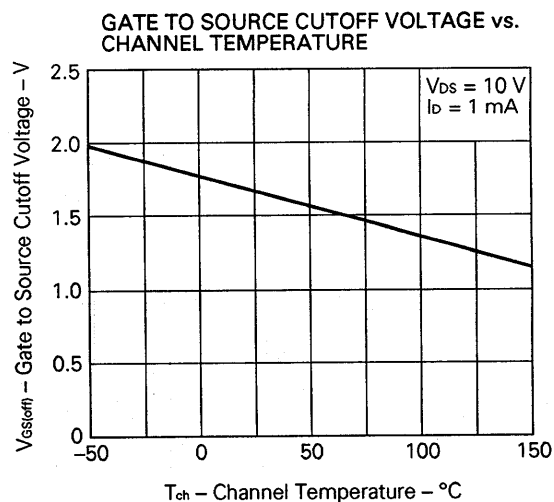
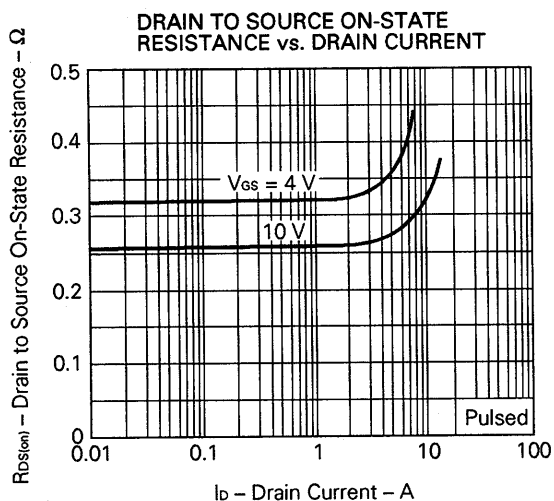
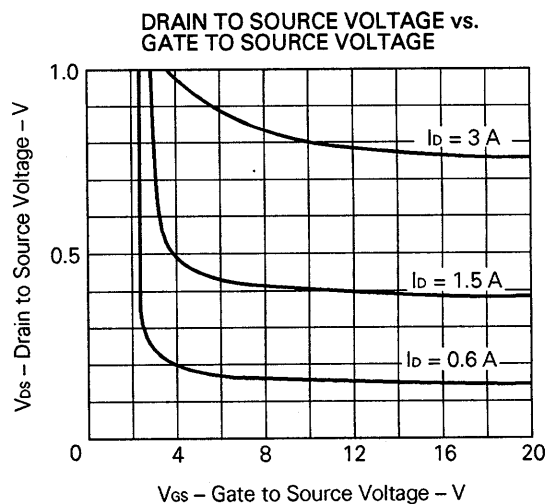
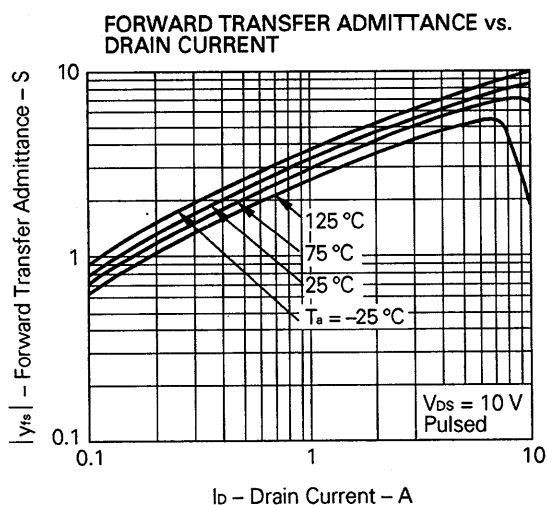
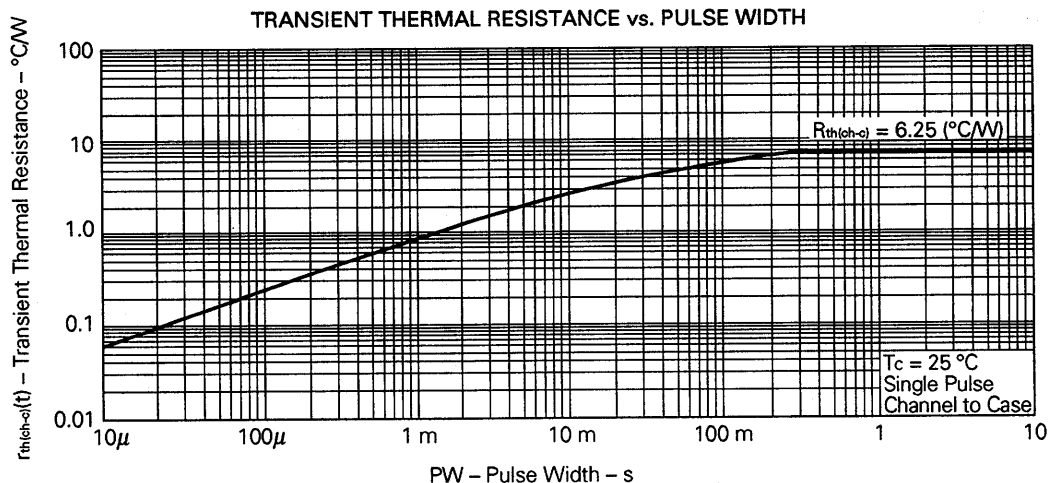


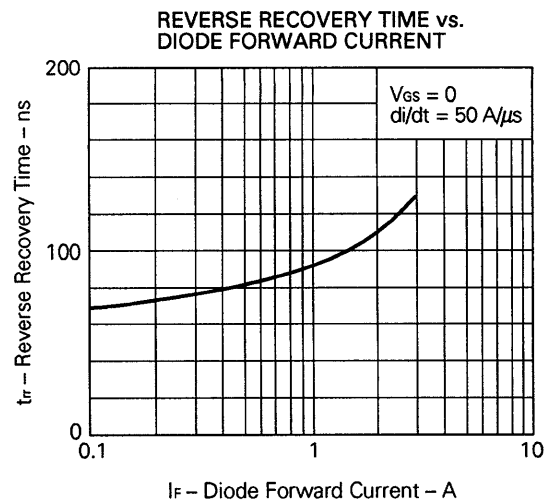
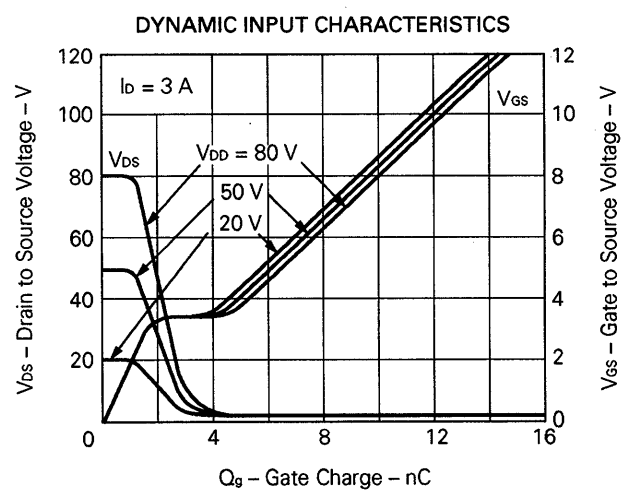
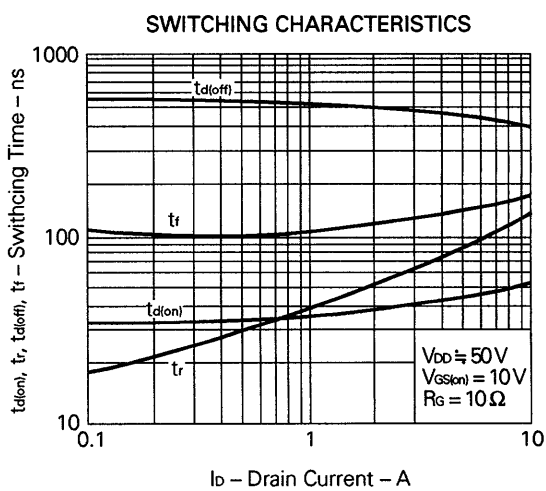
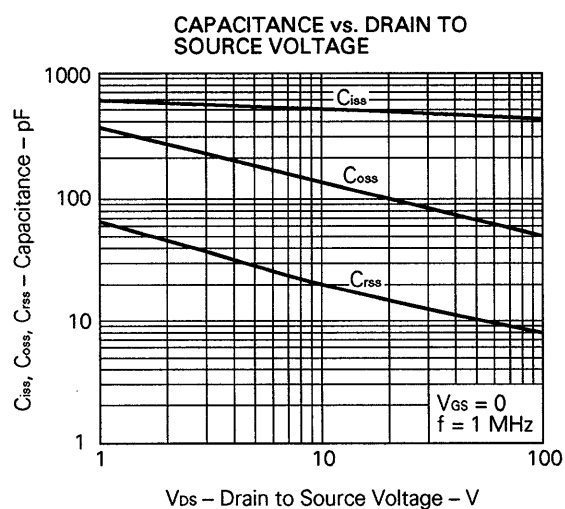
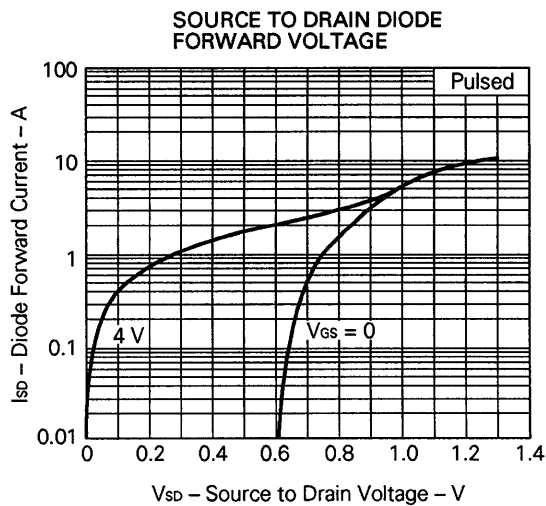
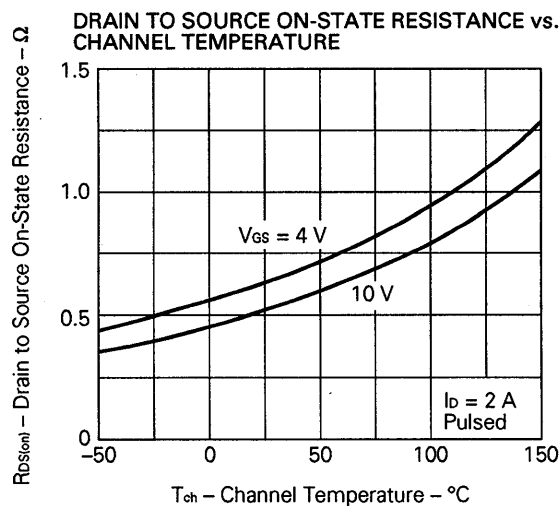
Test Circuit 2: Gate Charge



TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)







Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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