

MOS FIELD EFFECT POWER TRANSISTOR

2SK2040, 2SK2040-Z

SWITCHING

N-CHANNEL POWER MOS FET

INDUSTRIAL USE

DESCRIPTION

The 2SK2040 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} \leq 5.0 \Omega$ ($V_{GS} = 10 \text{ V}$, $I_D = 1.0 \text{ A}$)
- Low C_{iss} $C_{iss} = 275 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diode
- High Avalanche Capability Ratings

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ \text{C}$)

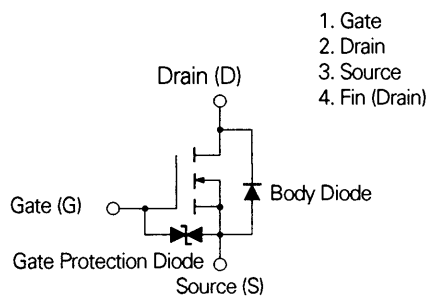
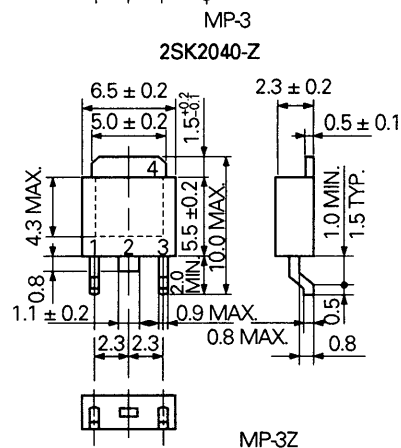
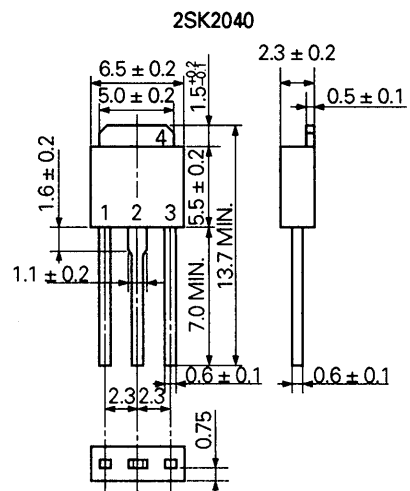
Drain to Source Voltage	V_{DSS}	600	V
Gate to Source Voltage	V_{GSS}	± 30	V
Drain Current (DC)	$I_{D(DC)}$	± 2.0	A
Drain Current (pulse)	$I_{D(pulse)}^*$	± 6.0	A
Total Power Dissipation ($T_C = 25^\circ \text{C}$)	P_{T1}	20	W
Total Power Dissipation ($T_a = 25^\circ \text{C}$)	P_{T2}	1.0	W
Channel Temperature	T_{ch}	150	$^\circ \text{C}$
Storage Temperature	T_{stg}	-55 to $+150$	$^\circ \text{C}$
Single Avalanche Current	I_{AS}^{**}	3.0	A
Single Avalanche Energy	E_{AS}^{**}	78	mJ

* $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

** Starting $T_{ch} = 25^\circ \text{C}$, $R_G = 25 \Omega$, $V_{GS} = 20 \text{ V} \rightarrow 0$

PACKAGE DIMENSIONS

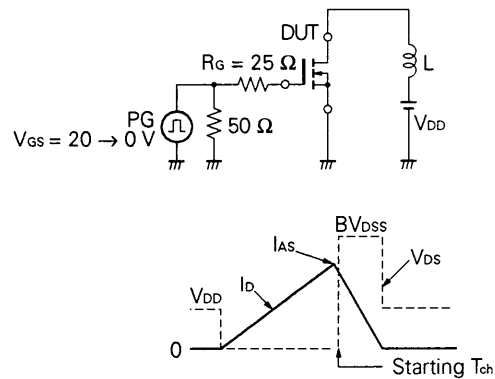
(in millimeters)



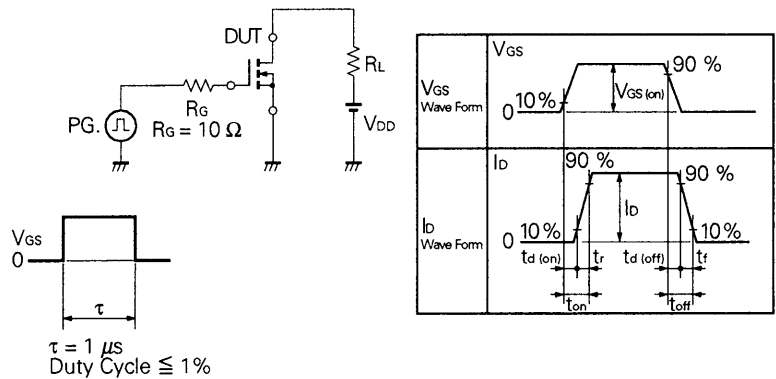
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R _{DS(on)}		4.2	5.0	Ω	V _{GS} = 10 V, I _D = 1 A
Gate to Source Cutoff Voltage	V _{GS(off)}	2.0		4.0	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	0.5			S	V _{DS} = 20 V, I _D = 1 A
Drain Leakage Current	I _{DSS}			100	μA	V _{DS} = 600 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±25 V, V _{DS} = 0
Input Capacitance	C _{iss}		275		pF	V _{DS} = 10 V V _{GS} = 0 f = 1 MHz
Output Capacitance	C _{oss}		68		pF	
Reverse Transfer Capacitance	C _{rss}		23		pF	
Turn-On Delay Time	t _{d(on)}		7		ns	V _{GS} = 10 V V _{DD} = 150 V I _D = 1.0 A, R _G = 10 Ω R _L = 150 Ω
Rise Time	t _r		4		ns	
Turn-Off Delay Time	t _{d(off)}		37		ns	
Fall Time	t _f		8		ns	
Total Gate Charge	Q _G		12		nC	V _{GS} = 10 V I _D = 2 A V _{DD} = 450 V
Gate to Source Charge	Q _{GS}		2.2		nC	
Gate to Drain Charge	Q _{GD}		6.2		nC	
Diode Forward Voltage	V _{F(S-D)}		0.9		V	I _F = 2 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		340		ns	I _F = 2 A di/dt = 50 A/μs
Reverse Recovery Charge	Q _{rr}		1.1		μC	

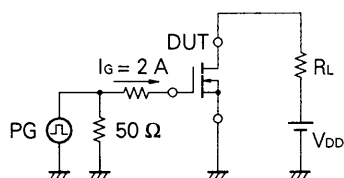
Test Circuit 1: Avalanche Capability



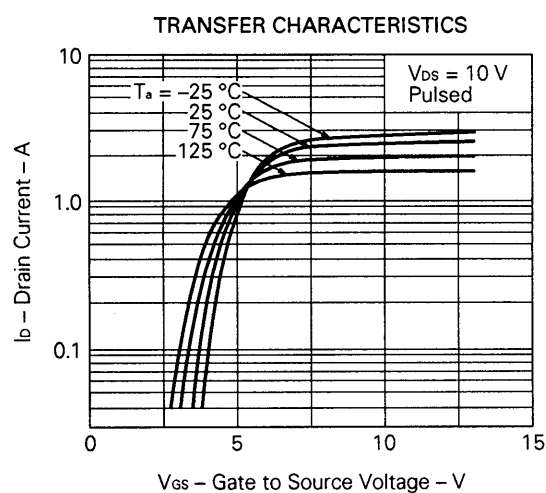
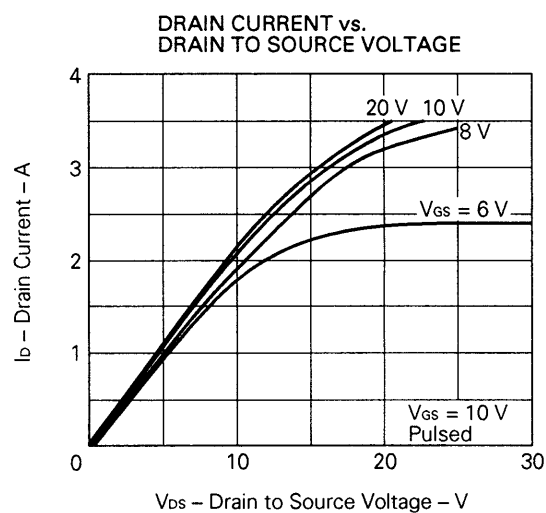
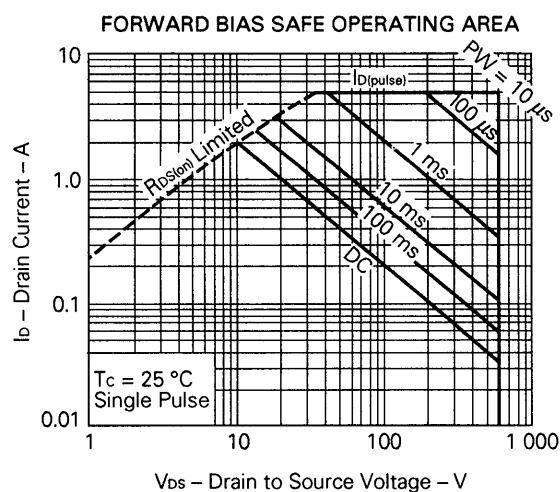
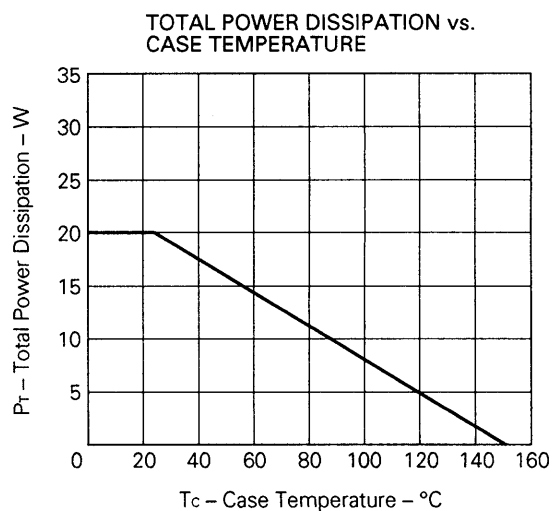
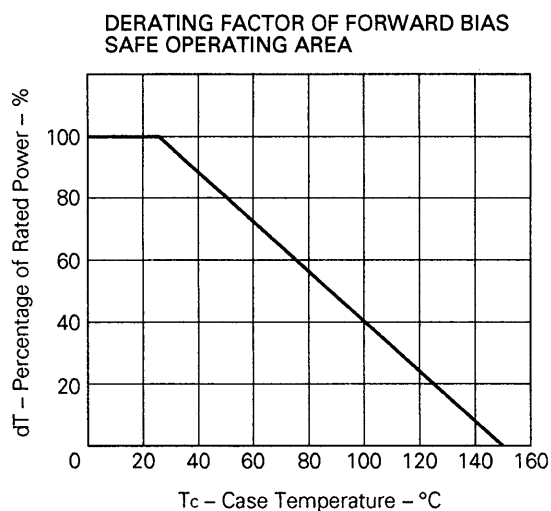
Test Circuit 2: Switching Time

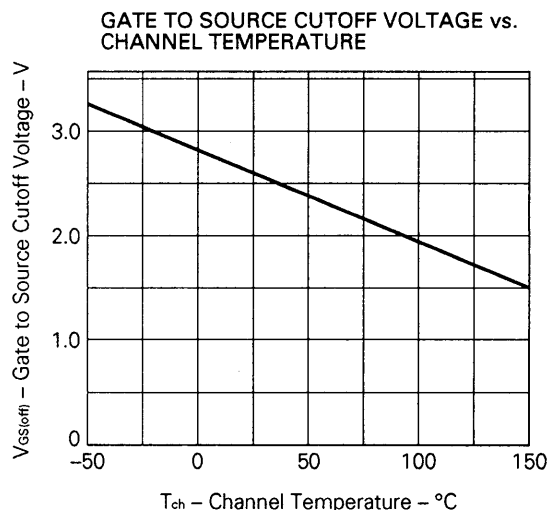
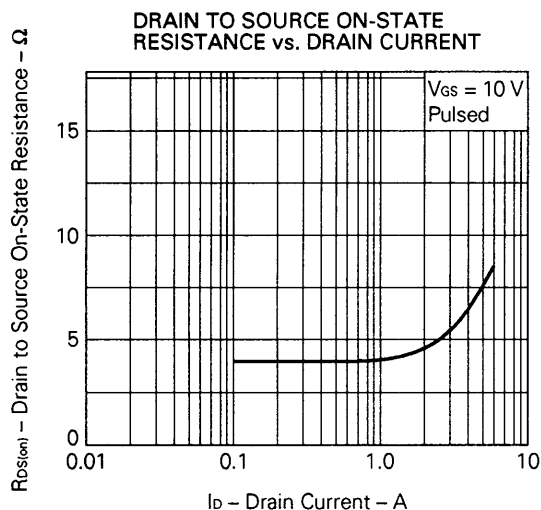
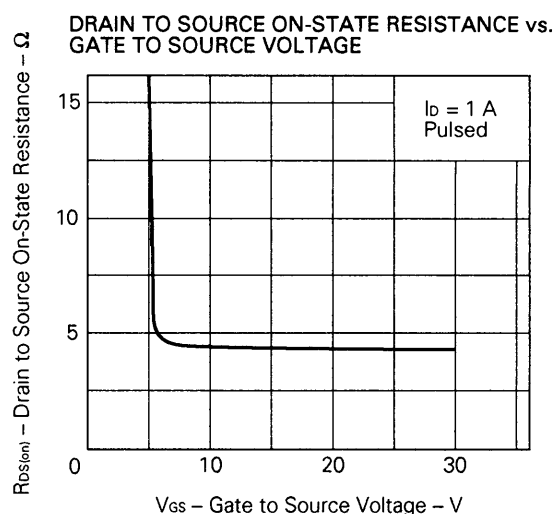
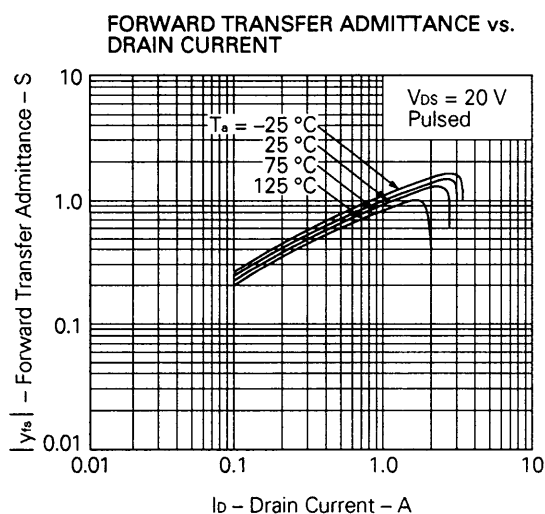
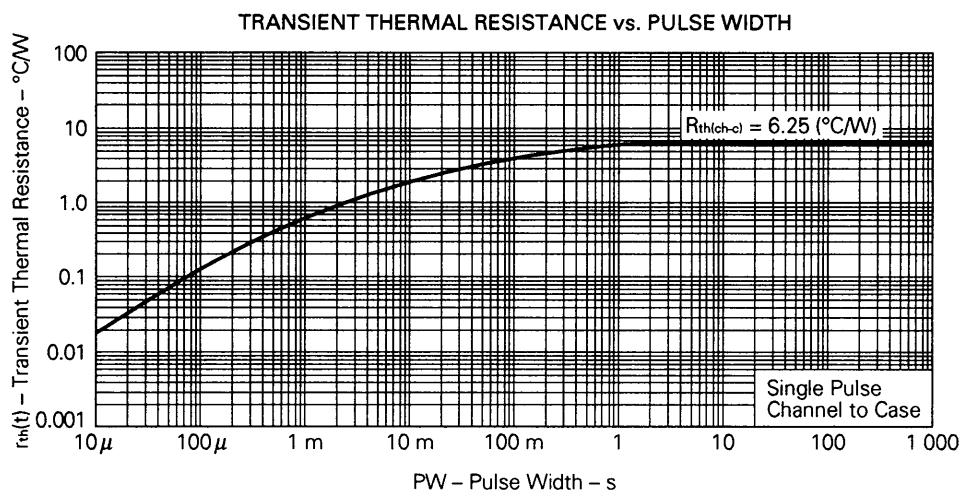


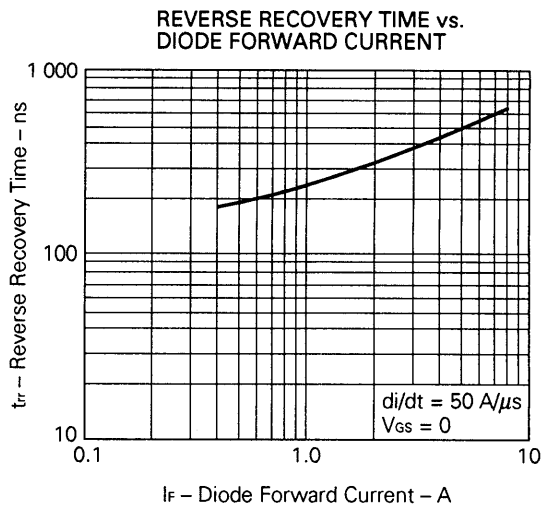
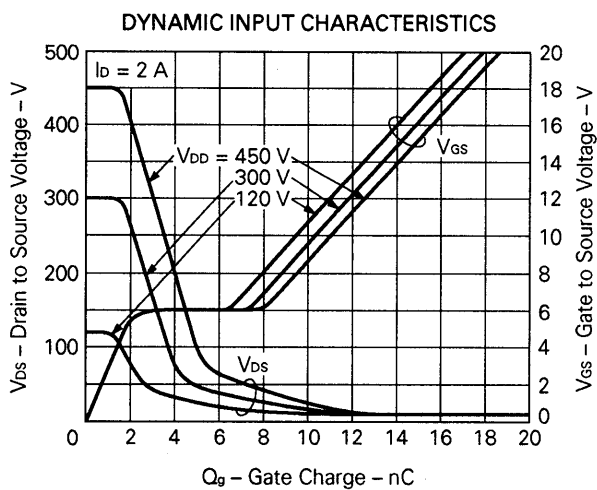
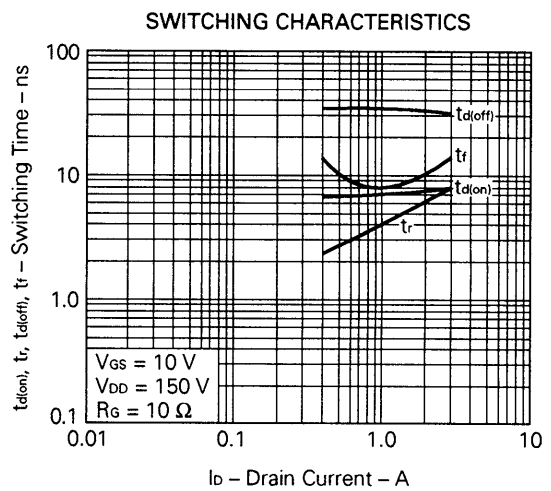
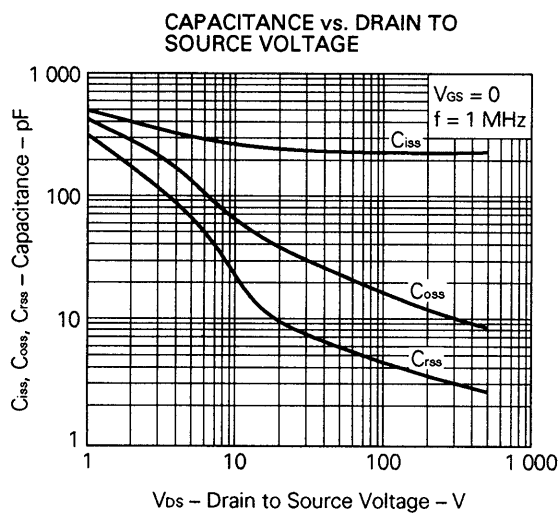
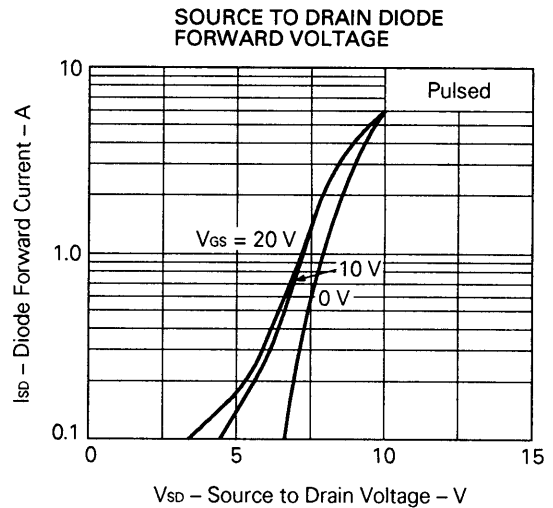
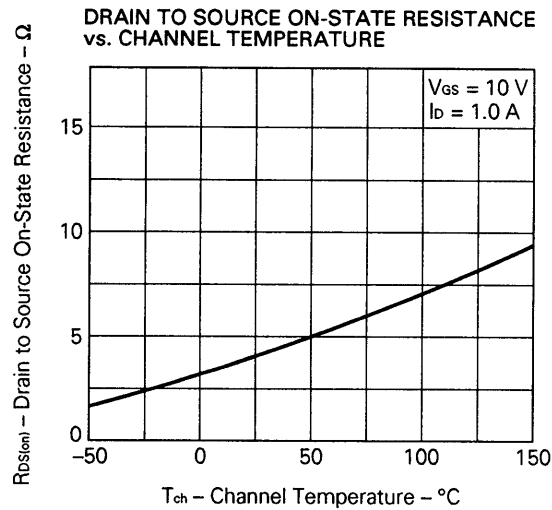
Test Circuit 3: Gate Charge

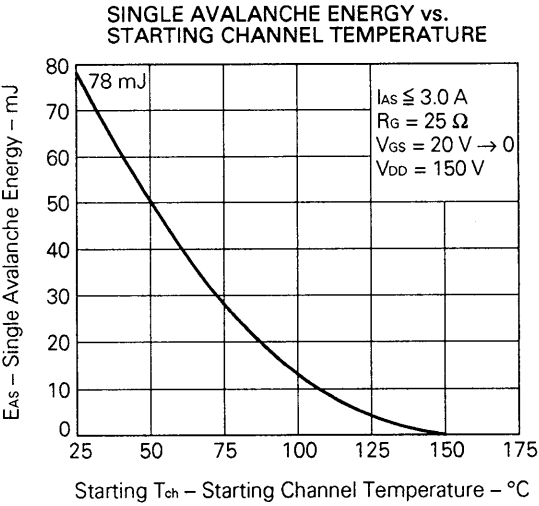
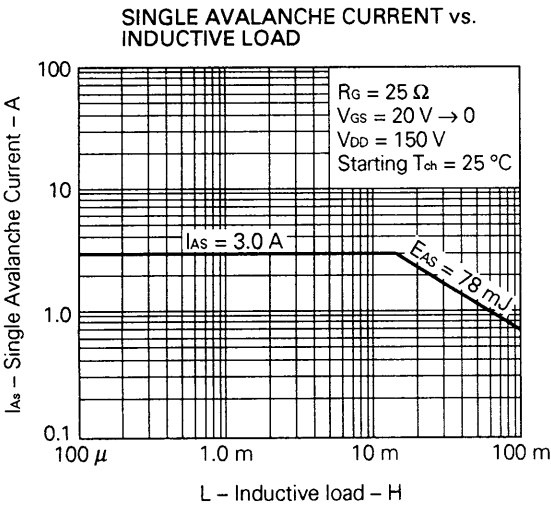


TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)









Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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