

MOS FIELD EFFECT TRANSISTOR  
**2SK2410**

SWITCHING  
 N-CHANNEL POWER MOS FET  
 INDUSTRIAL USE

**DESCRIPTION**

The 2SK2410 is N-Channel MOS Field Effect Transistor designed for high speed switching applications.

**FEATURES**

- Low On-Resistance  
 $R_{DS(on)1} = 40 \text{ m}\Omega \text{ MAX. (@ } V_{GS} = 10 \text{ V, } I_D = 15 \text{ A)}$   
 $R_{DS(on)2} = 60 \text{ m}\Omega \text{ MAX. (@ } V_{GS} = 4 \text{ V, } I_D = 15 \text{ A)}$
- Low  $C_{iss}$   $C_{iss} = 1500 \text{ pF TYP.}$
- High Avalanche Capability Ratings
- Built-in G-S Gate Protection Diodes

**QUALITY GRADE**

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

**ABSOLUTE MAXIMUM RATINGS (TA = 25 °C)**

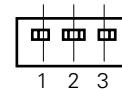
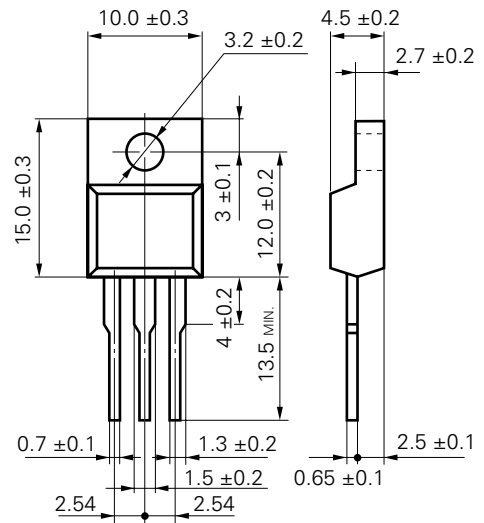
|   |                |             |                  |
|---|----------------|-------------|------------------|
| Drain to Source Voltage                                       | $V_{DSS}$      | 60          | V                |
| Gate to Source Voltage  | $V_{GSS}$      | $\pm 20$    | V                |
| Drain Current (DC)  | $I_{D(DC)}$    | $\pm 30$    | A                |
| Drain Current (pulse)*  | $I_{D(pulse)}$ | $\pm 120$   | A                |
| Total Power Dissipation ( $T_c = 25 \text{ }^\circ\text{C}$ ) | $P_{T1}$       | 35          | W                |
| Total Power Dissipation ( $T_A = 25 \text{ }^\circ\text{C}$ ) | $P_{T2}$       | 2.0         | W                |
| Channel Temperature   | $T_{ch}$       | 150         | $^\circ\text{C}$ |
| Storage Temperature   | $T_{stg}$      | -55 to +150 | $^\circ\text{C}$ |
| Single Avalanche Current**                                    | $I_{AS}$       | 30          | A                |
| Single Avalanche Energy**                                     | $E_{AS}$       | 90          | mJ               |

\*  $PW \leq 10 \text{ } \mu\text{s}$ , Duty Cycle  $\leq 1 \%$

\*\* Starting  $T_{ch} = 25 \text{ }^\circ\text{C}$ ,  $R_G = 25 \text{ } \Omega$ ,  $V_{GS} = 20 \text{ V} \rightarrow 0$

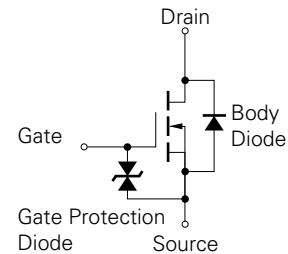
**PACKAGE DIMENSIONS**

(in millimeters)



1. Gate
2. Drain
3. Source

**MP-45F (ISOLATED TO-220)**

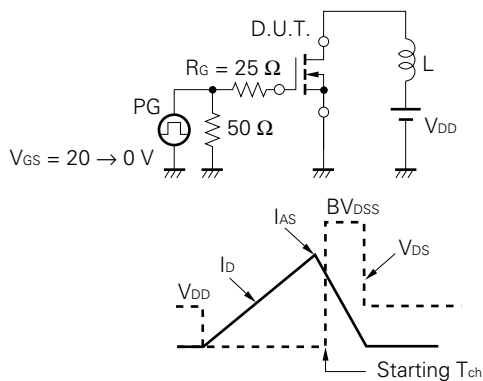


The information in this document is subject to change without notice.

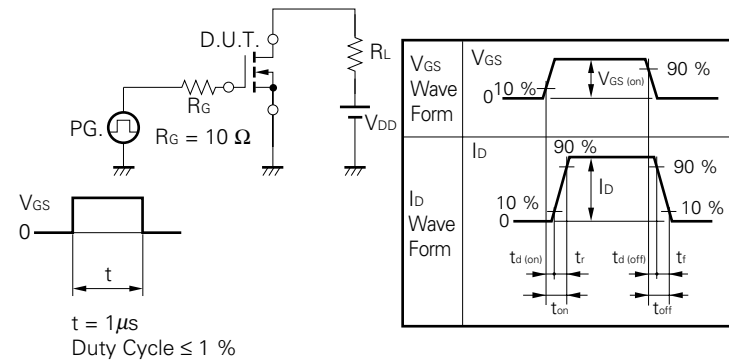
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)**

| CHARACTERISTIC                 | SYMBOL               | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS                               |
|--------------------------------|----------------------|------|------|------|------|---|
| Drain to Source On-Resistance  | R <sub>DS(on)1</sub> |      | 31   | 40   | mΩ   | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A |
| Drain to Source On-Resistance  | R <sub>DS(on)2</sub> |      | 40   | 60   | mΩ   | V <sub>GS</sub> = 4 V, I <sub>D</sub> = 15 A  |
| Gate to Source Cutoff Voltage  | V <sub>GS(off)</sub> | 1.0  | 1.5  | 2.0  | V    | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA |
| Forward Transfer Admittance    | y <sub>fs</sub>      | 15   | 27   |      | S    | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 15 A |
| Drain Leakage Current          | I <sub>bss</sub>     |      |      | 10   | μA   | V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0   |
| Gate to Source Leakage Current | I <sub>gss</sub>     |      |      | ±10  | μA   | V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0  |
| Input Capacitance              | C <sub>iss</sub>     |      | 1500 |      | pF   | V <sub>DS</sub> = 10 V                        |
| Output Capacitance             | C <sub>oss</sub>     |      | 720  |      | pF   | V <sub>GS</sub> = 0                           |
| Reverse Transfer Capacitance   | C <sub>rss</sub>     |      | 190  |      | pF   | f = 1 MHz                                     |
| Turn-On Delay Time             | t <sub>d(on)</sub>   |      | 22   |      | ns   | I <sub>D</sub> = 15 A                         |
| Rise Time                      | t <sub>r</sub>       |      | 260  |      | ns   | V <sub>GS(on)</sub> = 10 V                    |
| Turn-Off Delay Time            | t <sub>d(off)</sub>  |      | 130  |      | ns   | V <sub>DD</sub> = 30 V                        |
| Fall Time                      | t <sub>f</sub>       |      | 150  |      | ns   | R <sub>G</sub> = 10 Ω                         |
| Total Gate Charge              | Q <sub>G</sub>       |      | 50   |      | nC   | I <sub>D</sub> = 30 A                         |
| Gate to Source Charge          | Q <sub>GS</sub>      |      | 5.0  |      | nC   | V <sub>DD</sub> = 48 V                        |
| Gate to Drain Charge           | Q <sub>GD</sub>      |      | 15   |      | nC   | V <sub>GS</sub> = 10 V                        |
| Body Diode Forward Voltage     | V <sub>F(S-D)</sub>  |      | 1.1  |      | V    | I <sub>F</sub> = 30 A, V <sub>GS</sub> = 0    |
| Reverse Recovery Time          | t <sub>rr</sub>      |      | 110  |      | ns   | I <sub>F</sub> = 30 A, V <sub>GS</sub> = 0    |
| Reverse Recovery Charge        | Q <sub>rr</sub>      |      | 320  |      | nC   | di/dt = 100 A/μs                              |

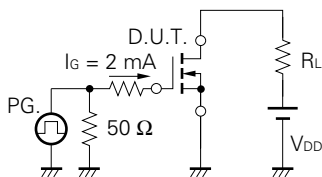
**Test Circuit 1 Avalanche Capability**



**Test Circuit 2 Switching Time**

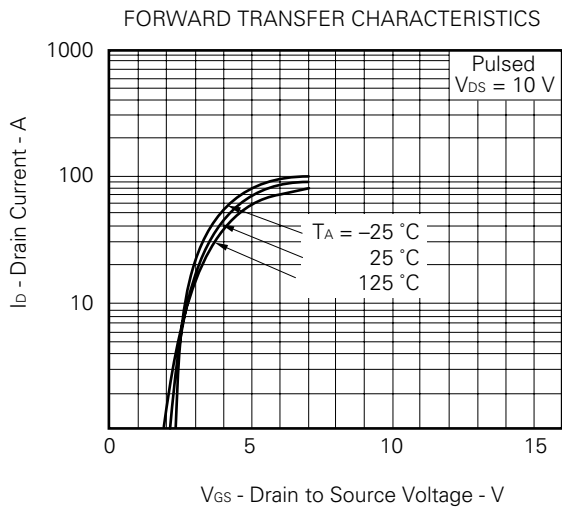
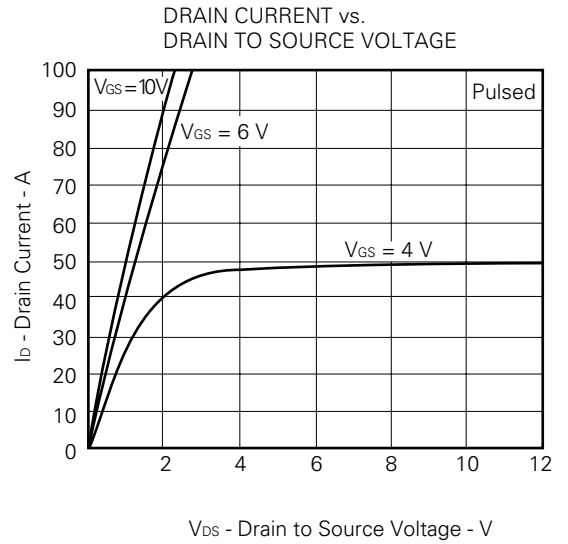
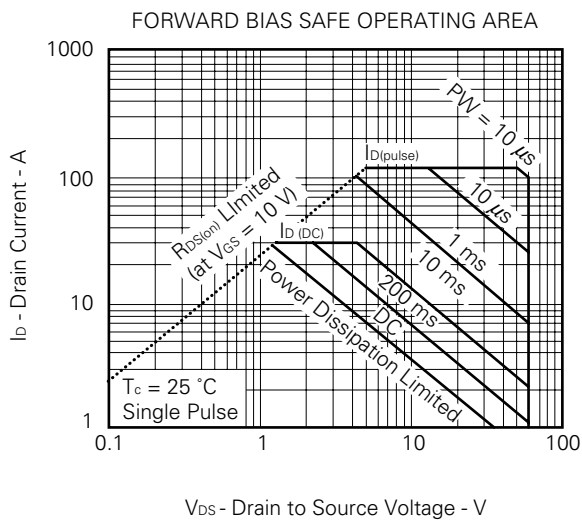
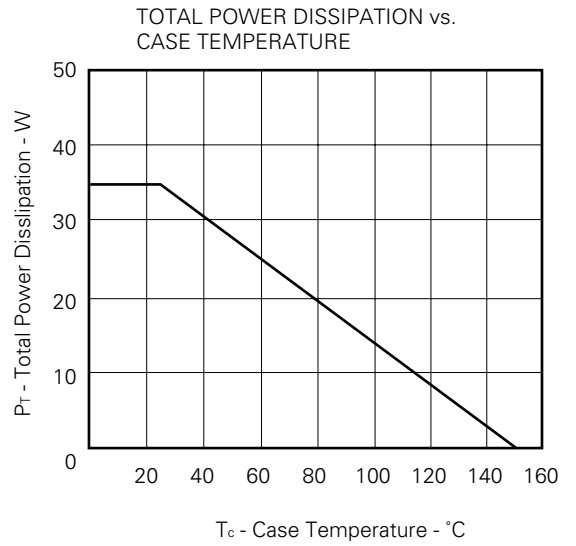
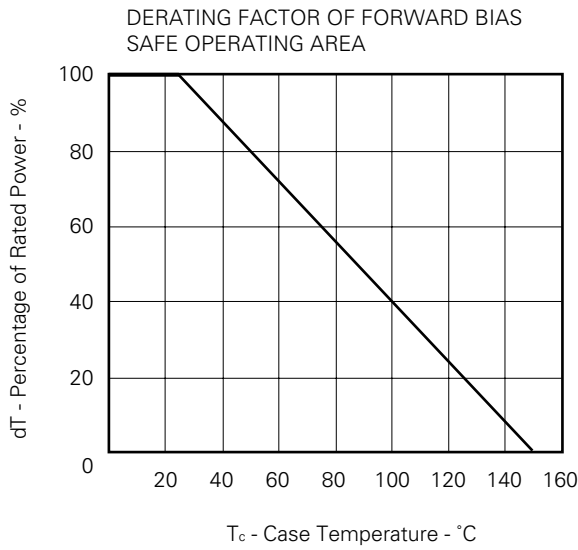


**Test Circuit 3 Gate Charge**

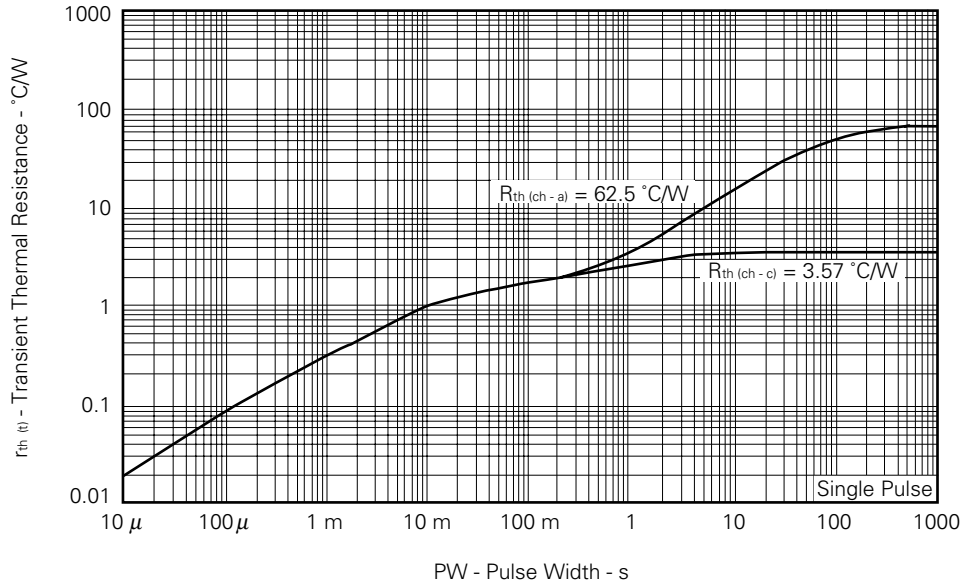


The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

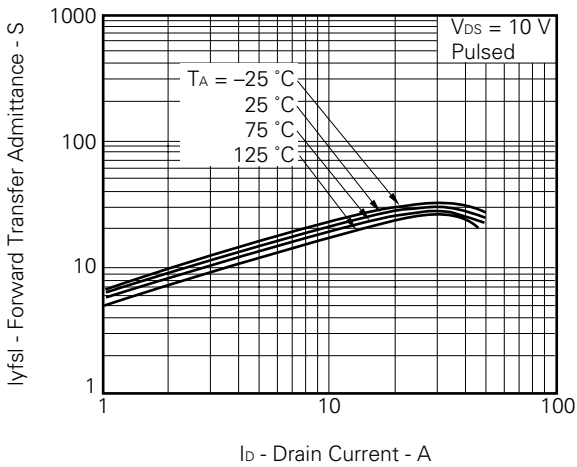
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)



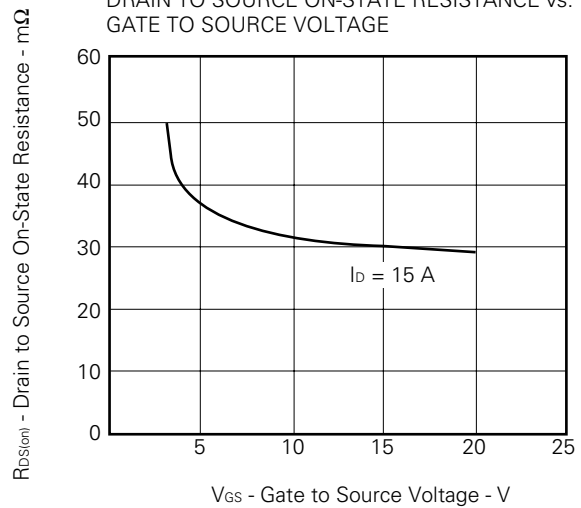
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



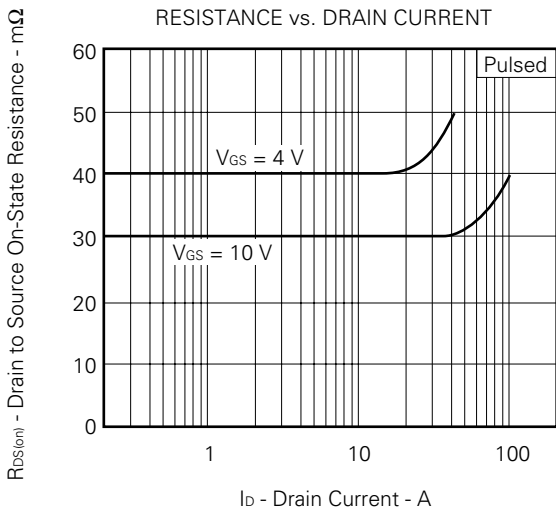
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



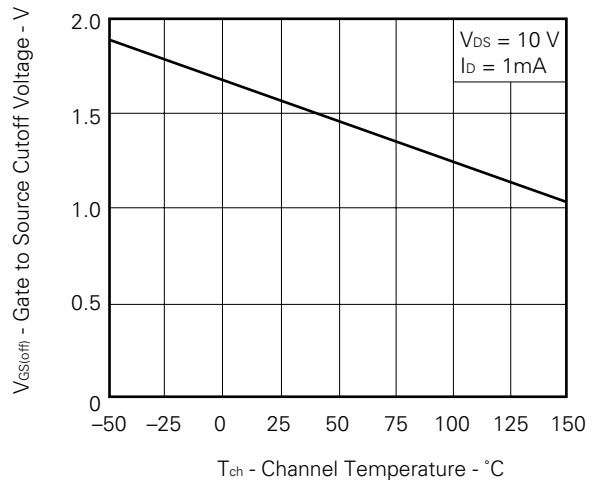
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

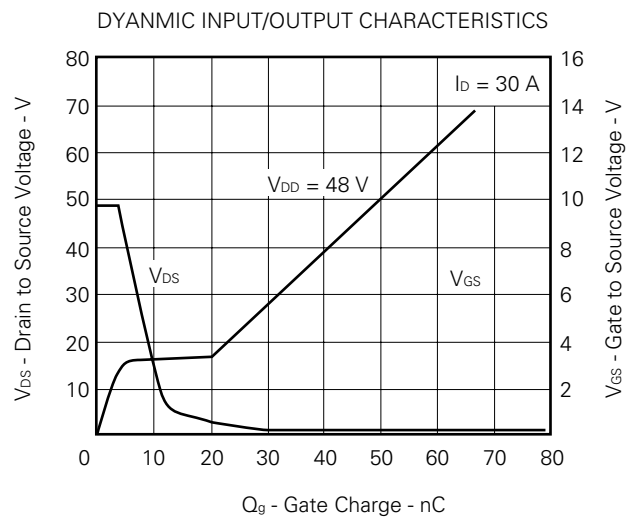
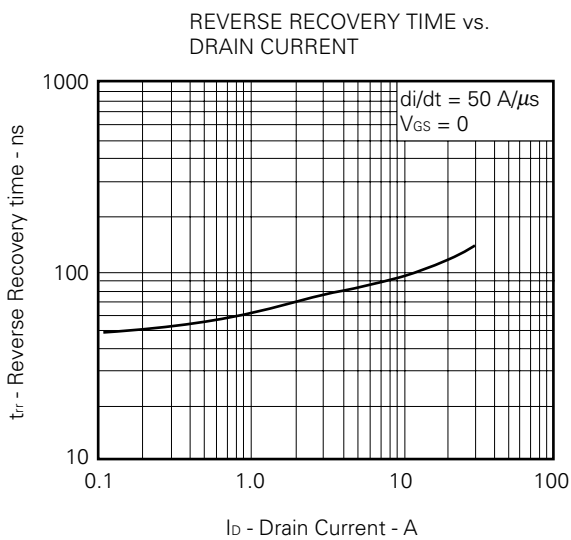
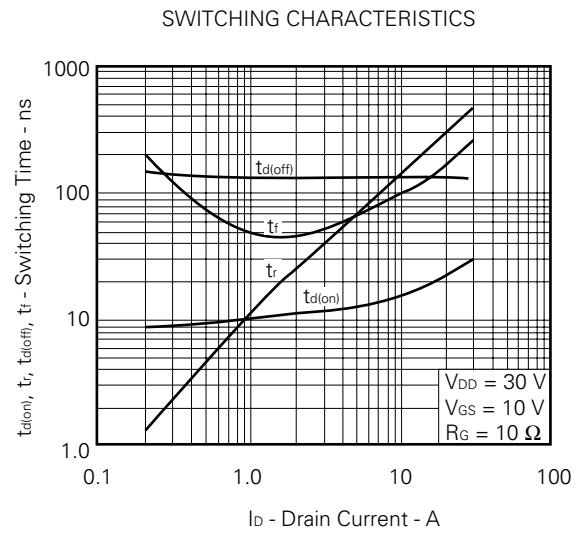
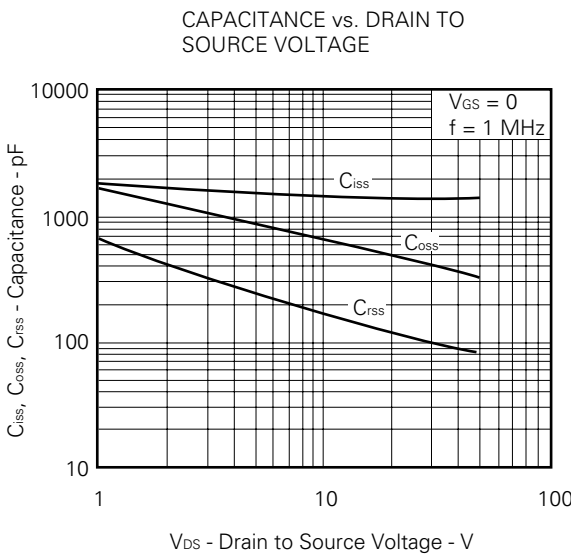
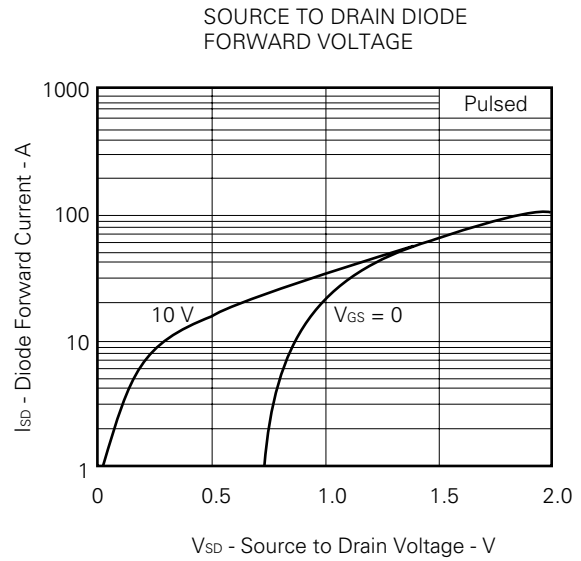
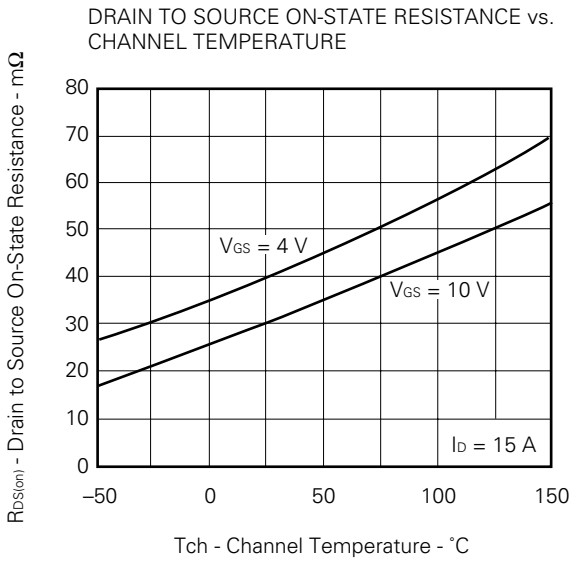


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

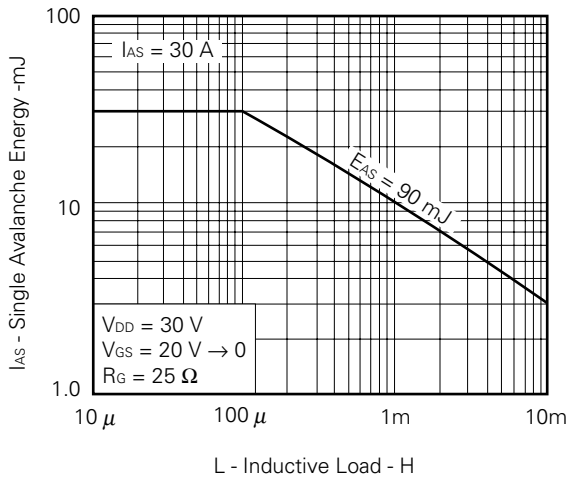


GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

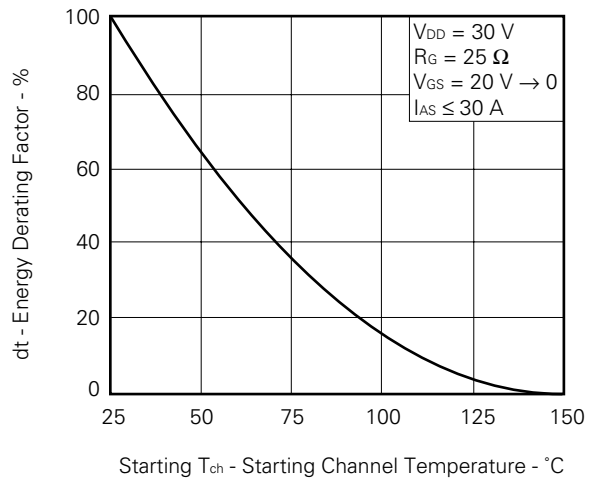




SINGLE AVALANCHE ENERGY vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY DERATING FACTOR



**REFERENCE**

| Document Name  | Document No. |
|--|--------------|
| NEC semiconductor device reliability/quality control system.   | TEI-1202     |
| Quality grade on NEC semiconductor devices.                    | IEI-1209     |
| Semiconductor device mounting technology manual.               | IEI-1207     |
| Semiconductor device package manual.                           | IEI-1213     |
| Guide to quality assurance for semiconductor devices.          | MEI-1202     |
| Semiconductor selection guide.                                 | MF-1134      |
| Power MOS FET features and application switching power supply. | TEA-1034     |
| Application circuits using Power MOS FET.                      | TEA-1035     |
| Safe operating area of Power MOS FET.                          | TEA-1037     |

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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