

MOS FIELD EFFECT TRANSISTOR
2SK2412SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK2412 is N-Channel MOS Field Effect Transistor designed for high speed switching applications.

FEATURES

- Low On-Resistance
 $R_{DS(on)1} = 70 \text{ m}\Omega \text{ MAX. (@ } V_{GS} = 10 \text{ V, } I_D = 10 \text{ A)}$
 $R_{DS(on)2} = 95 \text{ m}\Omega \text{ MAX. (@ } V_{GS} = 4 \text{ V, } I_D = 10 \text{ A)}$
- Low C_{iss} $C_{iss} = 860 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diodes
- High Avalanche Capability Ratings

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

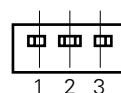
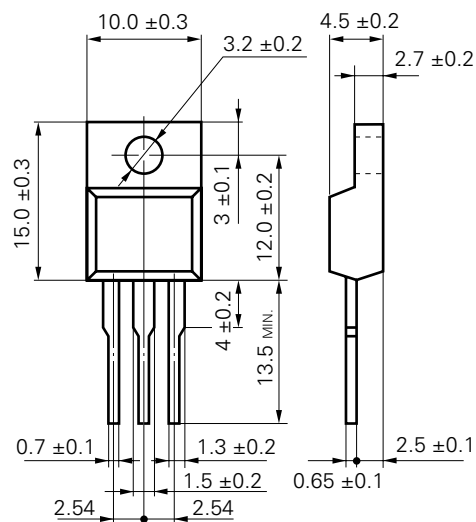
Drain to Source Voltage	V_{DSS}	60	V
Gate to Source Voltage	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 20	A
Drain Current (pulse)*	$I_{D(pulse)}$	± 80	A
Total Power Dissipation ($T_c = 25^\circ\text{C}$)	P_{T1}	30	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_{T2}	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-55 \text{ to } +150$	$^\circ\text{C}$
Single Avalanche Current**	I_{AS}	20	A
Single Avalanche Energy**	E_{AS}	22.5	mJ

* $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

** Starting $T_{ch} = 25^\circ\text{C}$, $R_G = 25 \Omega$, $V_{GS} = 20 \text{ V} \rightarrow 0$

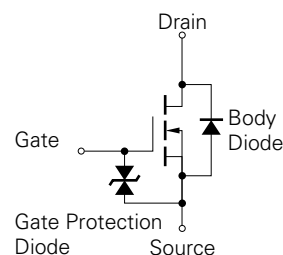
PACKAGE DIMENSIONS

(in millimeters)



1. Gate
2. Drain
3. Source

MP-45F (ISOLATED TO-220)

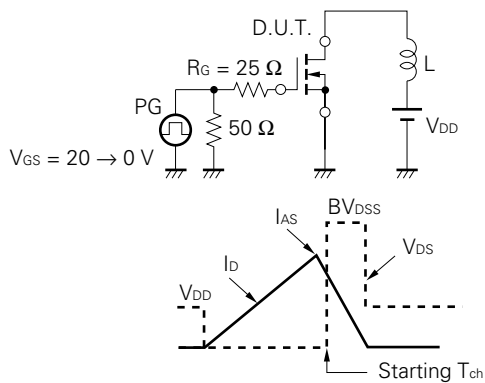


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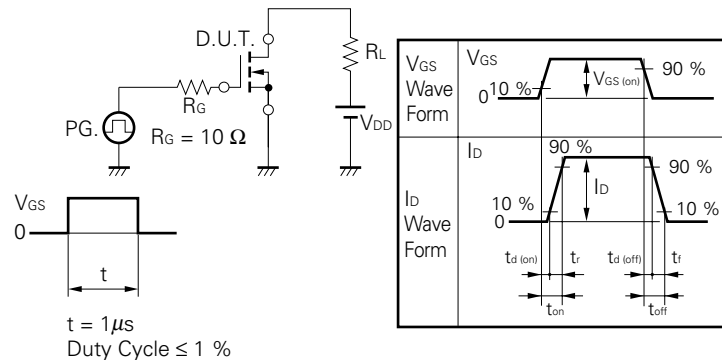
ELECTRICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-Resistance	$R_{DS(on)1}$		50	70	$\text{m}\Omega$	$V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$
Drain to Source On-Resistance	$R_{DS(on)2}$		67	95	$\text{m}\Omega$	$V_{GS} = 4\text{ V}$, $I_D = 10\text{ A}$
Gate to Source Cutoff Voltage	$V_{GS(off)}$	1.0	1.6	2.0	V	$V_{DS} = 10\text{ V}$, $I_D = 1\text{ mA}$
Forward Transfer Admittance	$ y_{fs} $	7.0	15		S	$V_{DS} = 10\text{ V}$, $I_D = 10\text{ A}$
Drain Leakage Current	I_{bss}			10	μA	$V_{DS} = 60\text{ V}$, $V_{GS} = 0$
Gate to Source Leakage Current	I_{GSS}			± 10	μA	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0$
Input Capacitance	C_{iss}		860		pF	$V_{DS} = 10\text{ V}$
Output Capacitance	C_{oss}		440		pF	$V_{GS} = 0$
Reverse Transfer Capacitance	C_{rss}		110		pF	$f = 1\text{ MHz}$
Turn-On Delay Time	$t_{d(on)}$		15		ns	$I_D = 10\text{ A}$
Rise Time	t_r		120		ns	$V_{GS(on)} = 10\text{ V}$
Turn-Off Delay Time	$t_{d(off)}$		70		ns	$V_{DD} = 30\text{ V}$
Fall Time	t_f		50		ns	$R_G = 10\text{ }\Omega$
Total Gate Charge	Q_G		27		nC	$I_D = 20\text{ A}$
Gate to Source Charge	Q_{GS}		2.7		nC	$V_{DD} = 48\text{ V}$
Gate to Drain Charge	Q_{GD}		8.9		nC	$V_{GS} = 10\text{ V}$
Body Diode Forward Voltage	$V_{F(S-D)}$		1.2		V	$I_F = 20\text{ A}$, $V_{GS} = 0$
Reverse Recovery Time	t_{rr}		120		ns	$I_F = 20\text{ A}$, $V_{GS} = 0$
Reverse Recovery Charge	Q_{rr}		350		nC	$di/dt = 100\text{ A}/\mu\text{s}$

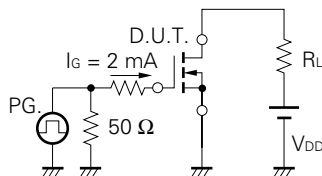
Test Circuit 1 Avalanche Capability



Test Circuit 2 Switching Time

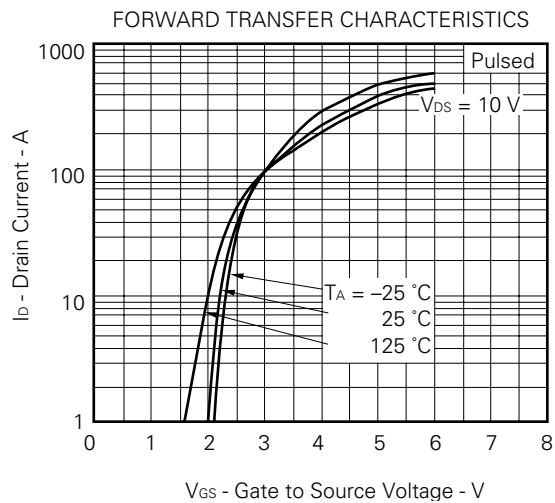
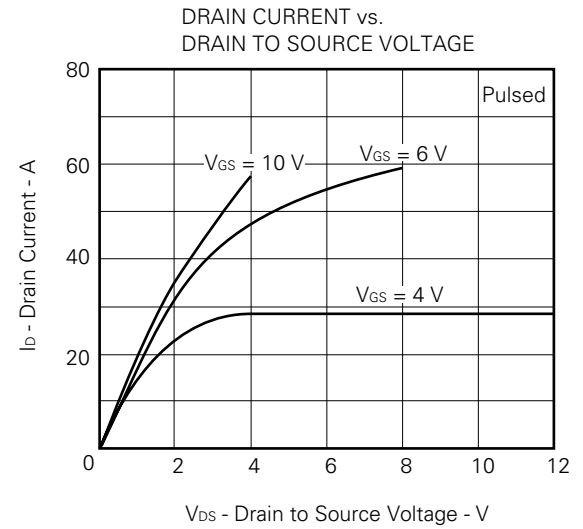
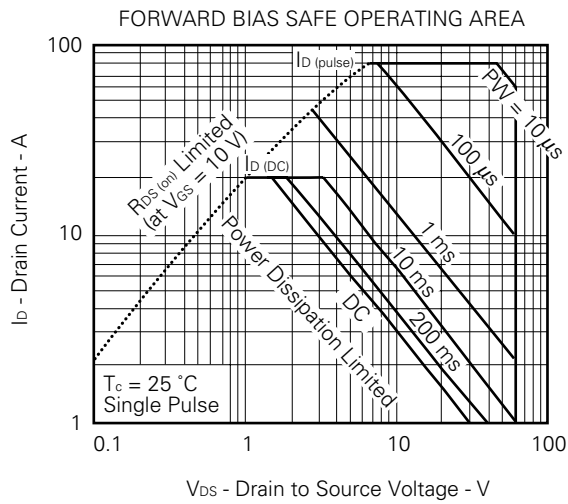
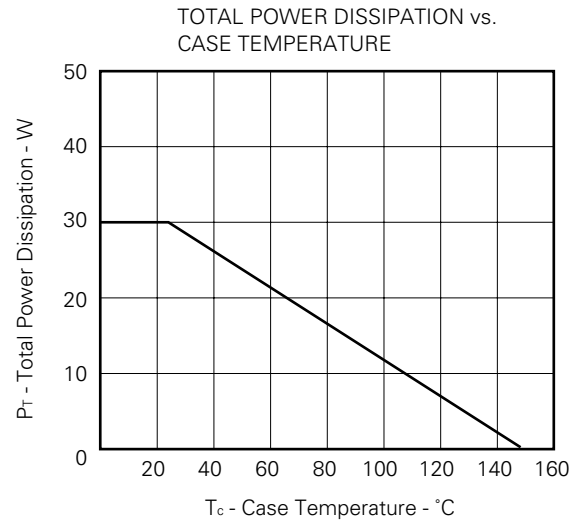
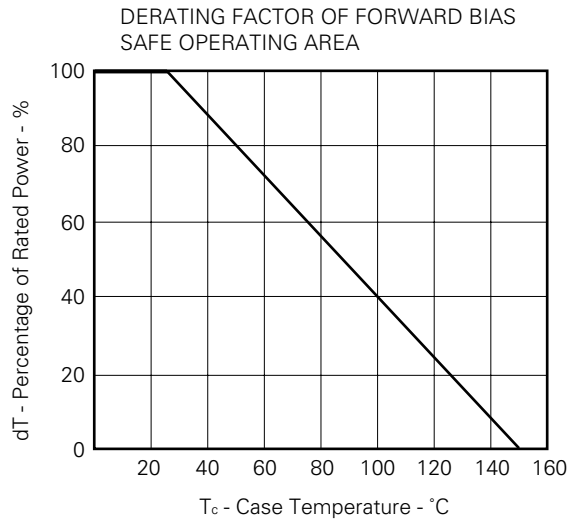


Test Circuit 3 Gate Charge

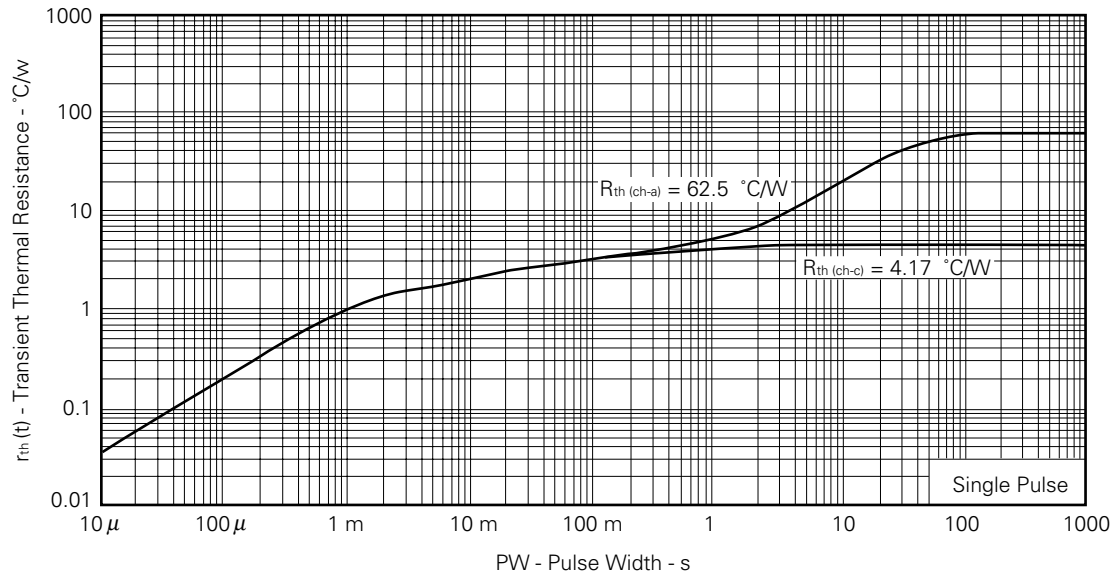


The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

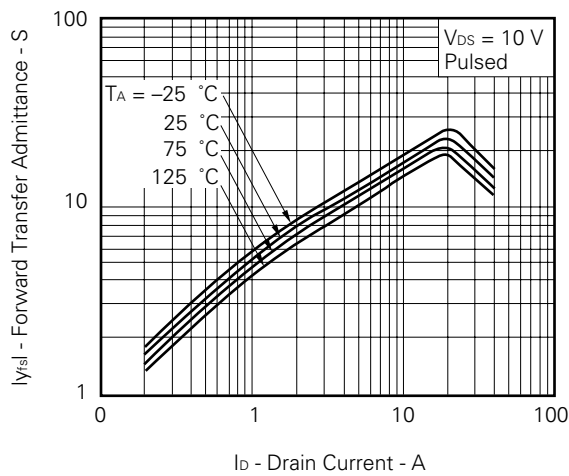
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$)



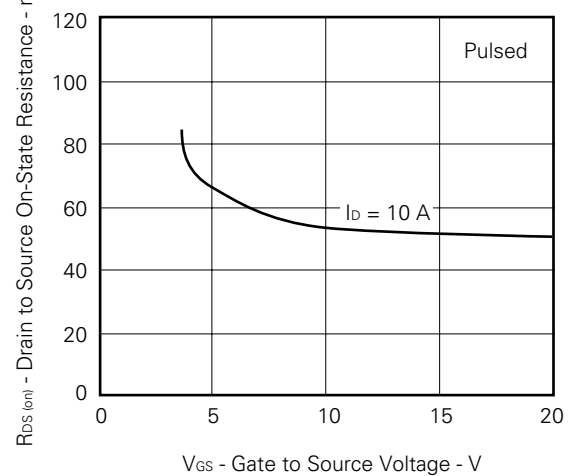
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



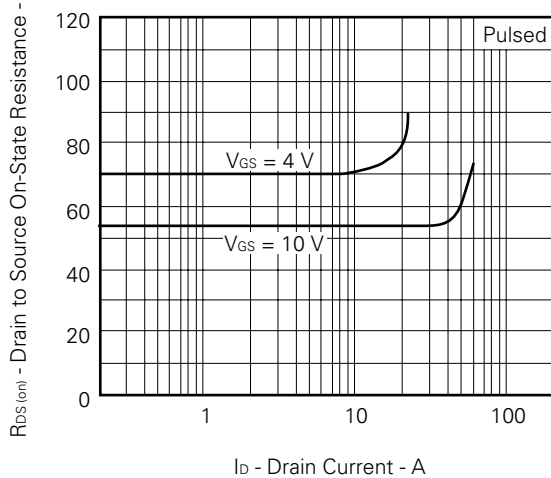
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



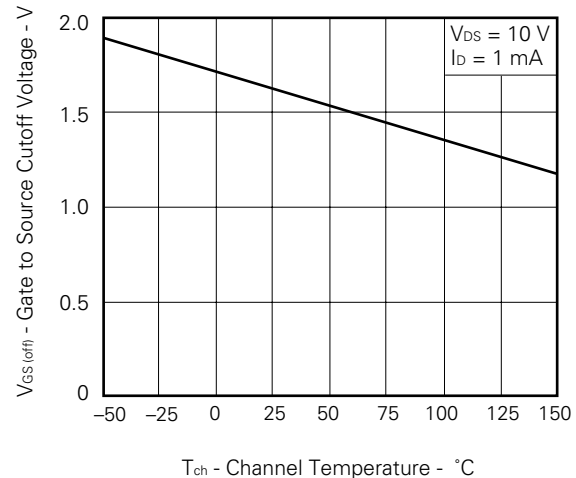
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

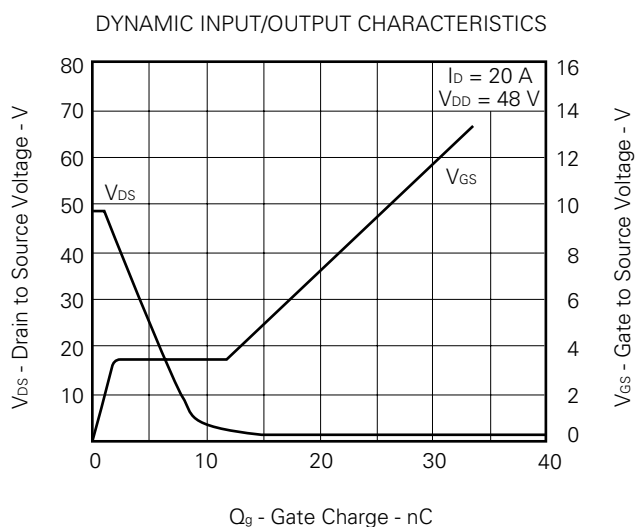
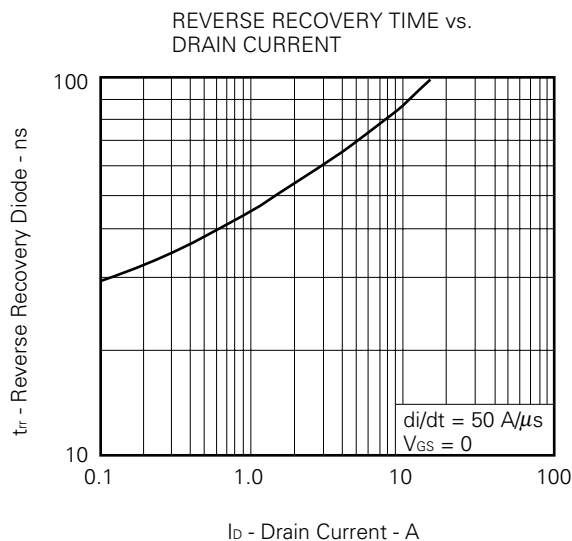
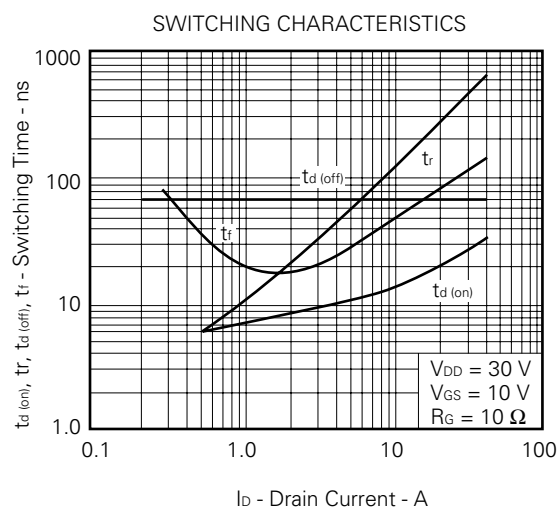
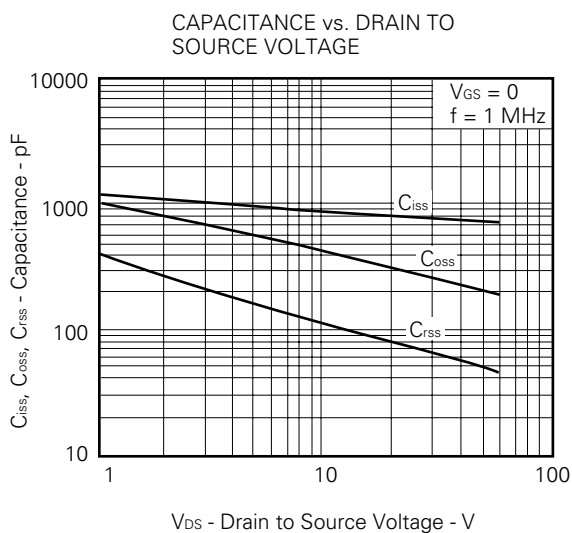
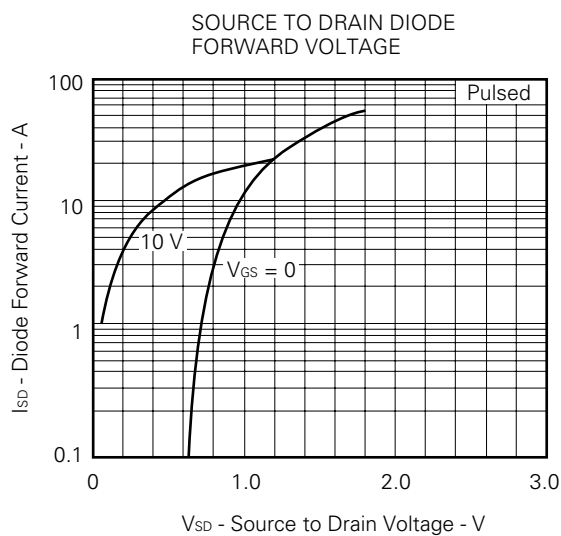
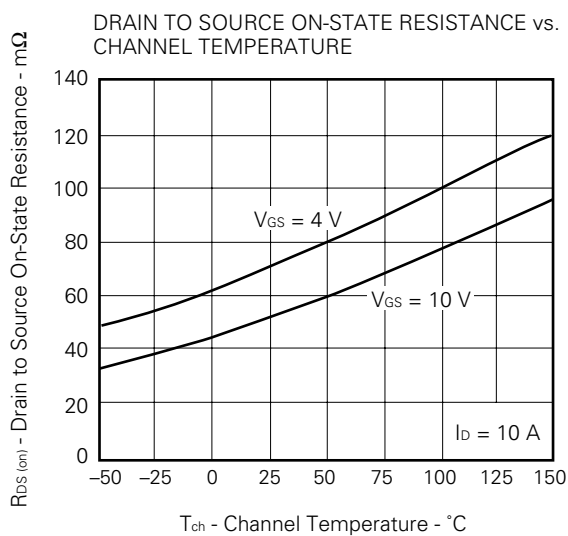


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

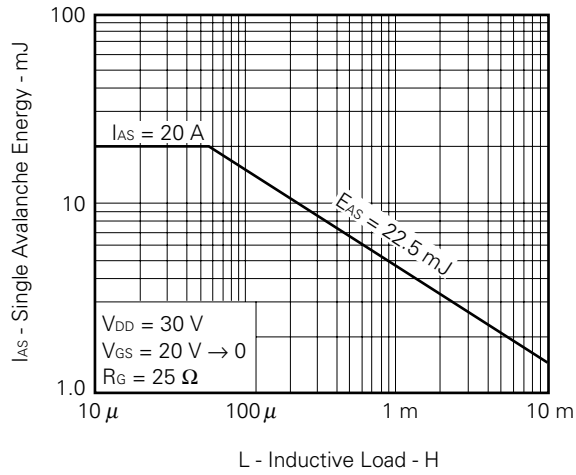


GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

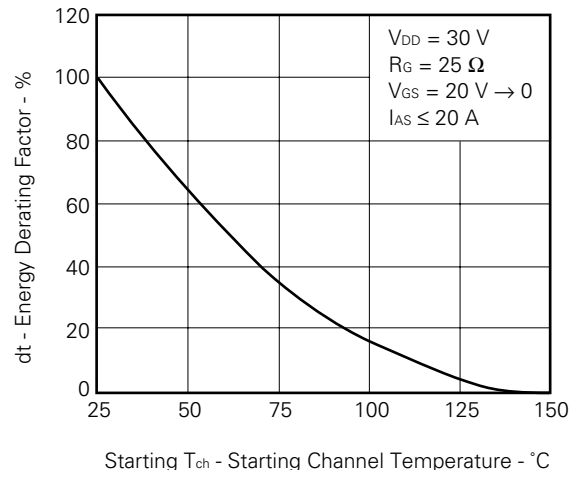




SINGLE AVALANCHE ENERGY vs.
INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY
DERATING FACTOR



REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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Special: Automotive and Transportation equipment, Traffic control systems, Antidisaster systems, Anticrime systems, etc.