

MOS FIELD EFFECT TRANSISTOR

2SK2483

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SK2483 is N-Channel MOS Field Effect Transistor designed for high voltage switching applications.

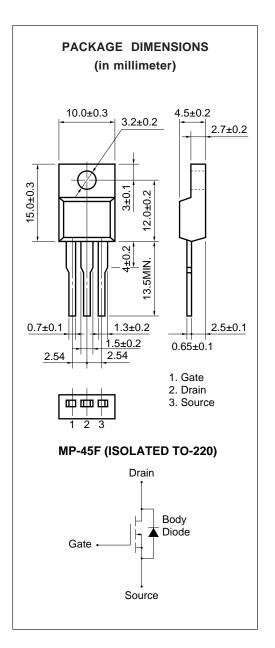
FEATURES

- Low On-Resistance
 - RDS (on) = 2.8Ω (VGS = 10 V, ID = 2.0 A)
- Low Ciss Ciss = 1 200 pF TYP.
- High Avalanche Capability Ratings
- Isolated TO-220 Package

ABSOLUTE MAXIMUM RATINGS $(T_A = 25 \degree C)$

Drain to Source Voltage	VDSS	900	V
Gate to Source Voltage	Vgss	±30	V
Drain Current (DC)	$I_{\text{D}(\text{DC})}$	±3.5	Α
Drain Current (pulse)*	ID(pulse	±10.5	Α
Total Power Dissipation (Tc = 25 °C)	P _{T1}	40	W
Total Power Dissipation (T _A = 25 °C)	P _{T2}	2.0	W
Channel Temperature	T_ch	150	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Single Avalanche Current**	las	3.5	Α
Single Avalanche Energy**	Eas	147	mJ

- * PW \leq 10 μ s, Duty Cycle \leq 1 %
- ** Starting Tch = 25 °C, R G = 25 Ω , VGS = 20 V \rightarrow 0

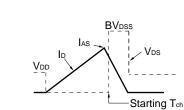




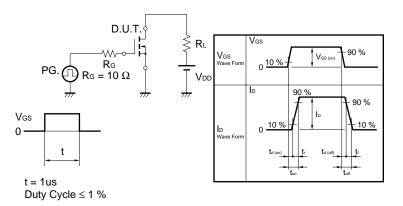
ELECTRICAL CHARACTERISTICS (TA = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-Resistance	RDS (on)			2.8	Ω	Vgs = 10 V, ID = 2.0 A
Gate to Source Cutoff Voltage	VGS (off)	2.5		3.5	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	yfs	1.0			S	V _{DS} = 20 V, I _D = 2.0 A
Drain Leakage Current	Ipss			100	μΑ	V _{DS} = V _{DSS} , V _{GS} = 0
Gate to Source Leakage Current	Igss			±100	nA	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0$
Input Capacitance	Ciss		1 200		pF	V _{DS} = 10 V
Output Capacitance	Coss		170		pF	V _G S = 0
Reverse Transfer Capacitance	Crss		30		pF	f = 1 MHz
Turn-On Delay Time	td (on)		20		ns	ID = 2.0 A
Rise Time	tr		10		ns	V _{GS} = 10 V
Turn-Off Delay Time	td (off)		70		ns	V _{DD} = 150 V
Fall Time	tf		15		ns	$R_G = 75 \Omega$
Total Gate Charge	Q _G		40		nC	ID = 3.5 A
Gate to Source Charge	Qgs		7		nC	V _{DD} = 450 V
Gate to Drain Charge	Q _{GD}		17		nC	V _{GS} = 10 V
Body Diode Forward Voltage	VF (S-D)		0.9		V	IF = 3.5 A, VGS = 0
Reverse Recovery Time	trr		580		ns	IF = 3.5 A, VGS = 0
Reverse Recovery Charge	Qrr		3.0		μC	$di/dt = 50 A/\mu s$

Test Circuit 1 Avalanche Capability



Test Circuit 2 Switching Time



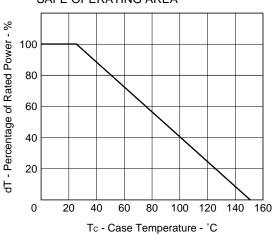
Test Circuit 3 Gate Charge

The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

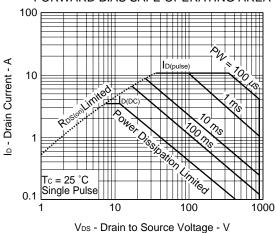
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TYPICAL CHARACTERISTICS (TA = 25 °C)

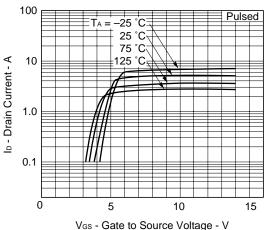




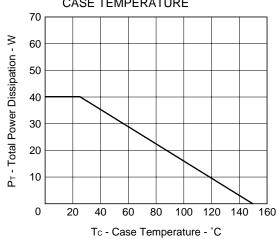
FORWARD BIAS SAFE OPERATING AREA



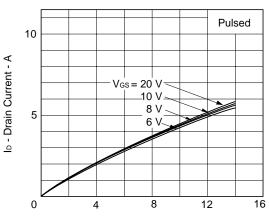
FORWARD TRANSFER CHARACTERISTICS



TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



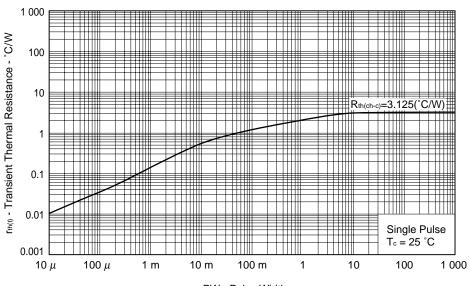
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



V_{DS} - Drain to Source Voltage - V

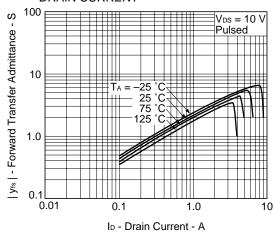


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



PW - Pulse Width - s

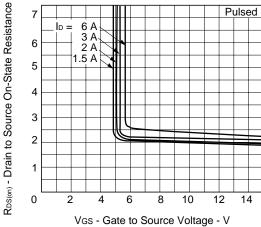
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



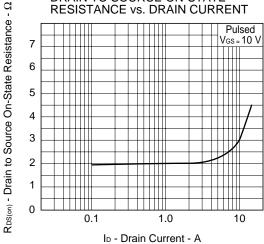
 $I_D =$

GATE TO SOURCE VOLTAGE

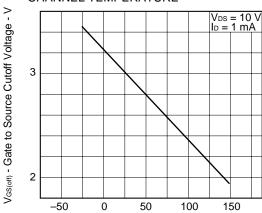
DRAIN TO SOURCE ON-STATE RESISTANCE vs.



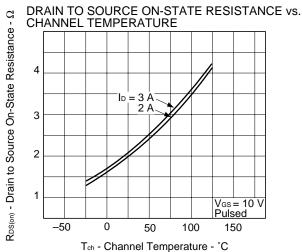
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

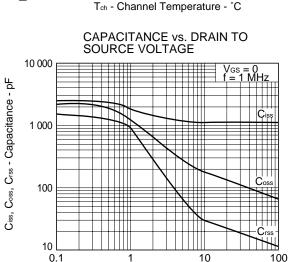


GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

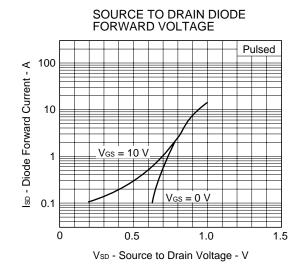


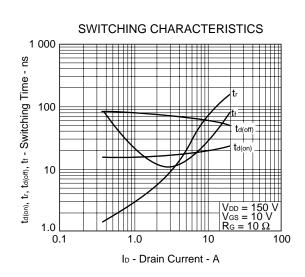
Tch - Channel Temperature - °C

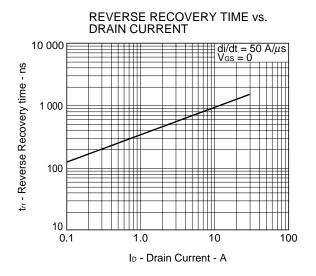


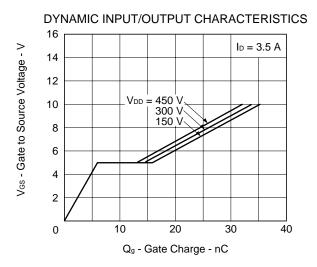


V_{DS} - Drain to Source Voltage - V



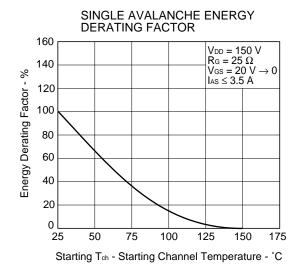








SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD 100 Value of the property of th





REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

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Anti-radioactive design is not implemented in this product.

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