

SWITCHING

N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3484 is N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Low on-state resistance
 $R_{DS(on)1} = 125 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 8 \text{ A)}$
 $R_{DS(on)2} = 148 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 8 \text{ A)}$
- Low C_{iss} : $C_{iss} = 900 \text{ pF TYP.}$
- Built-in gate protection diode
- TO-251/TO-252 package

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	100	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 16	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 22	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	30	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_{T2}	1.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Single Avalanche Current ^{Note2}	I_{AS}	10	A
Single Avalanche Energy ^{Note2}	E_{AS}	10	mJ

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 50 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

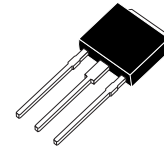
THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	4.17	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	125	$^\circ\text{C/W}$

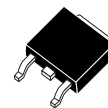
★ ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3484	TO-251 (MP-3)
2SK3484-Z	TO-252 (MP-3Z)

(TO-251)



(TO-252)



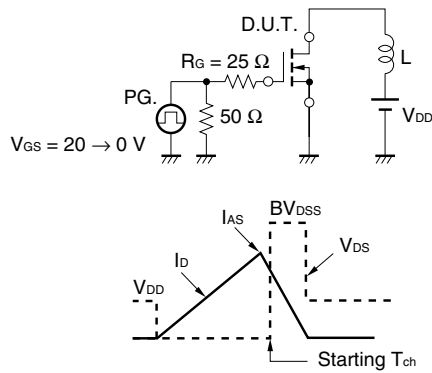
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ELECTRICAL CHARACTERISTICS (TA = 25°C)

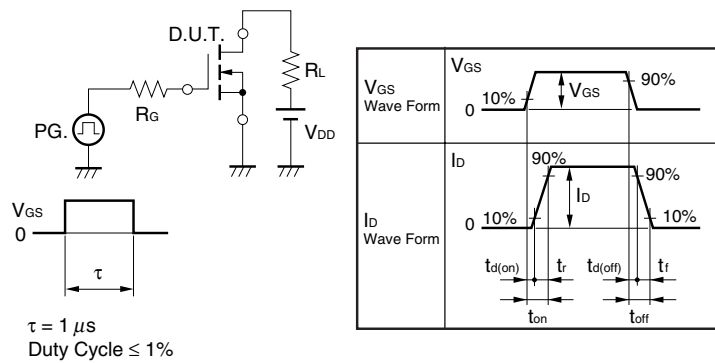
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$			10	μA
Gate Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			± 10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$	1.5	2.0	2.5	V
Forward Transfer Admittance ^{Note}	$ y_{fs} $	$V_{DS} = 10\text{ V}, I_D = 8\text{ A}$	4.7	9.5		S
Drain to Source On-state Resistance ^{Note}	$R_{DS(on)1}$	$V_{GS} = 10\text{ V}, I_D = 8\text{ A}$		100	125	$\text{m}\Omega$
	$R_{DS(on)2}$	$V_{GS} = 4.5\text{ V}, I_D = 8\text{ A}$		110	148	$\text{m}\Omega$
Input Capacitance	C_{iss}	$V_{DS} = 10\text{ V}$		900		pF
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$		110		pF
Reverse Transfer Capacitance	C_{rss}	$f = 1\text{ MHz}$		50		pF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 50\text{ V}, I_D = 8\text{ A}$		9.0		ns
Rise Time	t_r	$V_{GS} = 10\text{ V}$		5.0		ns
Turn-off Delay Time	$t_{d(off)}$	$R_G = 0\ \Omega$		30		ns
Fall Time	t_f			4.0		ns
Total Gate Charge	Q_G	$V_{DD} = 80\text{ V}$		20		nC
Gate to Source Charge	Q_{GS}	$V_{GS} = 10\text{ V}$		3.0		nC
Gate to Drain Charge	Q_{GD}	$I_D = 16\text{ A}$		5.0		nC
Body Diode Forward Voltage ^{Note}	$V_{F(S-D)}$	$I_F = 16\text{ A}, V_{GS} = 0\text{ V}$		1.0		V
Reverse Recovery Time	t_{rr}	$I_F = 16\text{ A}, V_{GS} = 0\text{ V}$		60		ns
Reverse Recovery Charge	Q_{rr}	$di/dt = 100\text{ A}/\mu\text{s}$		122		nC

Note Pulsed

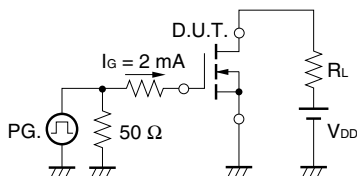
TEST CIRCUIT 1 AVALANCHE CAPABILITY



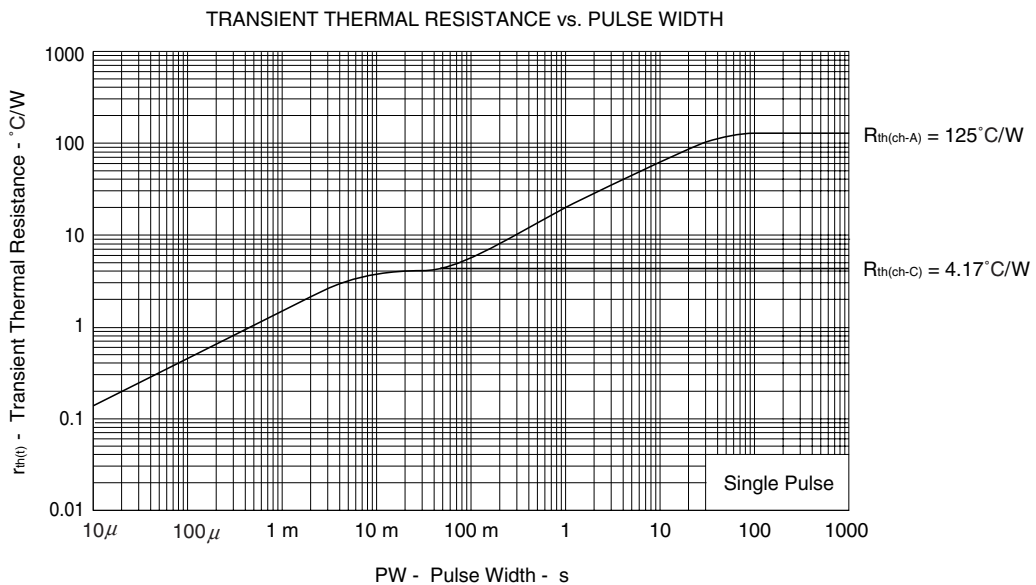
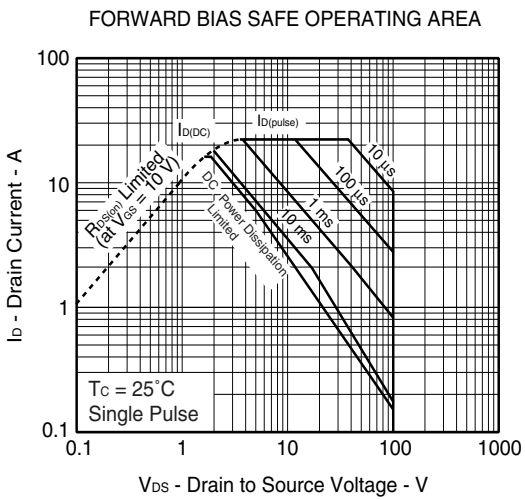
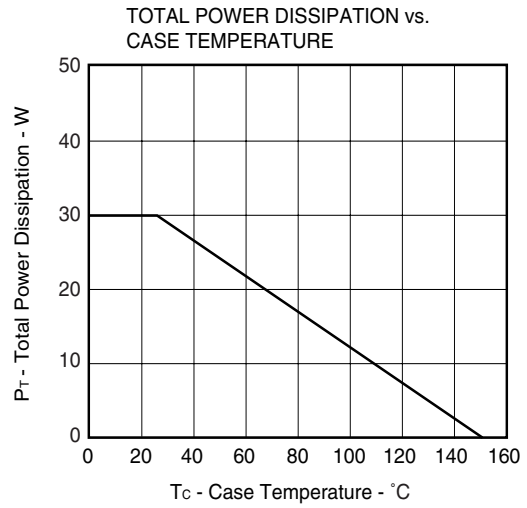
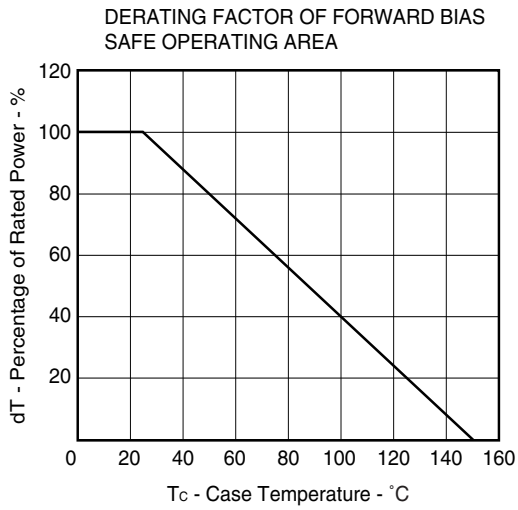
TEST CIRCUIT 2 SWITCHING TIME



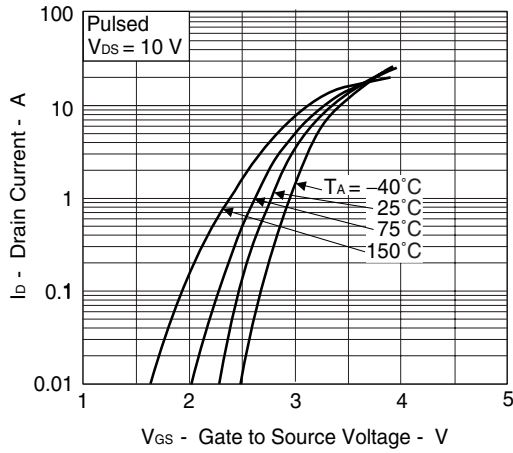
TEST CIRCUIT 3 GATE CHARGE



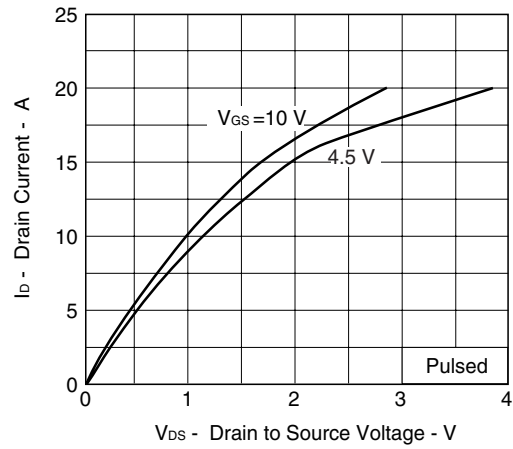
TYPICAL CHARACTERISTICS (T_A = 25°C)



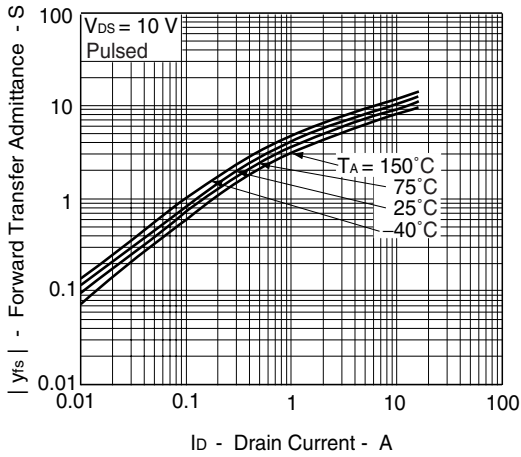
FORWARD TRANSFER CHARACTERISTICS



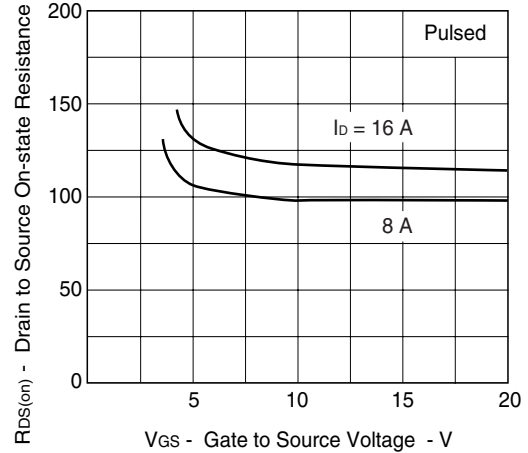
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



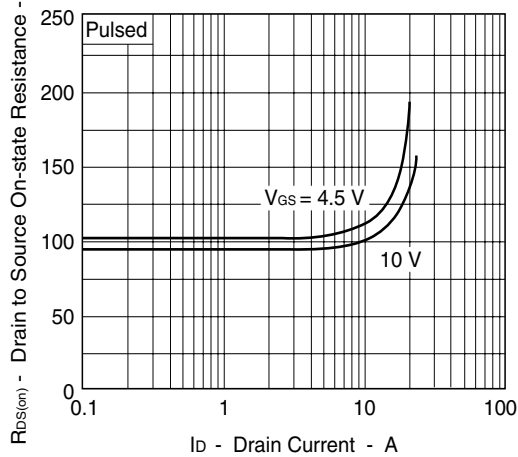
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



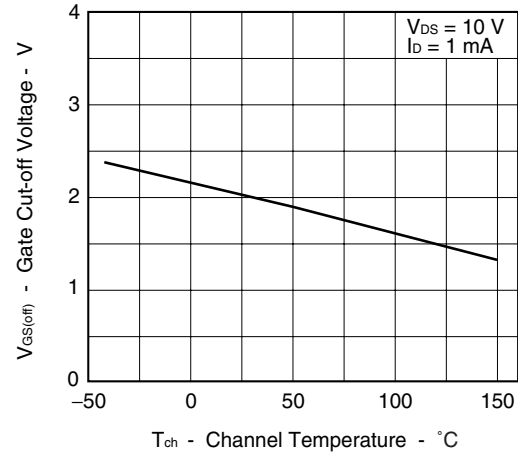
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

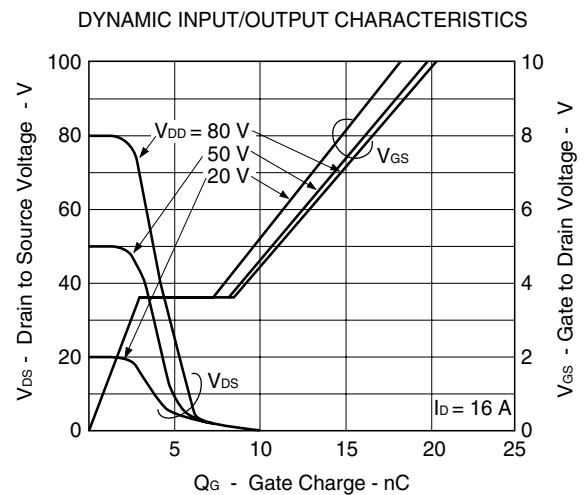
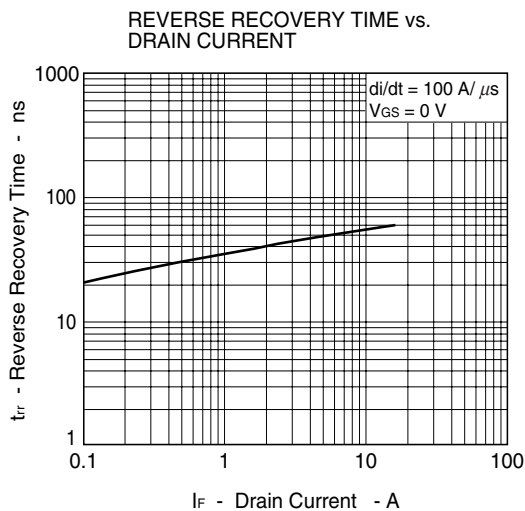
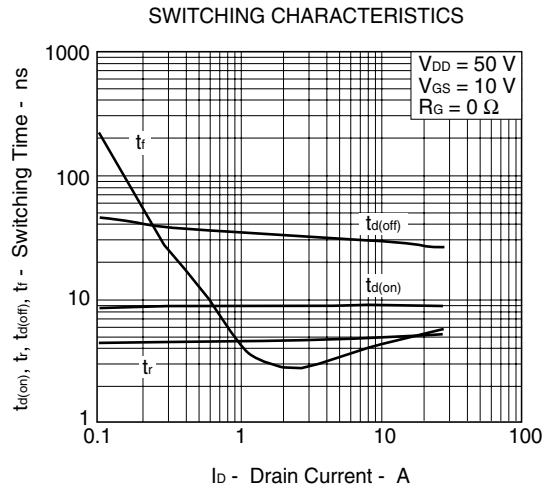
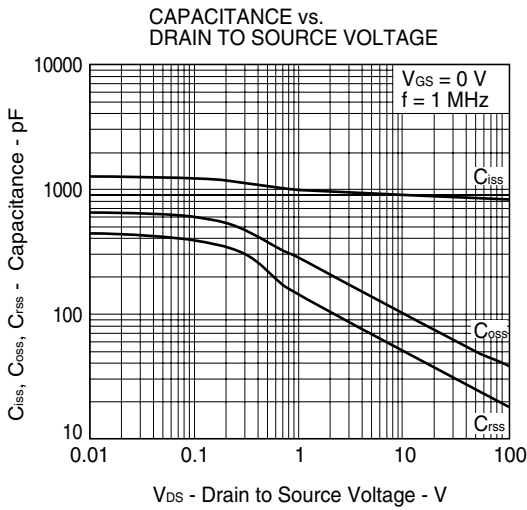
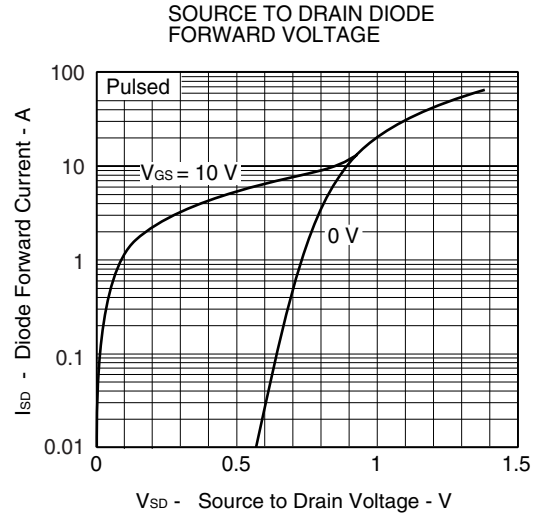
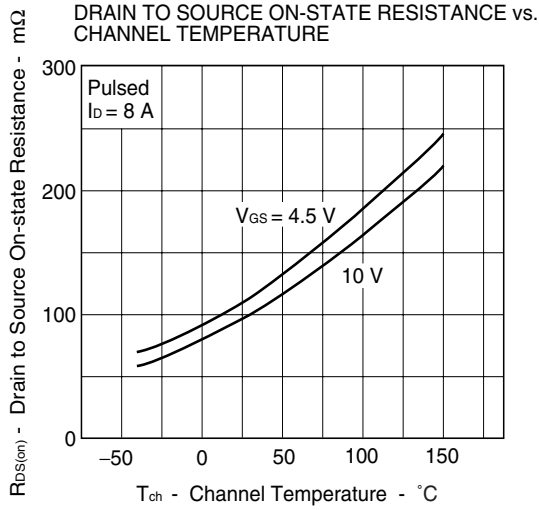


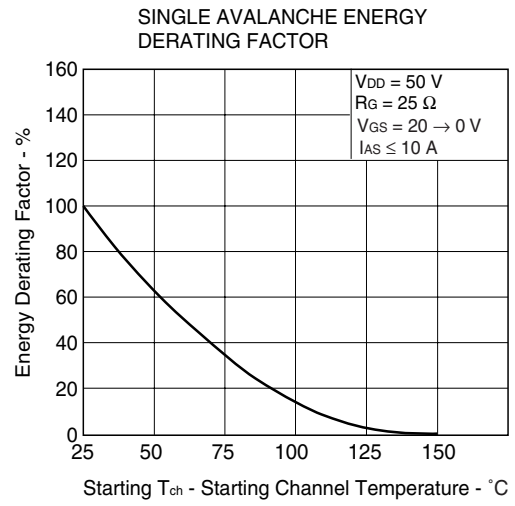
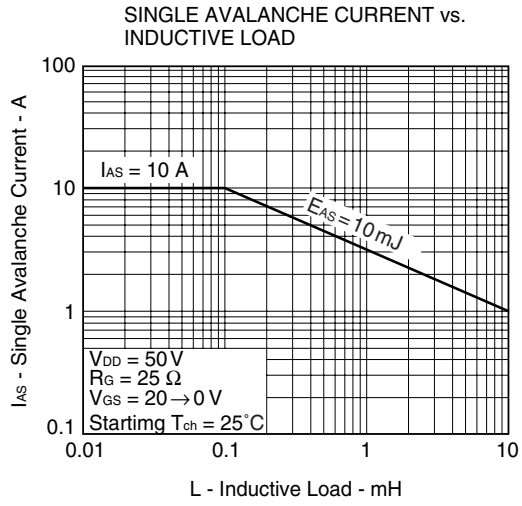
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE

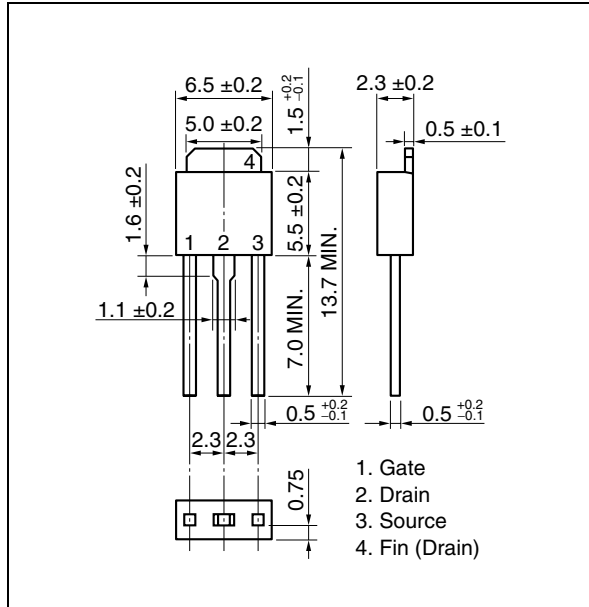




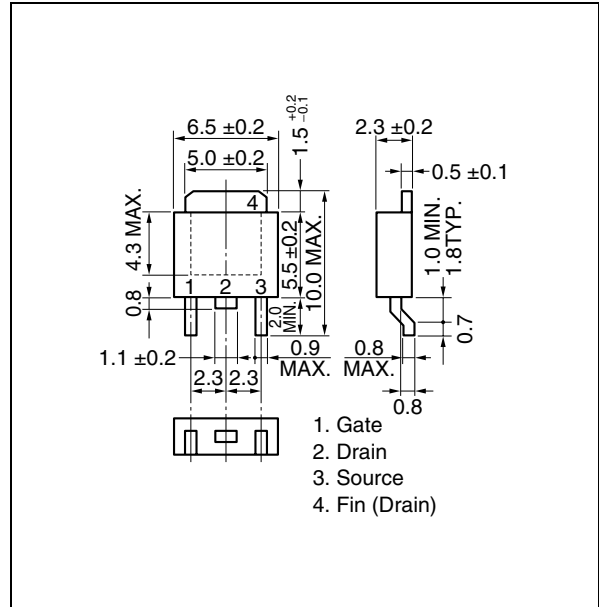


★ PACKAGE DRAWINGS (Unit: mm)

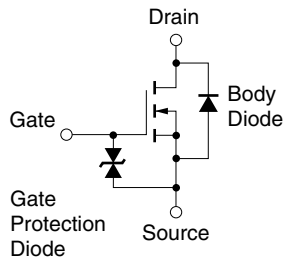
1) TO-251 (MP-3)



2) TO-252 (MP-3Z)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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