

SWITCHING
 N-CHANNEL POWER MOS FET
 INDUSTRIAL USE

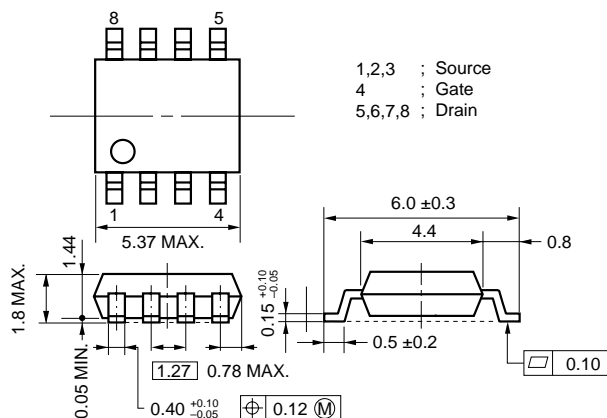
DESCRIPTION

This product is N-Channel MOS Field Effect Transistor designed for DC/DC converters and power management applications of notebook computers.

FEATURES

- Super Low on-resistance
 $R_{DS(on)1} = 5.8 \text{ m}\Omega$ (TYP.) ($V_{GS} = 10 \text{ V}$, $I_D = 7.0 \text{ A}$)
 $R_{DS(on)2} = 7.0 \text{ m}\Omega$ (TYP.) ($V_{GS} = 4.5 \text{ V}$, $I_D = 7.0 \text{ A}$)
 $R_{DS(on)3} = 8.0 \text{ m}\Omega$ (TYP.) ($V_{GS} = 4.0 \text{ V}$, $I_D = 7.0 \text{ A}$)
- Low C_{iss} : $C_{iss} = 3000 \text{ pF}$ (TYP.)
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit : mm)



ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1706G	Power SOP8

EQUIVALENT CIRCUIT

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, All terminals are connected)

Drain to Source Voltage ^{Note1}	V_{DSS}	30	V
Gate to Source Voltage ^{Note2}	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 13	A
Drain Current (pulse) ^{Note3}	$I_{D(pulse)}$	± 52	A
Total Power Dissipation ($T_A = 25^\circ\text{C}$) ^{Note4}	P_T	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to + 150	$^\circ\text{C}$

- Notes
1. $V_{GS} = 0 \text{ V}$
 2. $V_{DS} = 0 \text{ V}$
 3. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1 \%$
 4. Mounted on ceramic substrate of $1200 \text{ mm}^2 \times 0.7 \text{ mm}$



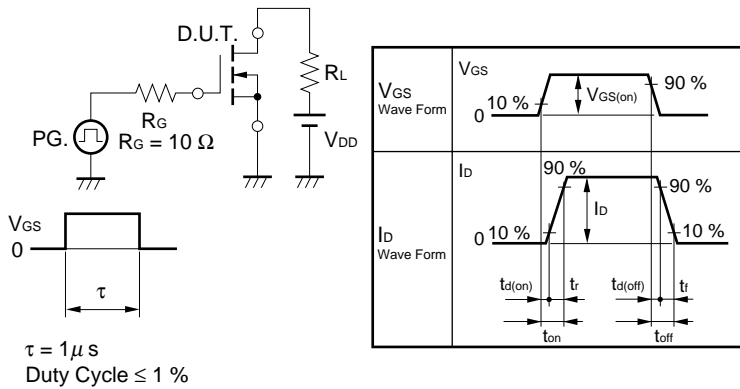
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

The information in this document is subject to change without notice.

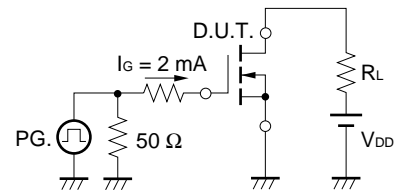
ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 7.0 A		5.8	7.8	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 7.0 A		7.0	10.0	mΩ
	R _{DS(on)3}	V _{GS} = 4.0 V, I _D = 7.0 A		8.0	12.0	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 7.0 A	10	22		S
Drain Leakage Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Input Capacitance	C _{iss}	V _{DS} = 10 V		3000		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		950		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		380		pF
Turn-on Delay Time	t _{d(on)}	I _D = 7.0 A		40		ns
Rise Time	t _r	V _{GS(on)} = 10 V		220		ns
Turn-off Delay Time	t _{d(off)}	V _{DD} = 15 V		140		ns
Fall Time	t _f	R _G = 10 Ω		90		ns
Total Gate Charge	Q _G	I _D = 13 A		56		nC
Gate to Source Charge	Q _{GS}	V _{DD} = 24 V		9		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = 10 V		14		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 13 A, V _{GS} = 0 V		0.8		V
Reverse Recovery Time	t _{rr}	I _F = 13 A, V _{GS} = 0 V		43		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		50		nC

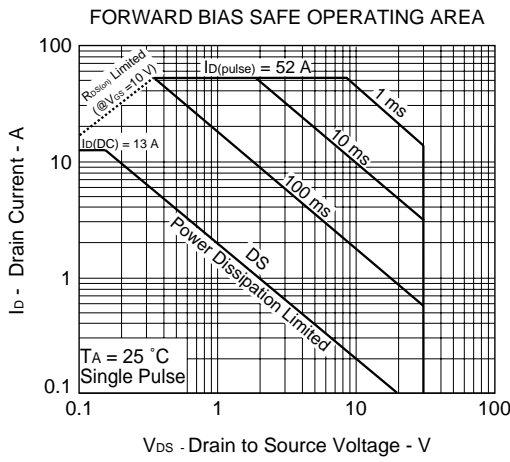
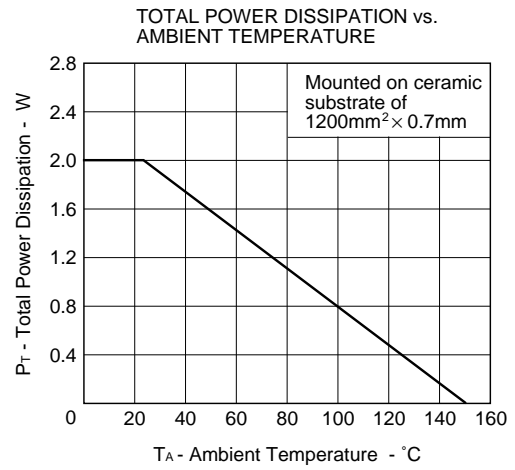
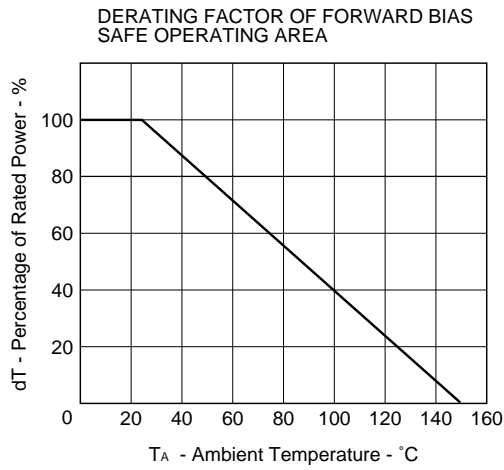
TEST CIRCUIT 1 SWITCHING TIME



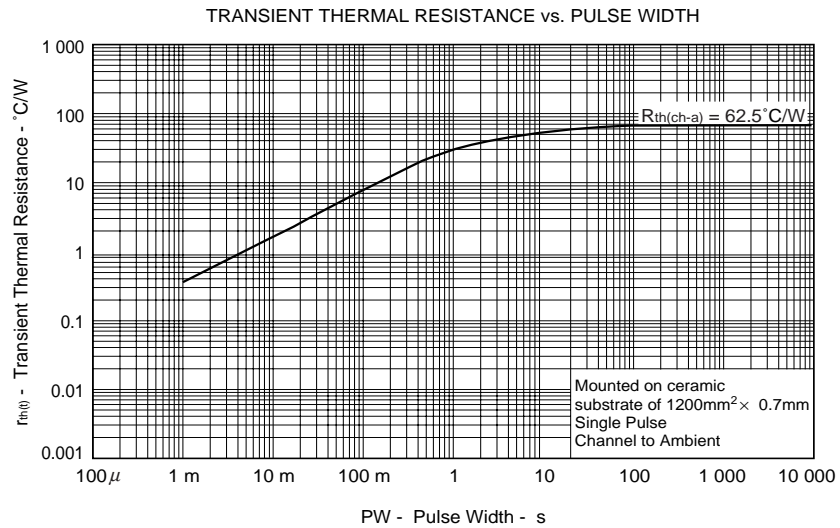
TEST CIRCUIT 2 GATE CHARGE

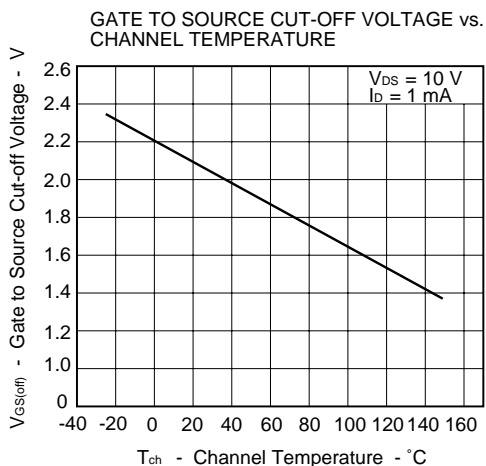
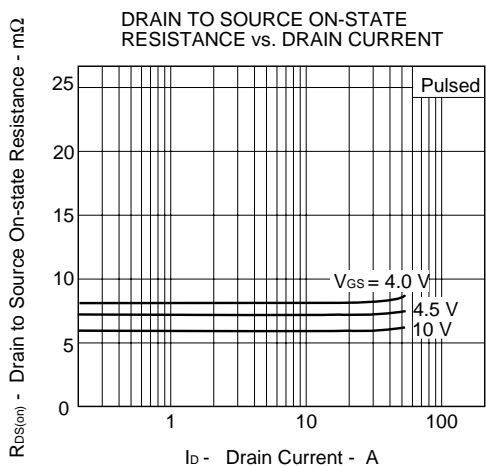
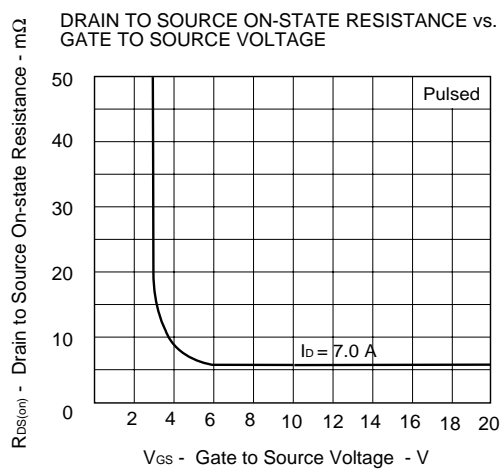
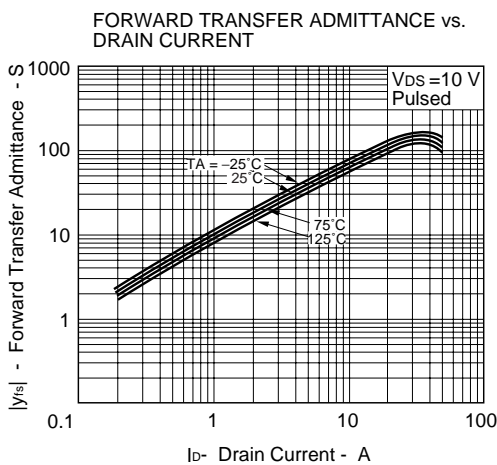
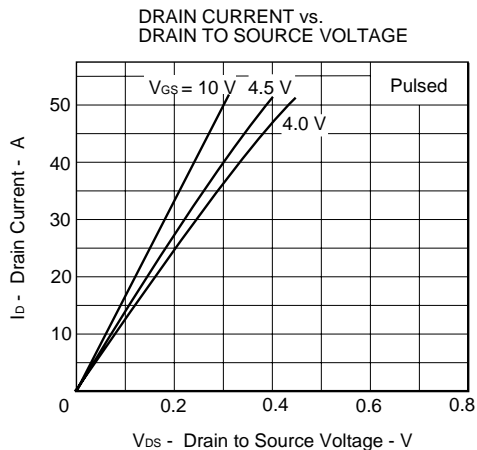
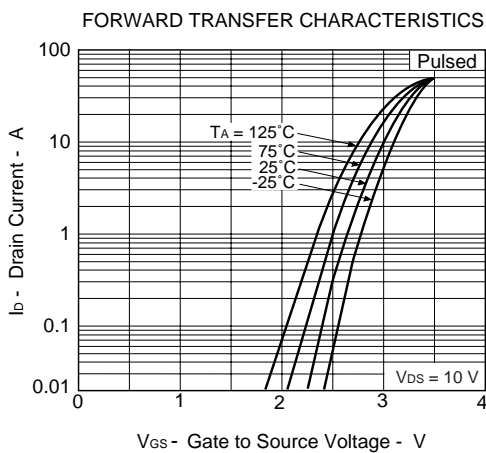


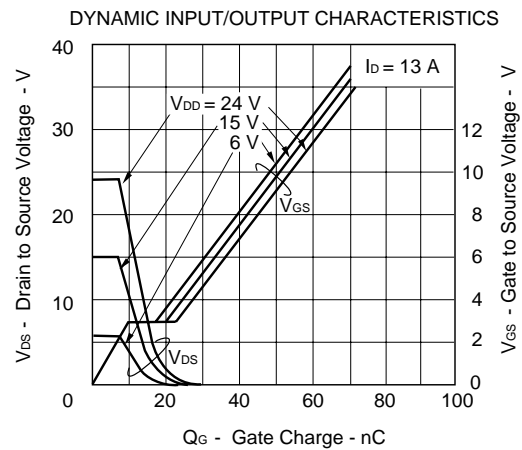
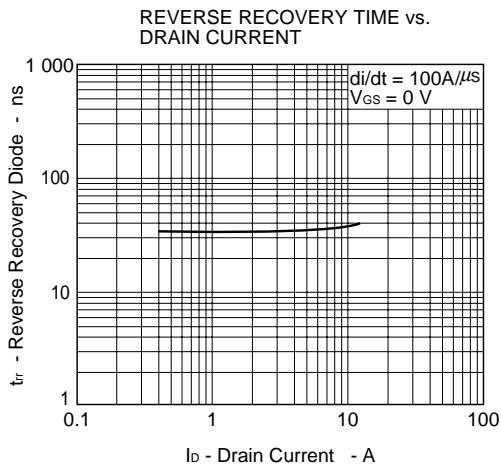
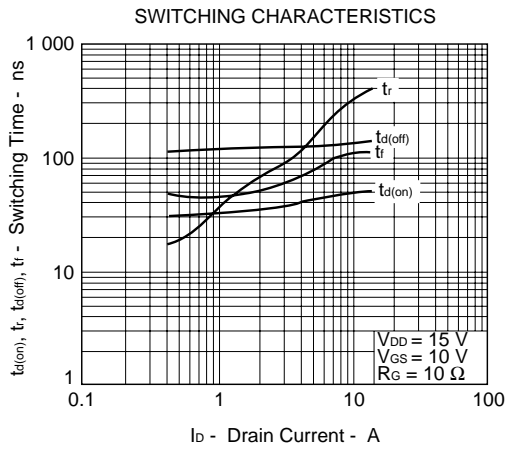
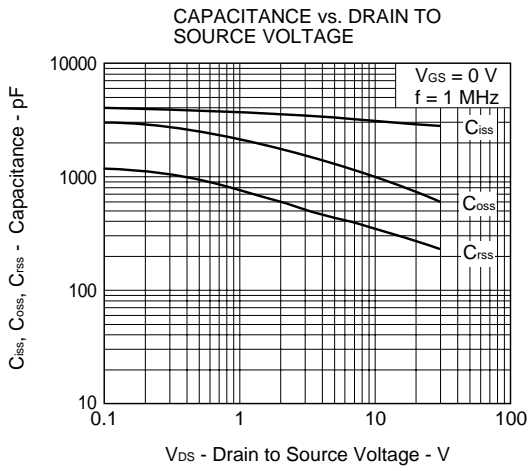
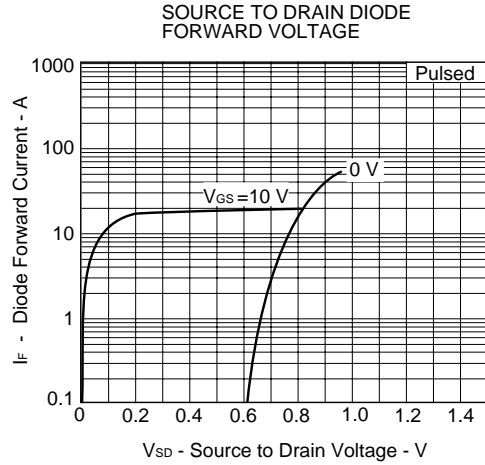
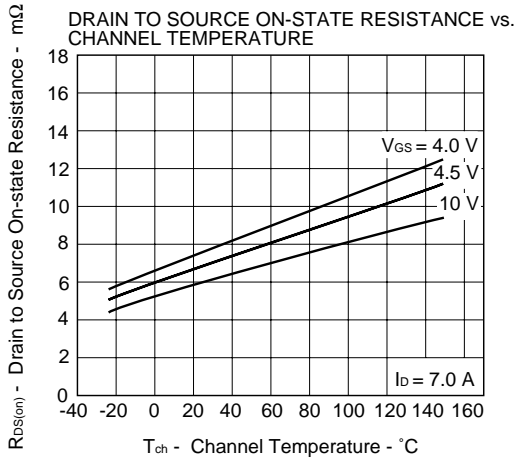
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$)



Remark Mounted on ceramic substrate of $1200\text{mm}^2 \times 0.7\text{mm}$







[MEMO]

[MEMO]

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Anti-radioactive design is not implemented in this product.