

### SWITCHING

### N-CHANNEL POWER MOS FET

### INDUSTRIAL USE

#### DESCRIPTION

The  $\mu$  PA1720 is N-Channel MOS Field Effect Transistor designed for DC / DC Converters and power management application of notebook computers.

#### FEATURES

- Low On-Resistance  
 $R_{DS(on)1} = 25.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 4.0 \text{ A)}$   
 $R_{DS(on)2} = 33.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 4.0 \text{ A)}$   
 $R_{DS(on)3} = 38.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.0 \text{ V, } I_D = 4.0 \text{ A)}$
- Low  $C_{iss}$  :  $C_{iss} = 800 \text{ pF TYP.}$
- Built-in G-S Protection Diode
- Small and Surface Mount Package (Power SOP8)

#### ORDERING INFORMATION

PART NUMBER	PACKAGE
$\mu$ PA1720G	Power SOP8

#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25 \text{ }^\circ\text{C}$ , All terminals are connected.)

Drain to Source Voltage ( $V_{GS} = 0$ )	$V_{DSS}$	30	V
Gate to Source Voltage ( $V_{DS} = 0$ )	$V_{GSS}$	$\pm 20$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 8$	A
Drain Current (Pulse) <sup>Note1</sup>	$I_{D(pulse)}$	$\pm 32$	A
Total Power Dissipation ( $T_A = 25 \text{ }^\circ\text{C}$ ) <sup>Note2</sup>	$P_T$	2.0	W
Single Avalanche Current <sup>Note3</sup>	$I_{AS}$	8.0	A
Single Avalanche Energy <sup>Note3</sup>	$E_{AS}$	6.4	mJ
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to + 150	$^\circ\text{C}$

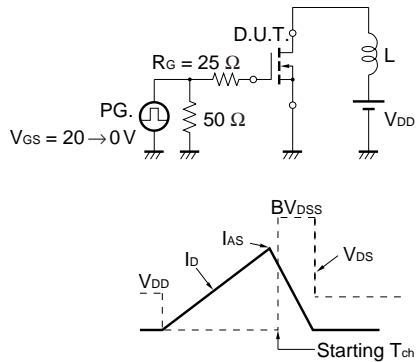
- Notes 1.**  $PW \leq 10 \text{ } \mu\text{s}$ , Duty cycle  $\leq 1 \%$
- 2.** Mounted on ceramic substrate of  $1200 \text{ mm}^2 \times 2.2 \text{ mm}$
- 3.** Starting  $T_{ch} = 25 \text{ }^\circ\text{C}$ ,  $R_G = 25 \text{ } \Omega$ ,  $V_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$

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 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

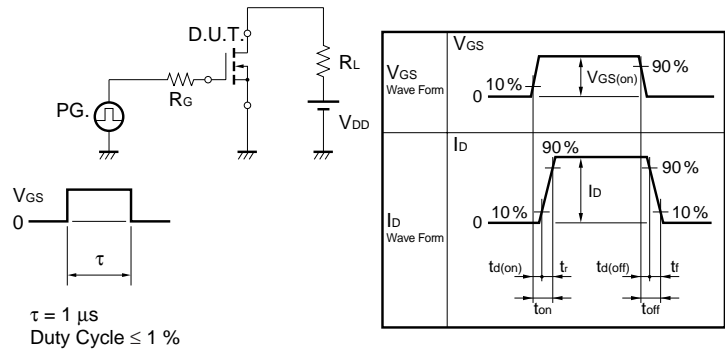
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, All terminals are connected.)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4.0 A		20.0	25.0	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 4.0 A		25.5	33.0	mΩ
	R <sub>DS(on)3</sub>	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 4.0 A		29.0	38.0	mΩ
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 4.0 A	3.0	7.0		S
Drain Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			10	μA
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0 V			±10	μA
Input Capacitance	C <sub>iSS</sub>	V <sub>DS</sub> = 10 V		800		pF
Output Capacitance	C <sub>oSS</sub>	V <sub>GS</sub> = 0 V		250		pF
Reverse Transfer Capacitance	C <sub>rSS</sub>	f = 1 MHz		96		pF
Turn-on Delay Time	t <sub>d(on)</sub>	I <sub>D</sub> = 4.0 A		20		ns
Rise Time	t <sub>r</sub>	V <sub>GS(on)</sub> = 10 V		80		ns
Turn-off Delay Time	t <sub>d(off)</sub>	V <sub>DD</sub> = 15 V		40		ns
Fall Time	t <sub>f</sub>	R <sub>G</sub> = 10 Ω		40		ns
Total Gate Charge	Q <sub>G</sub>	I <sub>D</sub> = 8 A		14		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>DD</sub> = 24 V		2.3		nC
Gate to Drain Charge	Q <sub>GD</sub>	V <sub>GS</sub> = 10 V		3.6		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 8 A, V <sub>GS</sub> = 0 V		0.86		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 8 A, V <sub>GS</sub> = 0 V		30		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		40		nC

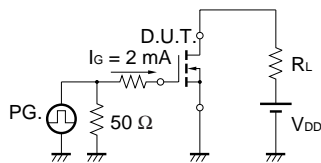
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



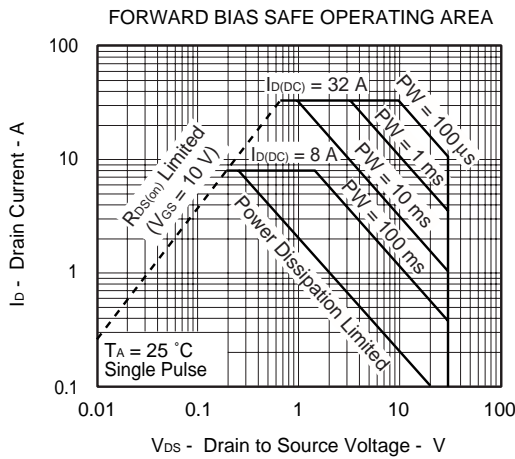
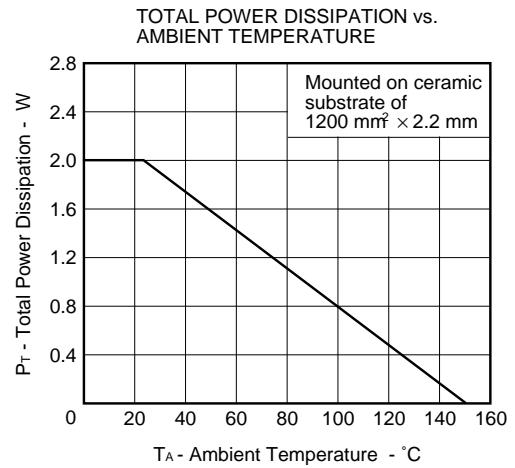
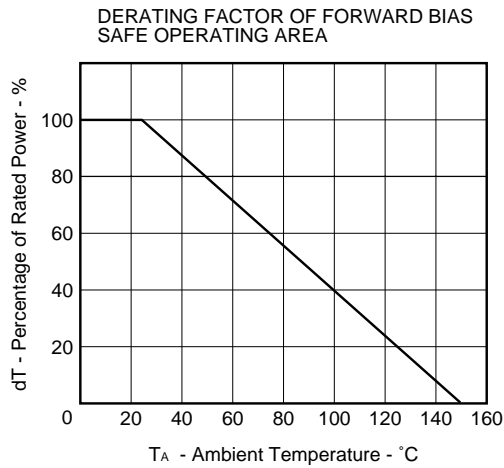
**TEST CIRCUIT 2 SWITCHING TIME**



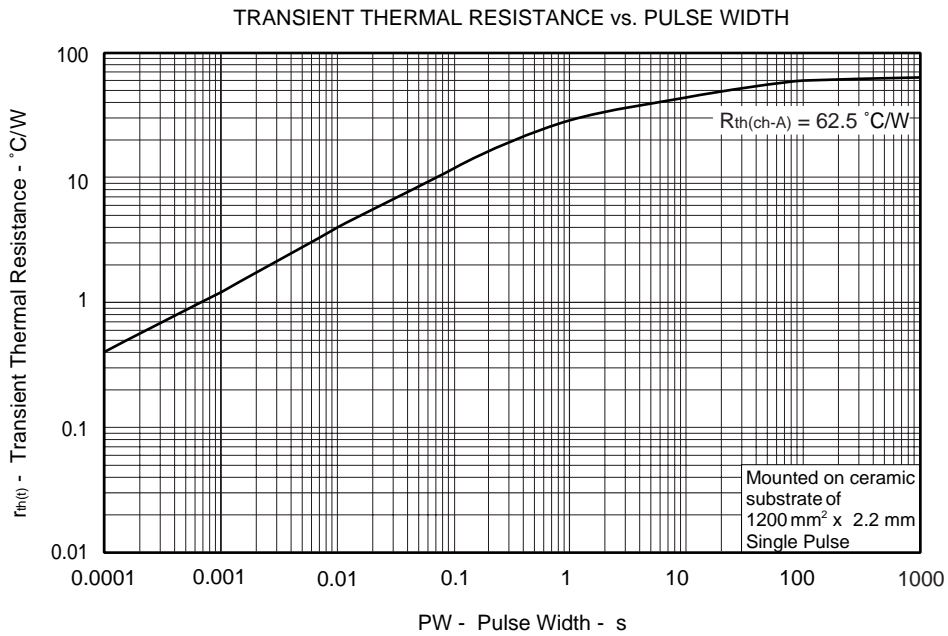
**TEST CIRCUIT 3 GATE CHARGE**

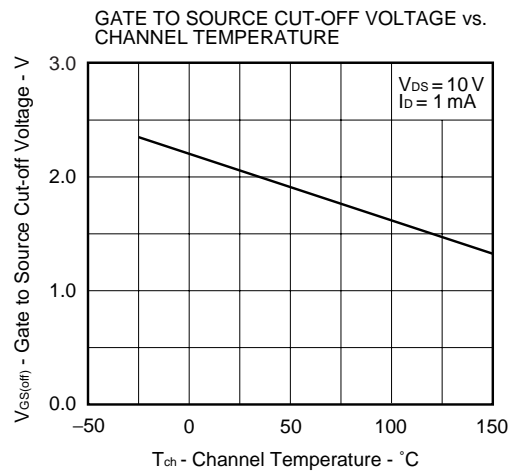
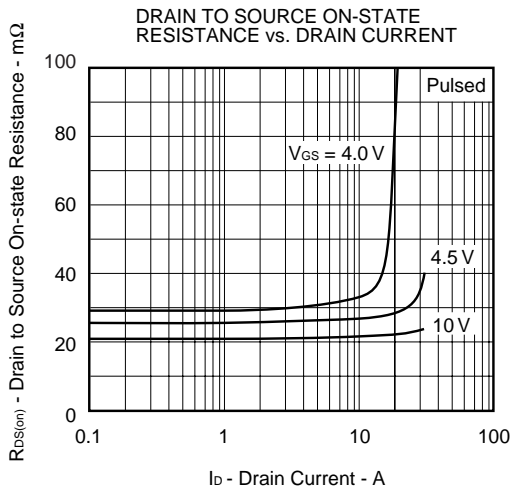
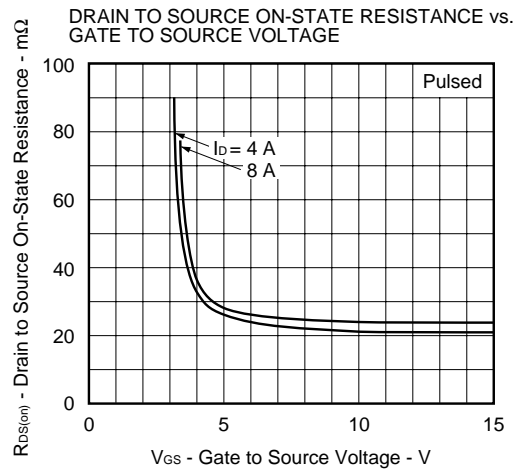
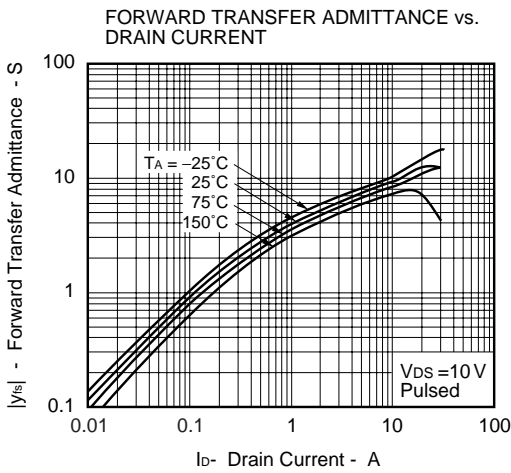
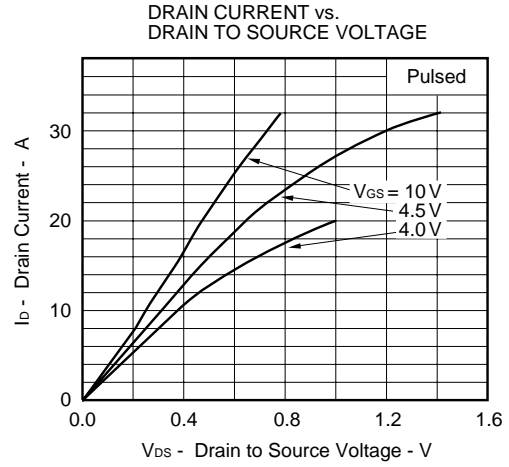
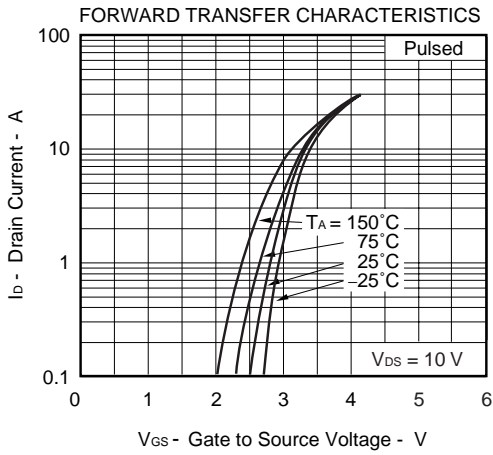


TYPICAL CHARACTERISTICS ( $T_A = 25\text{ }^\circ\text{C}$ )

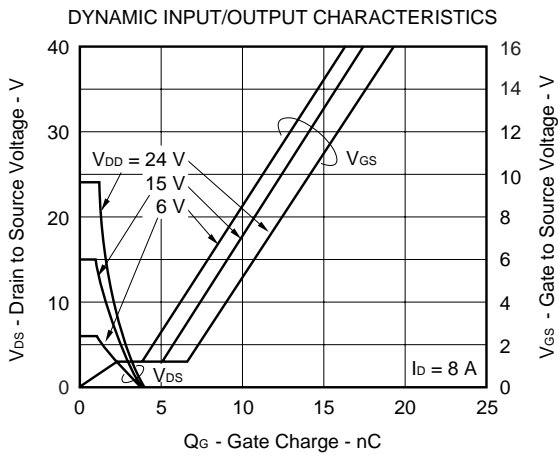
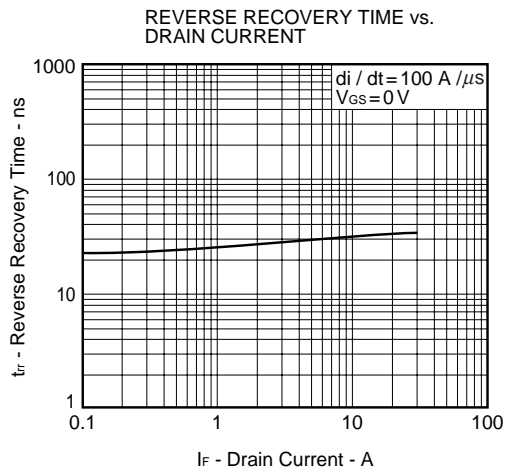
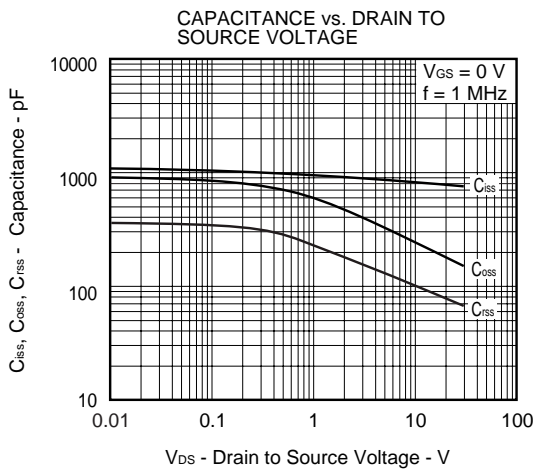
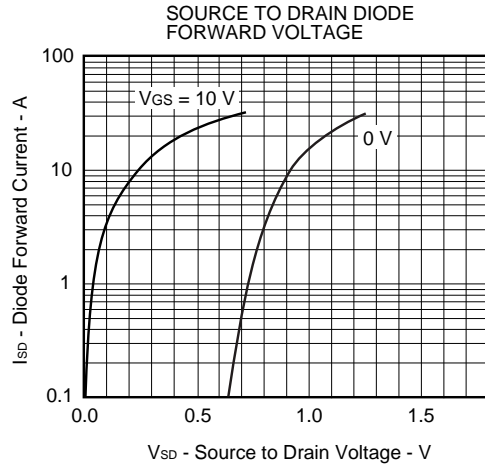
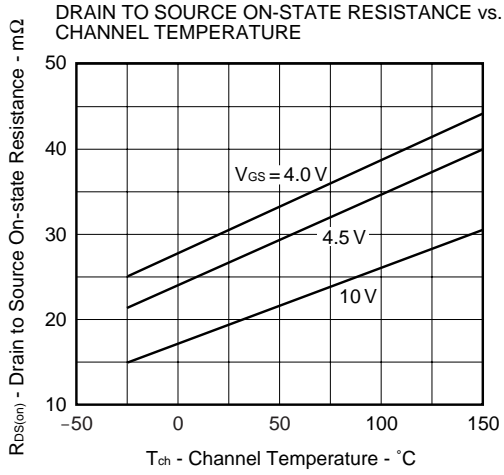


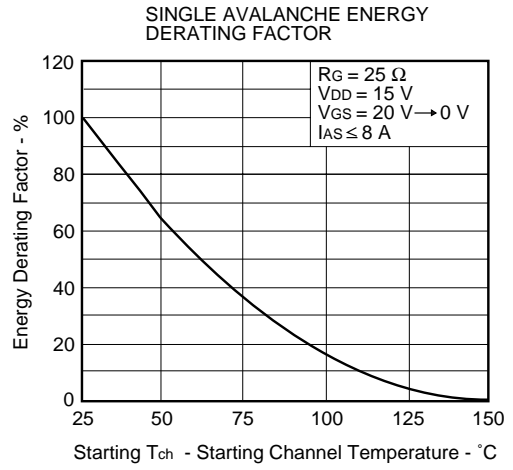
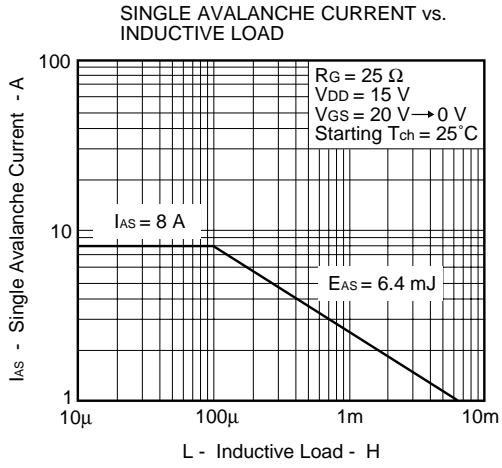
**Remark** Mounted on ceramic substrate of  $1200\text{ mm}^2 \times 2.2\text{ mm}$





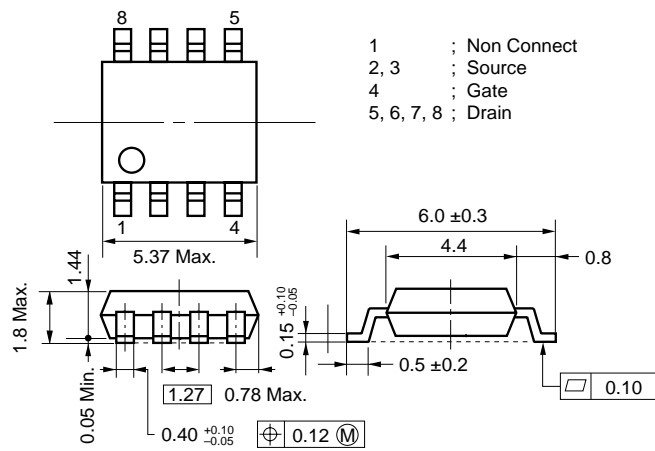
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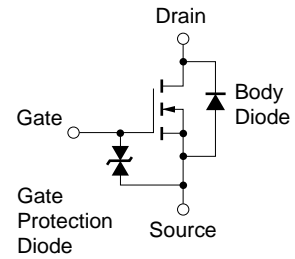


PACKAGE DRAWING (Unit : mm)

Power SOP8



EQUIVALENT CIRCUIT



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage Exceeding the rated voltage may be applied to this device.

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