

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

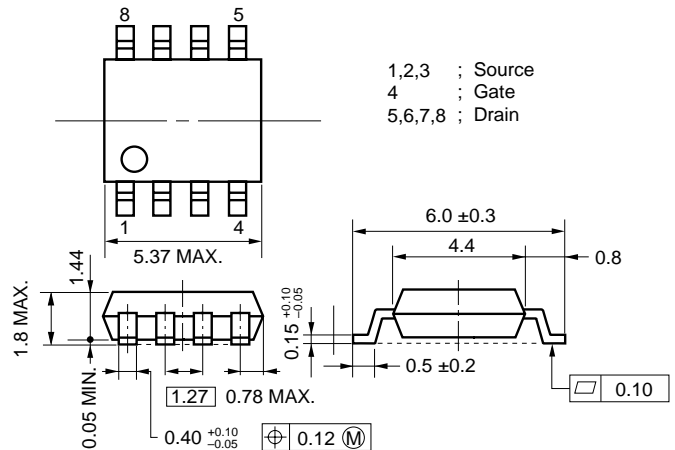
DESCRIPTION

The μPA1721 is N-Channel MOS Field Effect Transistor designed for DC/DC converters and power management applications of notebook computers.

FEATURES

- Low on-resistance
 $R_{DS(on)1} = 10.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 5.0 \text{ A)}$
 $R_{DS(on)2} = 14.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 5.0 \text{ A)}$
 $R_{DS(on)3} = 17.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.0 \text{ V, } I_D = 5.0 \text{ A)}$
- Low C_{iss} : $C_{iss} = 2200 \text{ pF TYP.}$
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit : mm)



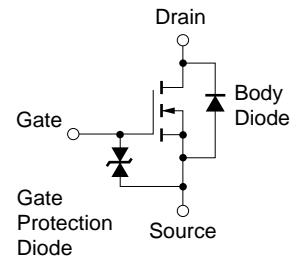
ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1721G	Power SOP8

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	30	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC)	I _{D(DC)}	±10	A
Drain Current (pulse) ^{Note1}	I _{D(pulse)}	±40	A
Total Power Dissipation (T _A = 25°C) ^{Note2}	P _T	2.0	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C

EQUIVALENT CIRCUIT



Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1 %

★ **2.** Mounted on ceramic substrate of 1200 mm² x 2.2 mm

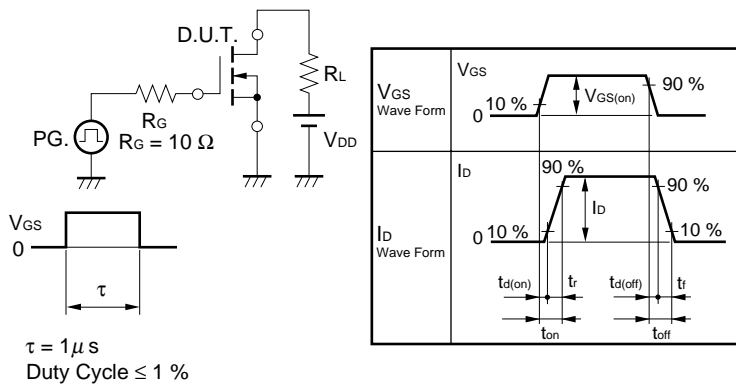
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

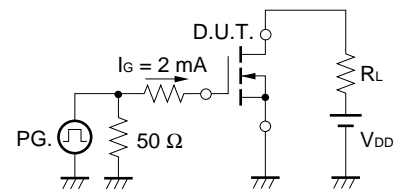
ELECTRICAL CHARACTERISTICS (T_A = 25 °C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 5.0 A		8.0	10.5	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 5.0 A		10.0	14.0	mΩ
	R _{DS(on)3}	V _{GS} = 4.0 V, I _D = 5.0 A		12.0	17.0	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 5.0 A	7.0	14.0		S
Drain Leakage Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Input Capacitance	C _{iss}	V _{DS} = 10 V		2200		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		710		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		270		pF
Turn-on Delay Time	t _{d(on)}	I _D = 5.0 A		30		ns
Rise Time	t _r	V _{GS(on)} = 10 V		90		ns
Turn-off Delay Time	t _{d(off)}	V _{DD} = 15 V		90		ns
Fall Time	t _f	R _G = 10 Ω		50		ns
Total Gate Charge	Q _G	I _D = 10 A		39		nC
Gate to Source Charge	Q _{GS}	V _{DD} = 24 V		6.3		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = 10 V		10.0		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 10 A, V _{GS} = 0 V		0.8		V
Reverse Recovery Time	t _{rr}	I _F = 10 A, V _{GS} = 0 V		40		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		50		nC

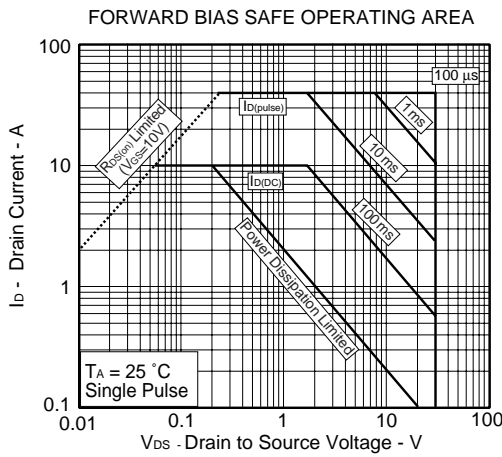
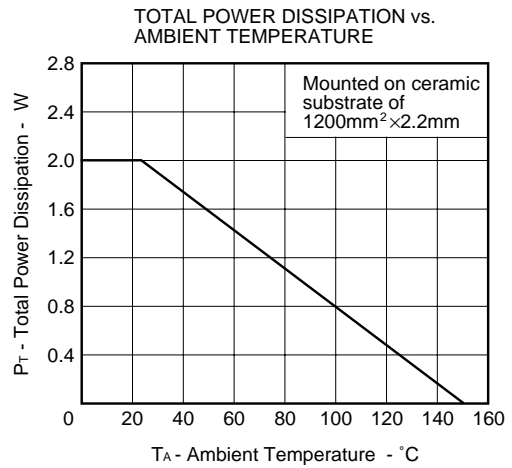
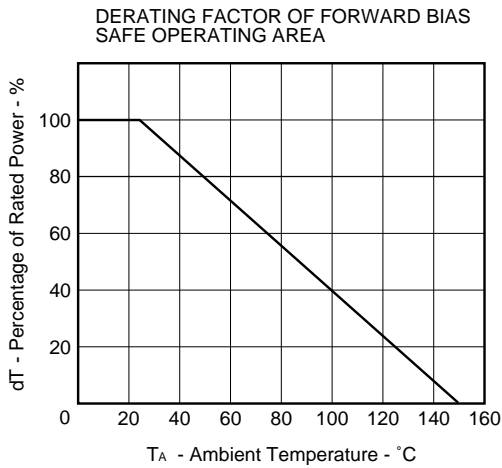
TEST CIRCUIT 1 SWITCHING TIME



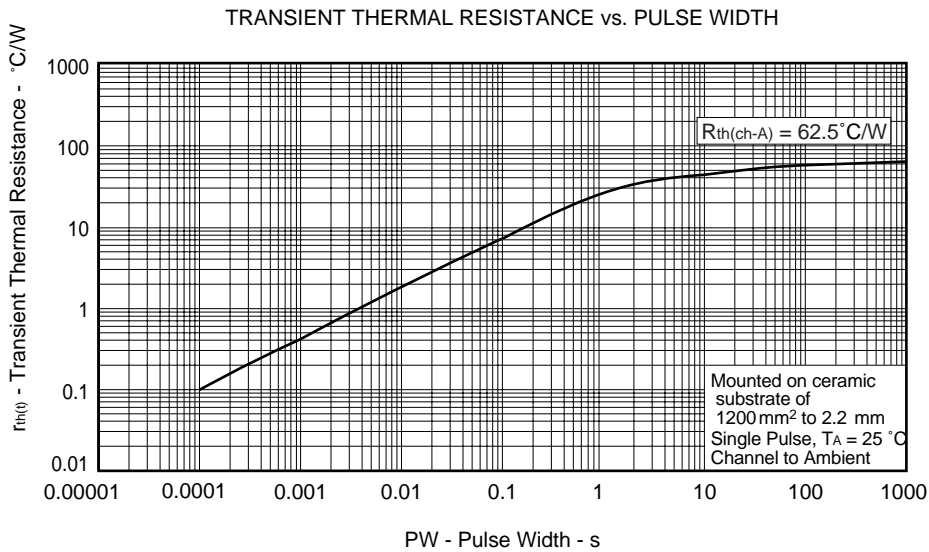
TEST CIRCUIT 2 GATE CHARGE



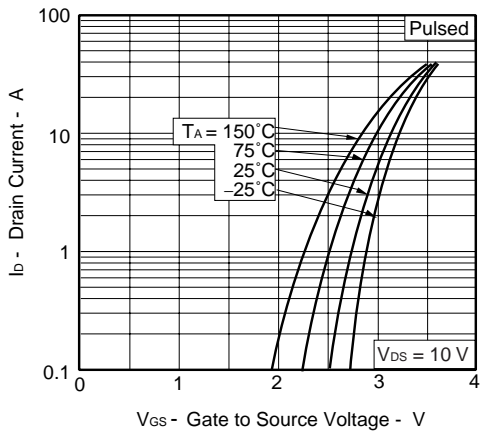
★ TYPICAL CHARACTERISTICS (T_A = 25 °C)



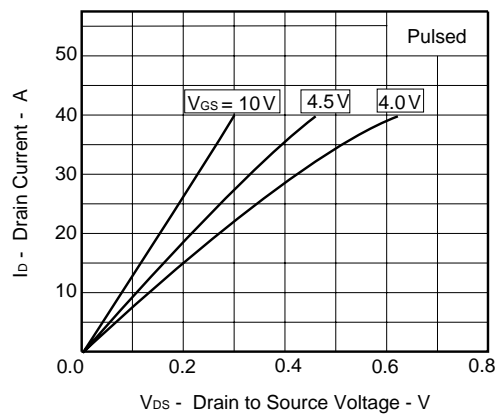
Note
Mounted on ceramicsubstrate of 1200 mm² × 2.2 mm



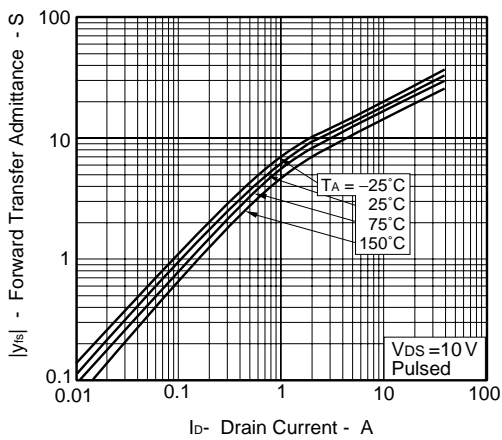
FORWARD TRANSFER CHARACTERISTICS



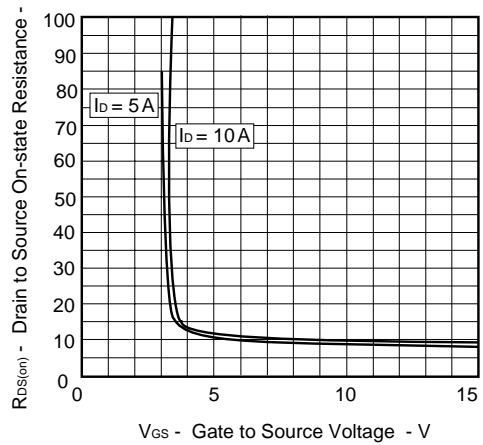
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



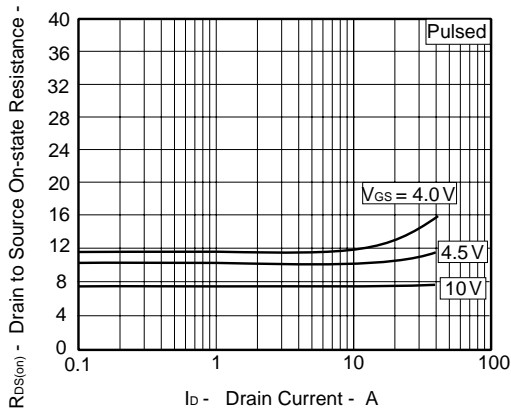
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



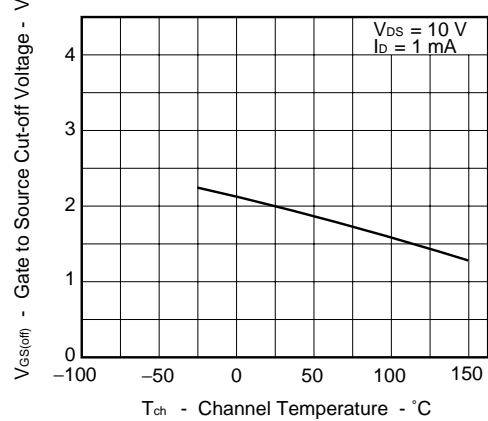
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



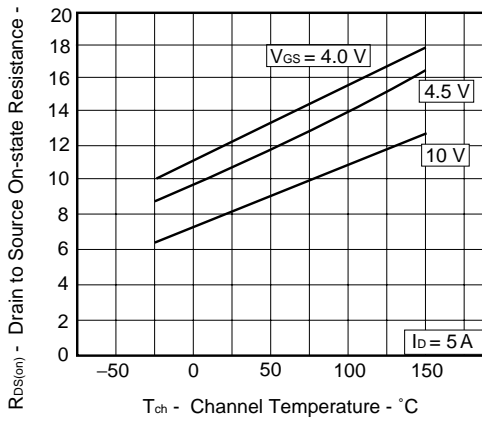
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



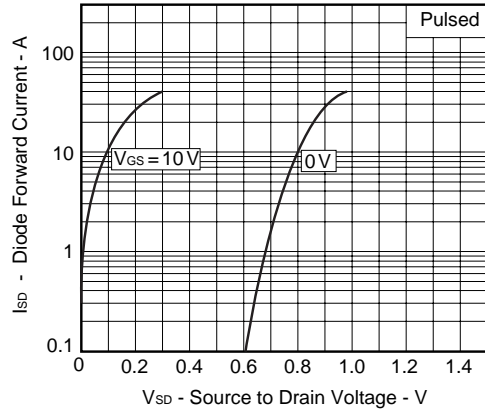
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



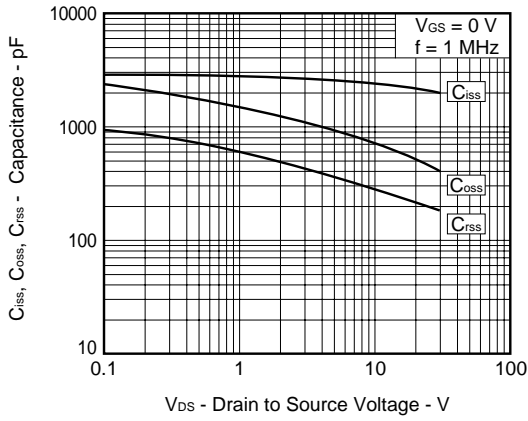
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



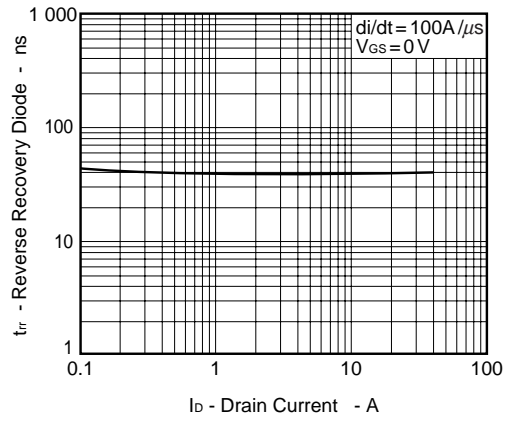
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



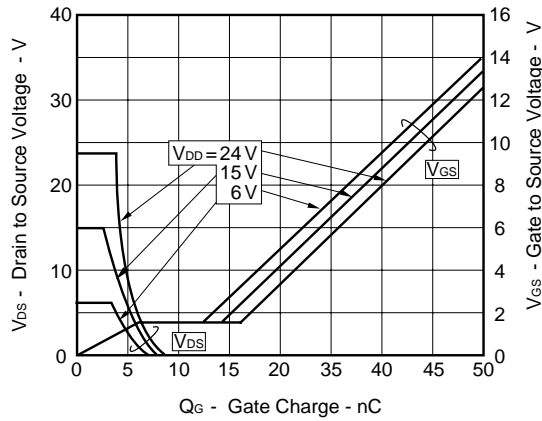
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



REVERSE RECOVERY TIME vs. DRAIN CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



[MEMO]

[MEMO]

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