

SWITCHING

N-CHANNEL POWER MOS FET

INDUSTRIAL USE

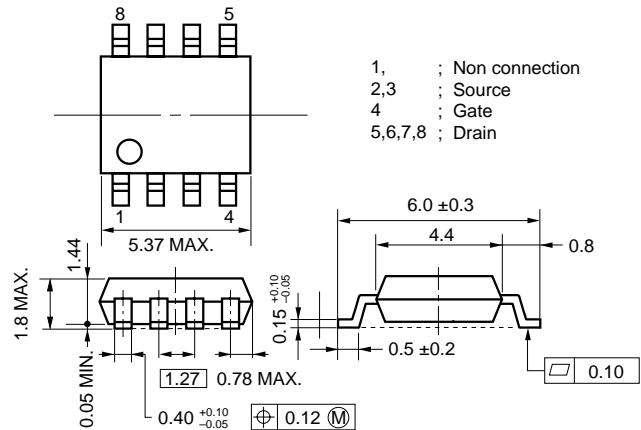
DESCRIPTION

This μ PA1725 is N-Channel MOS Field Effect Transistor designed for power management applications of notebook computers and so on.

FEATURES

- 2.5-V gate drive and low on-resistance
- ★ $R_{DS(on)1} = 21.0 \text{ m}\Omega \text{ MAX.}$ ($V_{GS} = 4.5 \text{ V}$, $I_D = 3.5 \text{ A}$)
- ★ $R_{DS(on)2} = 22.0 \text{ m}\Omega \text{ MAX.}$ ($V_{GS} = 4.0 \text{ V}$, $I_D = 3.5 \text{ A}$)
- ★ $R_{DS(on)3} = 30.0 \text{ m}\Omega \text{ MAX.}$ ($V_{GS} = 2.5 \text{ V}$, $I_D = 3.5 \text{ A}$)
- Low C_{iss} : $C_{iss} = 950 \text{ pF TYP.}$
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit : mm)



ORDERING INFORMATION

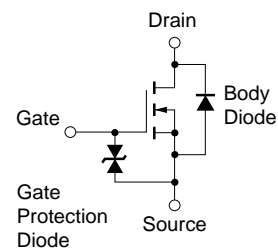
PART NUMBER	PACKAGE
μ PA1725G	Power SOP8

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, All terminals are connected.)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	20	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 12	V
Drain Current (DC)	$I_{D(DC)}$	± 7	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 28	A
Total Power Dissipation ($T_A = 25^\circ\text{C}$) ^{Note2}	P_T	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

- Notes 1.** $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1 \%$
- 2.** Mounted on ceramic substrate of $1200 \text{ mm}^2 \times 2.2 \text{ mm}$

EQUIVALENT CIRCUIT



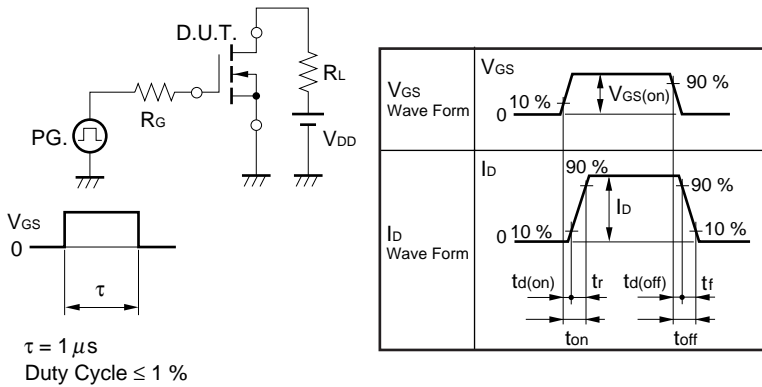
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

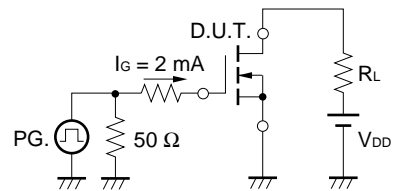
ELECTRICAL CHARACTERISTICS (T_A = 25 °C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
★ Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 4.5 V, I _D = 3.5 A		16.5	21.0	mΩ
	R _{DS(on)2}	V _{GS} = 4.0 V, I _D = 3.5 A		17.0	22.0	mΩ
	R _{DS(on)3}	V _{GS} = 2.5 V, I _D = 3.5 A		22.0	30.0	mΩ
★ Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	0.5	1.0	1.5	V
★ Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 3.5 A	5.0	11.0		S
Drain Leakage Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±12 V, V _{DS} = 0 V			±10	μA
Input Capacitance	C _{iSS}	V _{DS} = 10 V		950		pF
Output Capacitance	C _{oSS}	V _{GS} = 0 V		310		pF
Reverse Transfer Capacitance	C _{rSS}	f = 1 MHz		160		pF
Turn-on Delay Time	t _{d(on)}	I _D = 3.5 A		30		ns
Rise Time	t _r	V _{GS(on)} = 4.5 V		120		ns
Turn-off Delay Time	t _{d(off)}	V _{DD} = 10 V		70		ns
Fall Time	t _f	R _G = 10 Ω		70		ns
Total Gate Charge	Q _G	I _D = 7 A		9.6		nC
Gate to Source Charge	Q _{GS}	V _{DD} = 16 V		1.7		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = 4.5 V		4.1		nC
★ Body Diode Forward Voltage	V _{F(S-D)}	I _F = 7 A, V _{GS} = 0 V		0.8		V
Reverse Recovery Time	t _{rr}	I _F = 7 A, V _{GS} = 0 V		40		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		27		nC

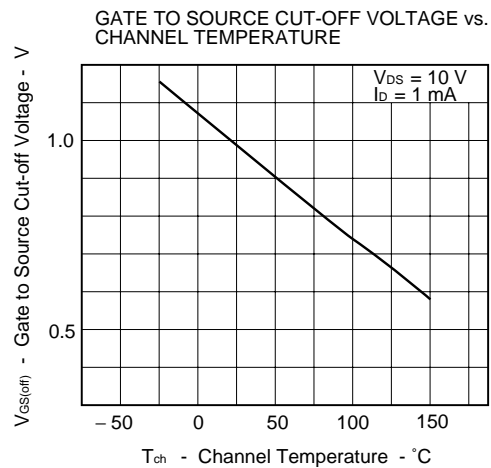
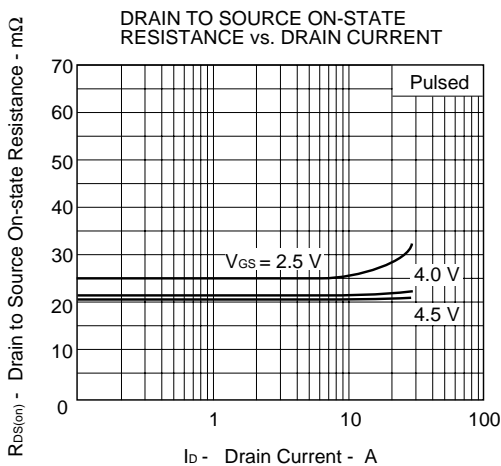
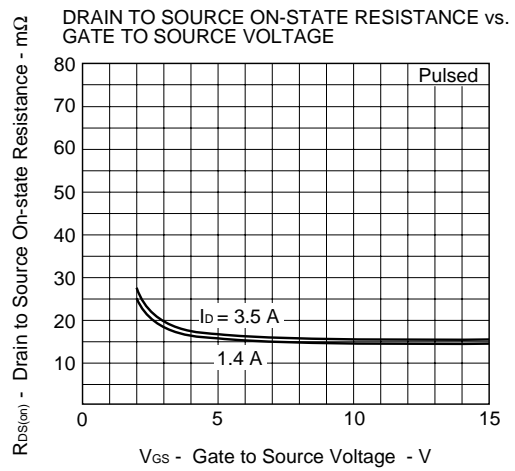
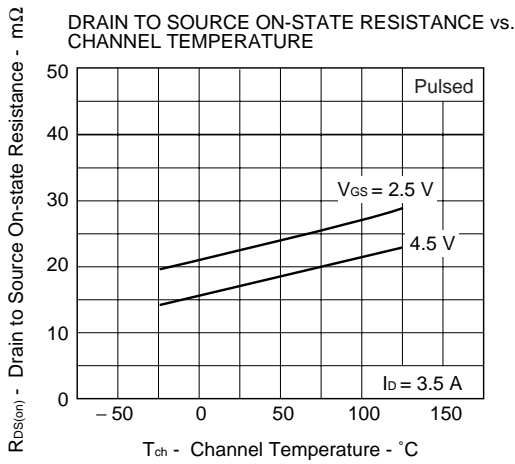
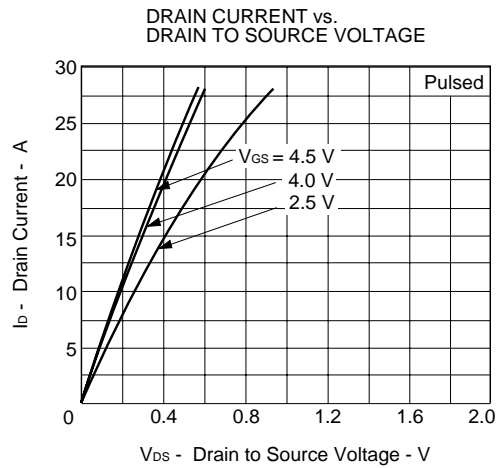
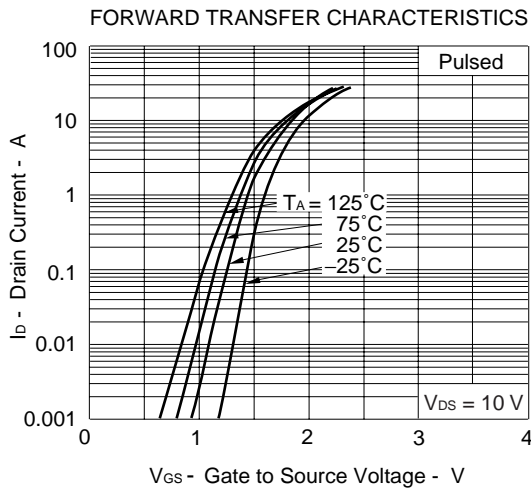
TEST CIRCUIT 2 SWITCHING TIME

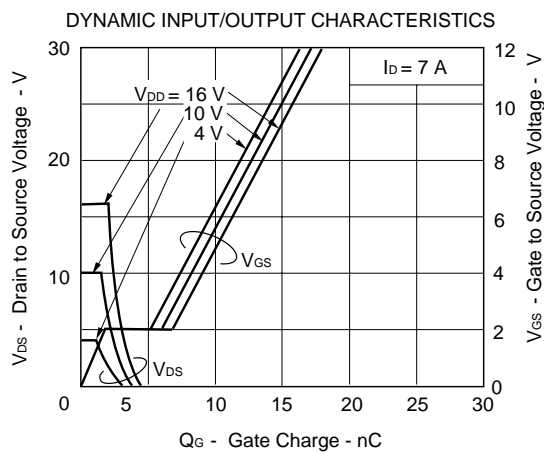
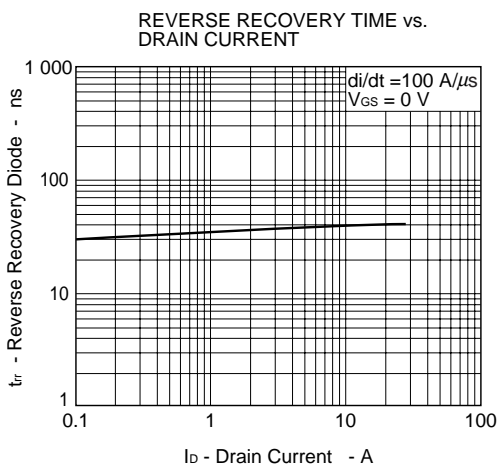
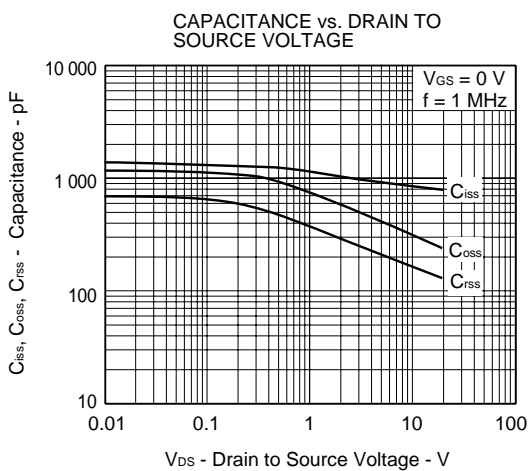
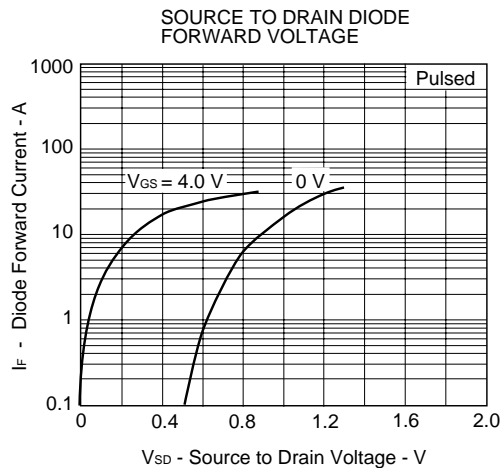
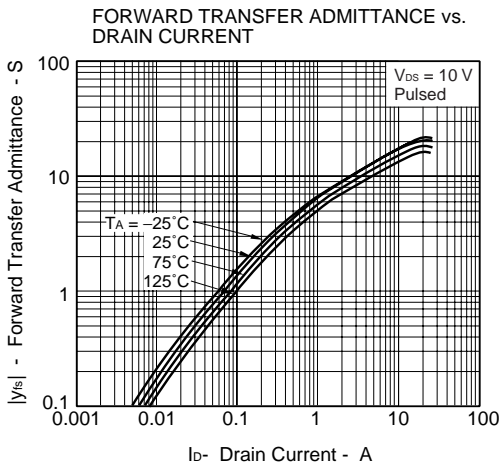


TEST CIRCUIT 3 GATE CHARGE

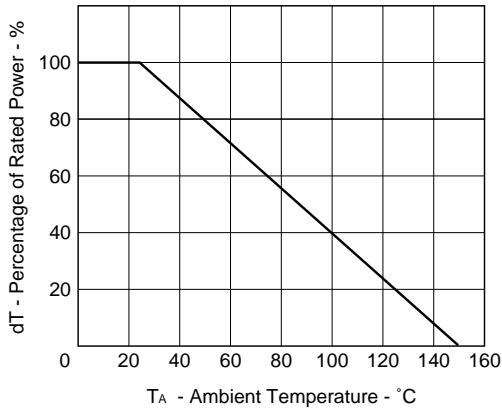


★ TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, All terminals are connected.)

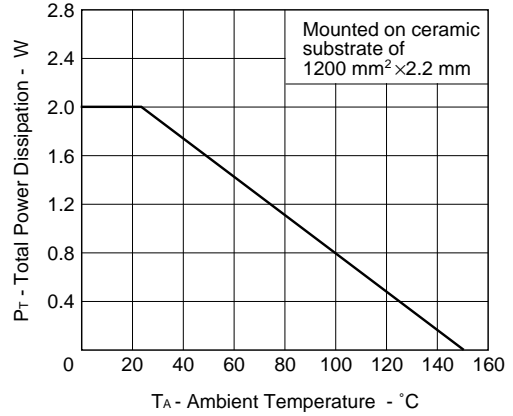




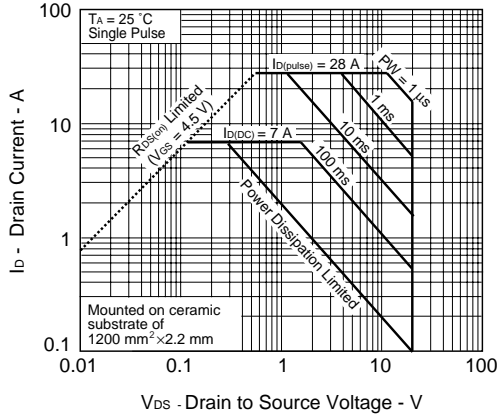
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



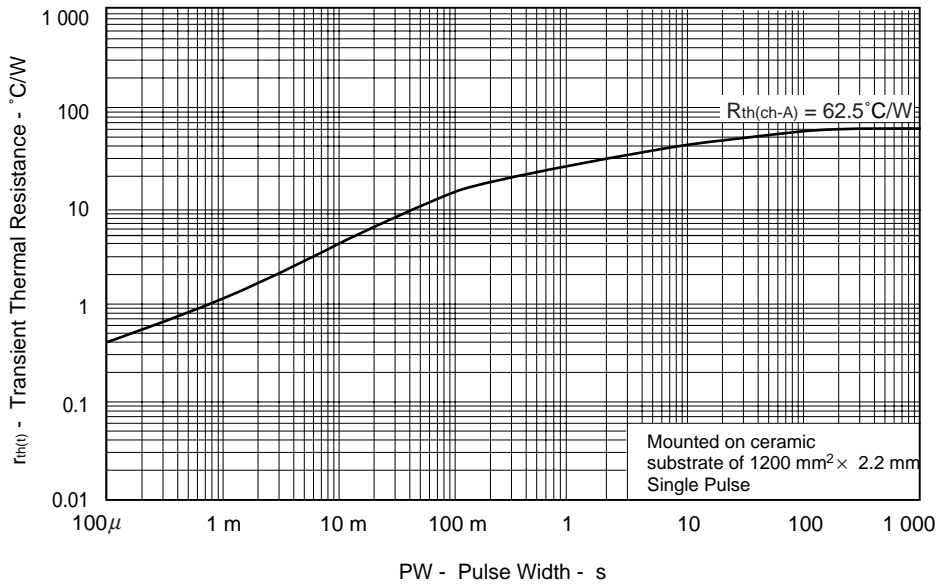
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



FORWARD BIAS SAFE OPERATING AREA



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



[MEMO]

[MEMO]

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