

MOS FIELD EFFECT TRANSISTOR

μ PA1727

SWITCHING

N-CHANNEL POWER MOS FET

DESCRIPTION

The μ PA1727 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

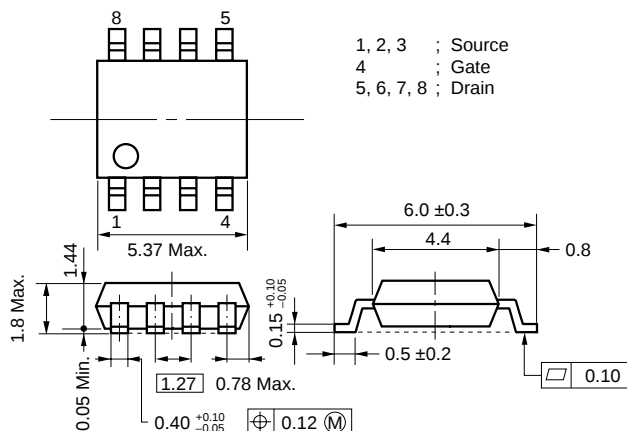
FEATURES

- Single chip type
- Low on-state resistance
 $R_{DS(on)1} = 14 \text{ m}\Omega$ TYP. ($V_{GS} = 10 \text{ V}$, $I_D = 5.0 \text{ A}$)
 $R_{DS(on)2} = 17 \text{ m}\Omega$ TYP. ($V_{GS} = 4.5 \text{ V}$, $I_D = 5.0 \text{ A}$)
 $R_{DS(on)3} = 19 \text{ m}\Omega$ TYP. ($V_{GS} = 4.0 \text{ V}$, $I_D = 5.0 \text{ A}$)
- Low C_{iss} : $C_{iss} = 2400 \text{ pF}$ TYP.
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

★ ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1727G	Power SOP8

PACKAGE DRAWING (Unit: mm)



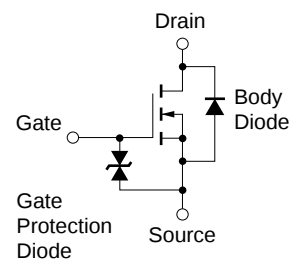
ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, All terminals are connected.)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{BSS}	60	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 10	A
Drain Current (Pulse) ^{Note1}	$I_{D(pulse)}$	± 40	A
Total Power Dissipation ($T_A = 25^\circ\text{C}$) ^{Note2}	P_T	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-55 \text{ to } +150$	$^\circ\text{C}$
Single Avalanche Current ^{Note3}	I_{AS}	10	A
Single Avalanche Energy ^{Note3}	E_{AS}	200	mJ

- Notes**
1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$
 2. Mounted on ceramic substrate of $1200 \text{ mm}^2 \times 2.2 \text{ mm}$
 3. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 30 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

EQUIVALENT CIRCUIT

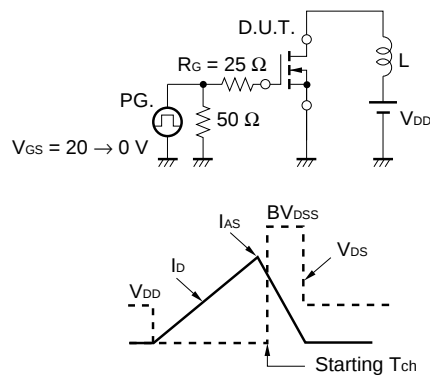


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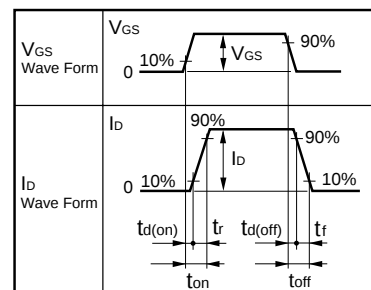
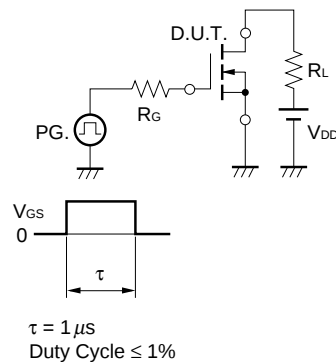
ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 5.0 A	8.0	14		S
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 5.0 A		14	19	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 5.0 A		17	22	mΩ
	R _{DS(on)3}	V _{GS} = 4.0 V, I _D = 5.0 A		19	25	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10 V		2400		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		400		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		200		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 30 V, I _D = 5.0 A		24		ns
Rise Time	t _r	V _{GS} = 10 V		120		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		120		ns
Fall Time	t _f			70		ns
Total Gate Charge	Q _G	V _{DD} = 48 V		45		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		6		nC
Gate to Drain Charge	Q _{GD}	I _D = 10 A		13		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 10 A, V _{GS} = 0 V		0.8		V
Reverse Recovery Time	t _{rr}	I _F = 10 A, V _{GS} = 0 V		45		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		84		nC

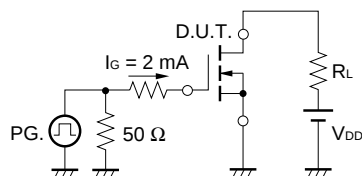
TEST CIRCUIT 1 AVALANCHE CAPABILITY



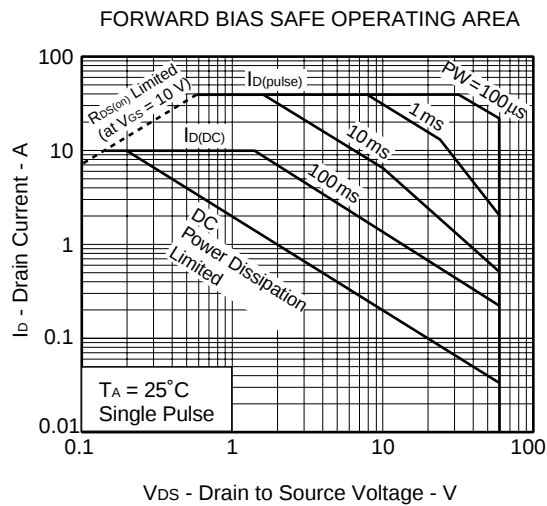
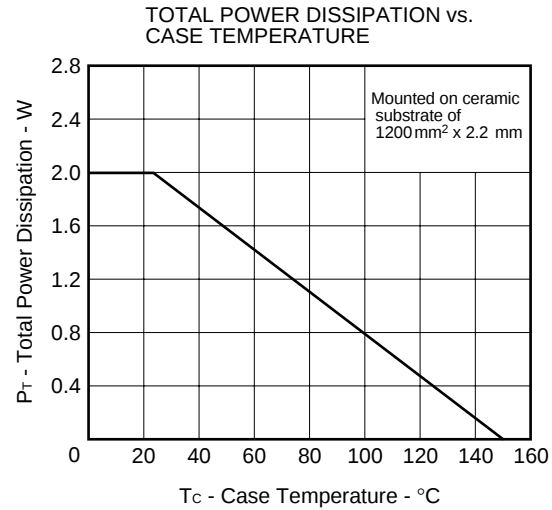
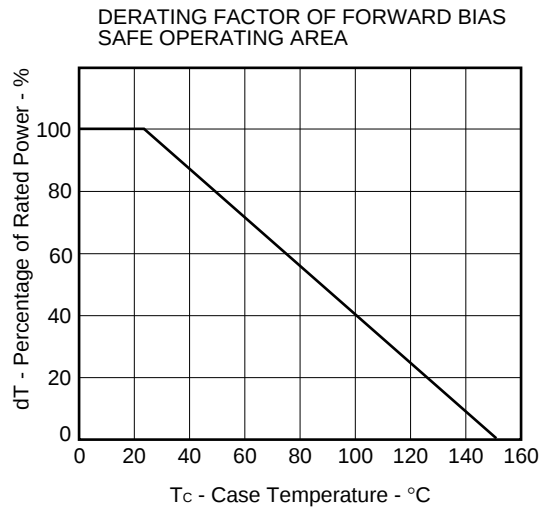
TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



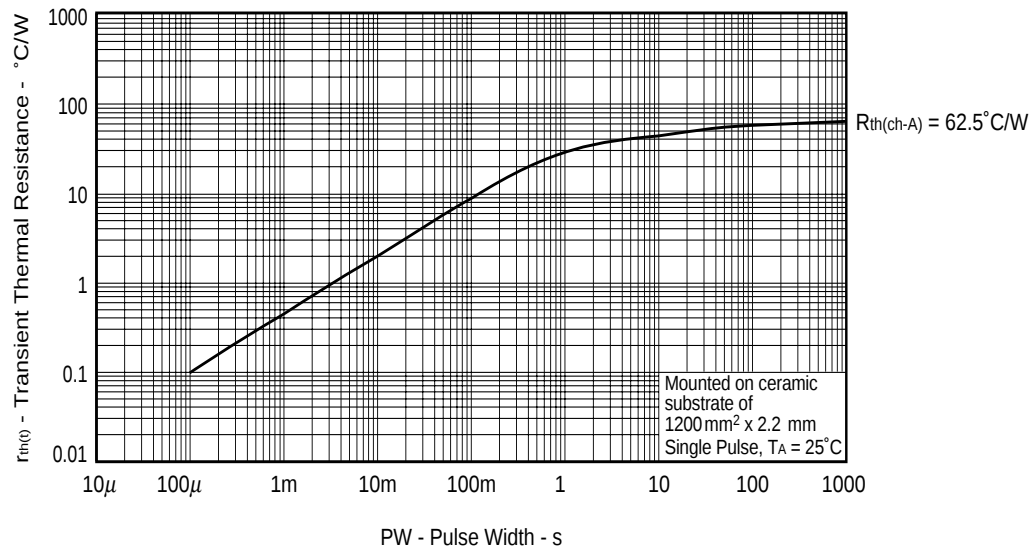
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, All terminals are connected.)



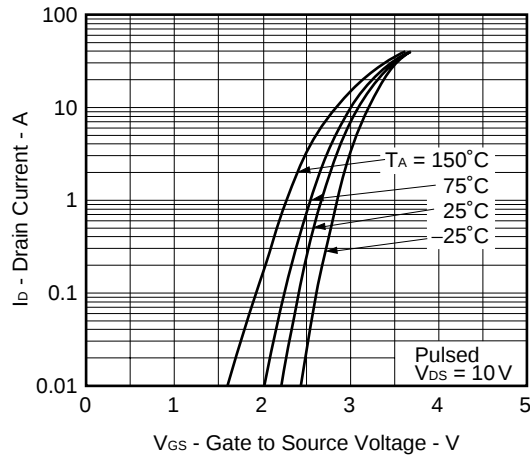
Remark

Mounted on ceramic substrate of $1200\text{ mm}^2 \times 2.2\text{ mm}$

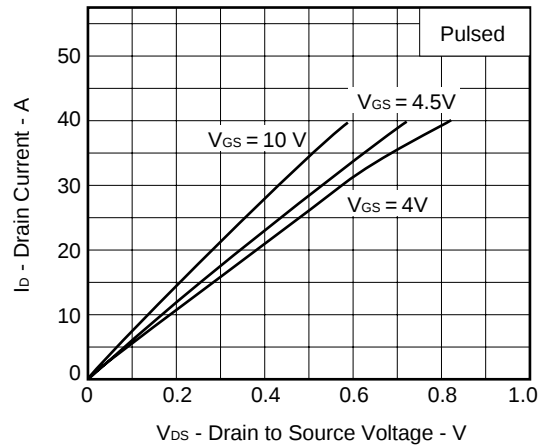
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



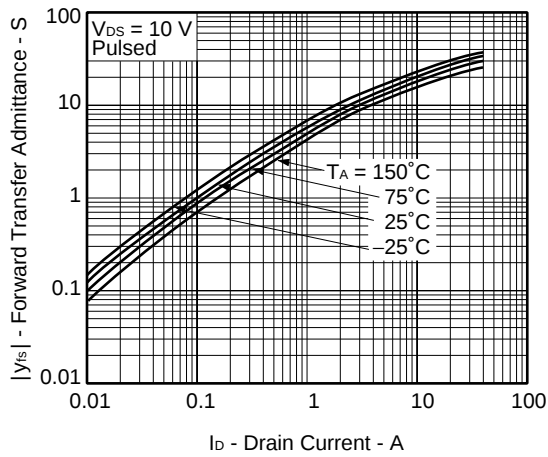
FORWARD TRANSFER CHARACTERISTICS



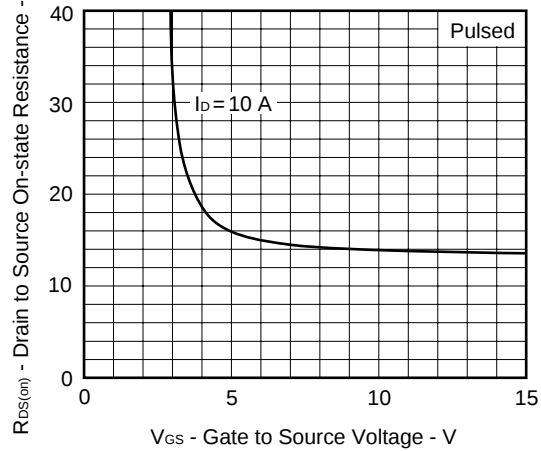
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



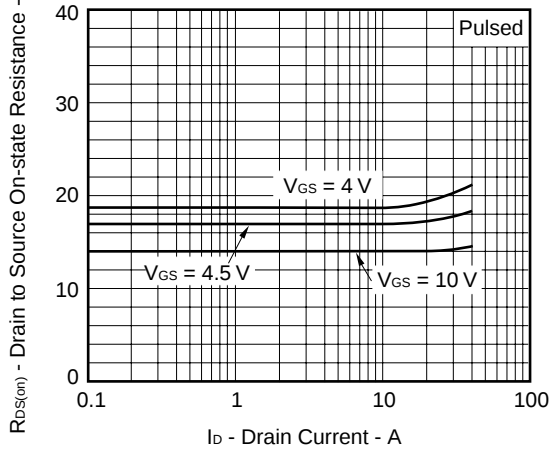
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



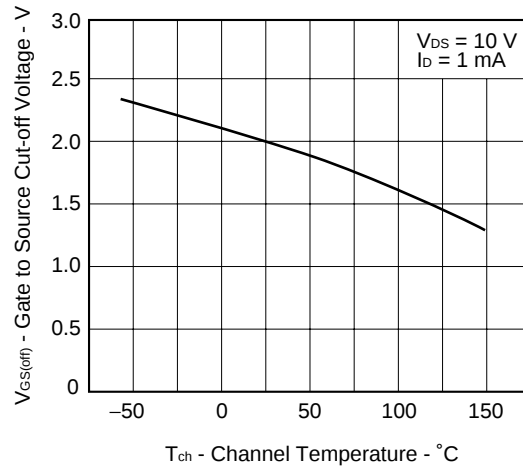
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

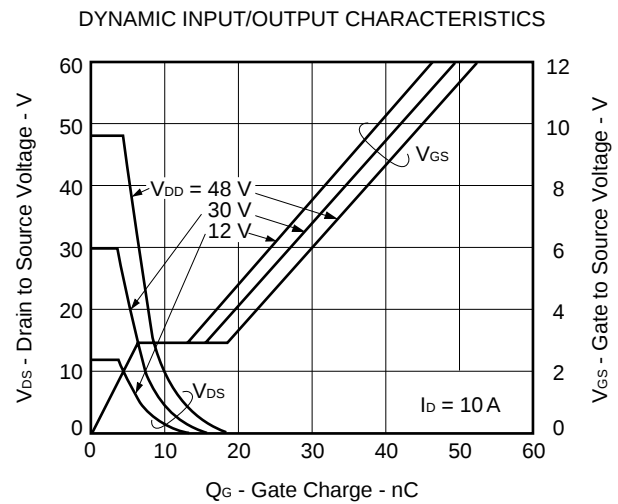
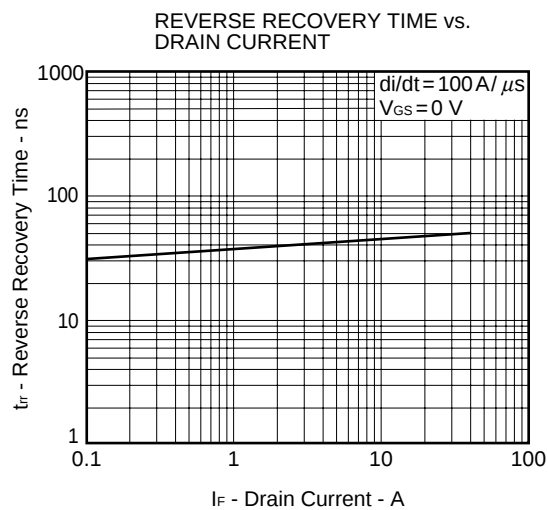
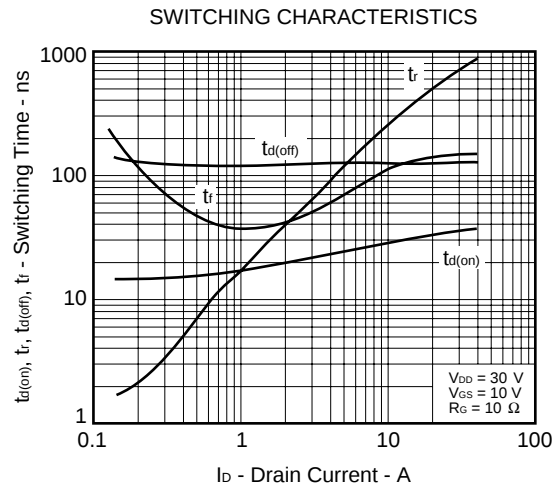
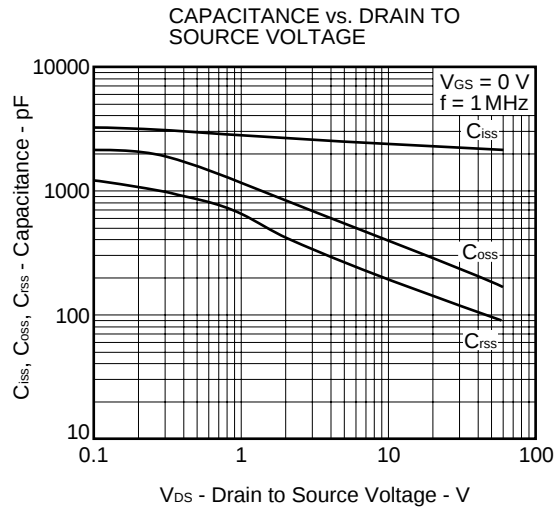
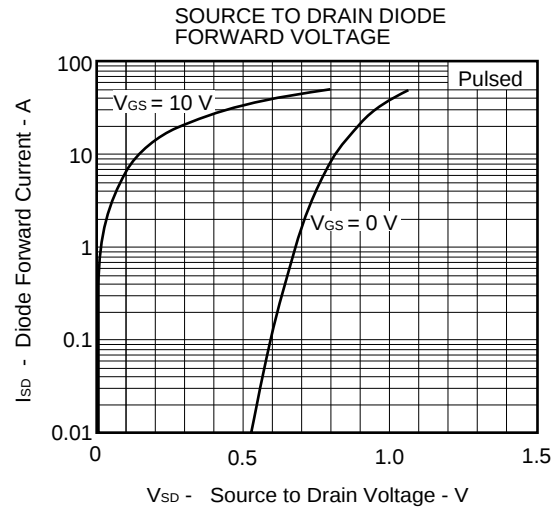
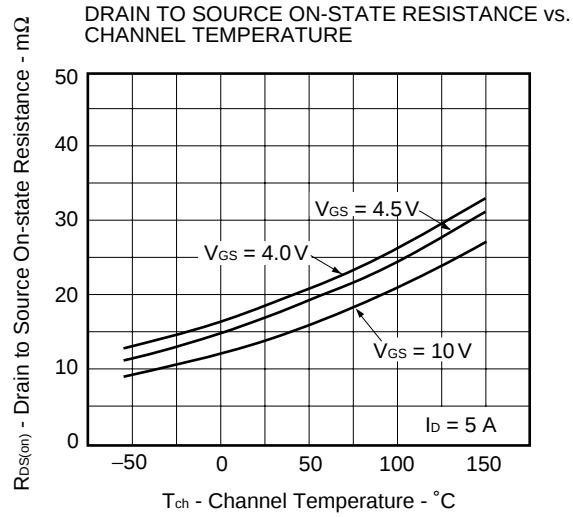


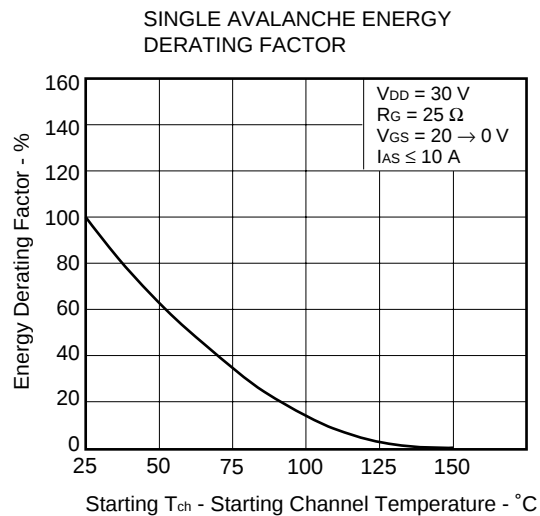
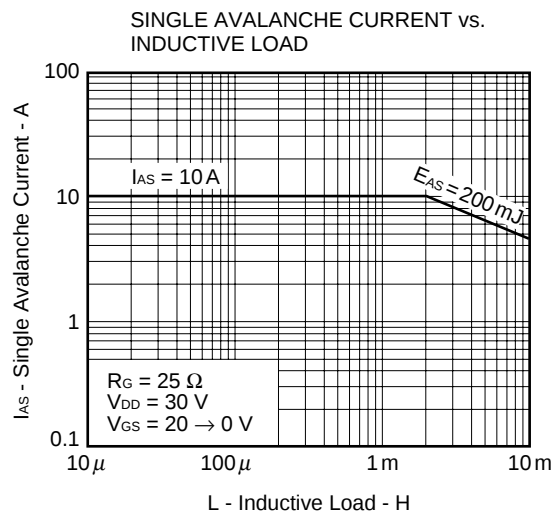
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE







[MEMO]

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