

SWITCHING
 DUAL N-CANNEL POWER MOS FET
 INDUSTRIAL USE

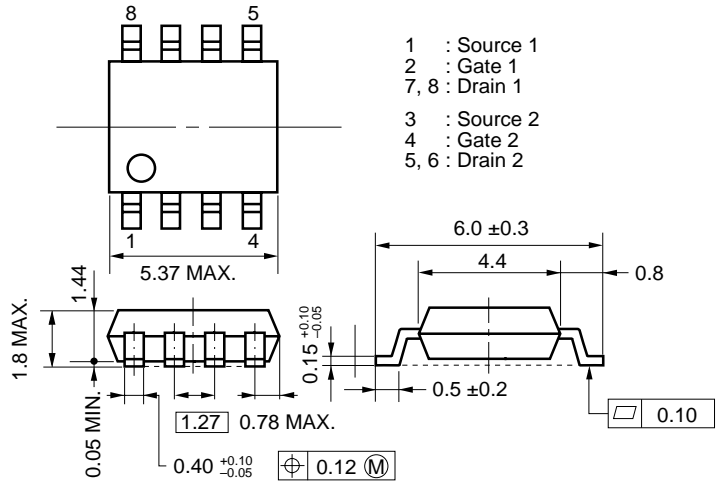
DESCRIPTION

The μ PA1764 is N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Dual chip type
- Low On-state Resistance
- ★ $R_{DS(on)1} = 27 \text{ m}\Omega$ (TYP.) ($V_{GS} = 10 \text{ V}$, $I_D = 3.5 \text{ A}$)
- ★ $R_{DS(on)2} = 32 \text{ m}\Omega$ (TYP.) ($V_{GS} = 4.5 \text{ V}$, $I_D = 3.5 \text{ A}$)
- ★ $R_{DS(on)3} = 34 \text{ m}\Omega$ (TYP.) ($V_{GS} = 4.0 \text{ V}$, $I_D = 3.5 \text{ A}$)
- Low input capacitance
- ★ $C_{iss} = 1300 \text{ pF}$ (TYP.)
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit : mm)



ORDERING INFORMATION

| PART NUMBER | PACKAGE |
|---------------|------------|
| μ PA1764G | Power SOP8 |

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, All terminals are connected.)

| | | | |
|---|----------------|-------------|------------------|
| Drain to Source Voltage | V_{DSS} | 60 | V |
| Gate to Source Voltage | V_{GSS} | ± 20 | V |
| Drain Current (DC) | $I_{D(DC)}$ | ± 7 | A |
| Drain Current (pulse) ^{Note1} | $I_{D(pulse)}$ | ± 28 | A |
| Total Power Dissipation (1 unit) ^{Note2} | P_T | 1.7 | W |
| Total Power Dissipation (2 unit) ^{Note2} | P_T | 2.0 | W |
| Channel Temperature | T_{ch} | 150 | $^\circ\text{C}$ |
| Storage Temperature | T_{stg} | -55 to +150 | $^\circ\text{C}$ |
| Single Avalanche Current ^{Note3} | I_{AS} | 7 | A |
| ★ Single Avalanche Energy ^{Note3} | E_{AS} | 98 | mJ |

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

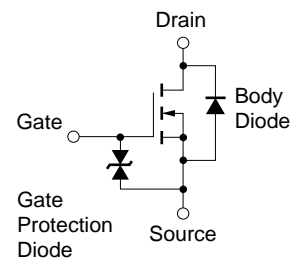
- ★ 2. Mounted on ceramic substrate of $2000 \text{ mm}^2 \times 2.2 \text{ mm}$
- 3. Starting $T_{ch} = 25^\circ\text{C}$, $R_G = 25 \Omega$, $V_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

EQUIVALENT CIRCUIT

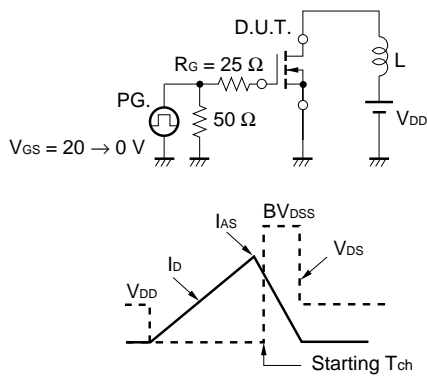
(1/2 circuit)



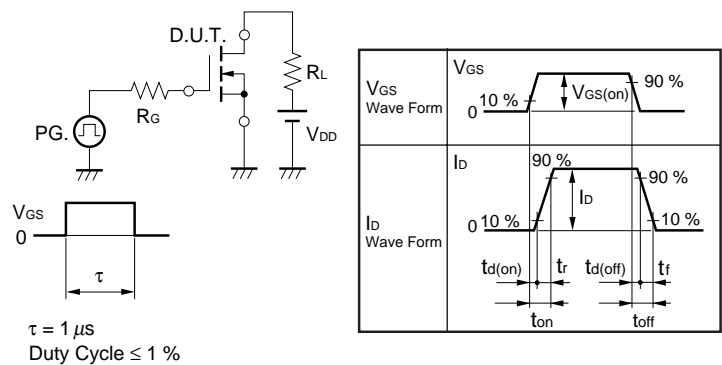
★ ELECTRICAL CHARACTERISTICS (T_A = 25 °C, All terminals are connected.)

| CHARACTERISTICS | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-------------------------------------|----------------------|---|------|------|------|------|
| Drain to Source On-state Resistance | R _{DS(on)1} | V _{GS} = 10 V, I _D = 3.5 A | | 27 | 35 | mΩ |
| | R _{DS(on)2} | V _{GS} = 4.5 V, I _D = 3.5 A | | 32 | 42 | mΩ |
| | R _{DS(on)3} | V _{GS} = 4.0 V, I _D = 3.5 A | | 34 | 46 | mΩ |
| Gate to Source Cut-off Voltage | V _{GS(off)} | V _{DS} = 10 V, I _D = 1 mA | 1.5 | 2.0 | 2.5 | V |
| Forward Transfer Admittance | y _{fs} | V _{DS} = 10 V, I _D = 3.5 A | 5.0 | 9.0 | | S |
| Drain Leakage Current | I _{DSS} | V _{DS} = 60 V, V _{GS} = 0 V | | | 10 | μA |
| Gate to Source Leakage Current | I _{GSS} | V _{GS} = ±20 V, V _{DS} = 0 V | | | ±10 | μA |
| Input Capacitance | C _{iSS} | V _{DS} = 10 V | | 1300 | | pF |
| Output Capacitance | C _{oSS} | V _{GS} = 0 V | | 230 | | pF |
| Reverse Transfer Capacitance | C _{rSS} | f = 1 MHz | | 110 | | pF |
| Turn-on Delay Time | t _{d(on)} | I _D = 3.5 A | | 15 | | ns |
| Rise Time | t _r | V _{GS(on)} = 10 V | | 69 | | ns |
| Turn-off Delay Time | t _{d(off)} | V _{DD} = 30 V | | 65 | | ns |
| Fall Time | t _f | R _G = 10 Ω | | 27 | | ns |
| Total Gate Charge | Q _G | I _D = 7.0 A | | 29 | | nC |
| Gate to Source Charge | Q _{GS} | V _{DD} = 48 V | | 3.6 | | nC |
| Gate to Drain Charge | Q _{GD} | V _{GS} = 10 V | | 7.4 | | nC |
| Body Diode Forward Voltage | V _{F(S-D)} | I _F = 7.0 A, V _{GS} = 0 V | | 0.84 | | V |
| Reverse Recovery Time | t _{rr} | I _F = 7.0 A, V _{GS} = 0 V | | 40 | | ns |
| Reverse Recovery Charge | Q _{rr} | di/dt = 100 A / μs | | 66 | | nC |

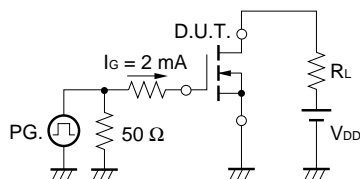
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



[MEMO]

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