

Description

The μPD4364 is a high-speed, 8192-word by 8-bit static RAM. Its unique circuitry, using CMOS peripheral circuits and N-channel memory cells with polysilicon resistors, makes the μPD4364 a very low-power device that requires no clock or refreshing to operate.

Two chip enable pins are provided for battery backup application, and an output enable pin is provided for easy interface. Data retention is guaranteed at a power supply voltage as low as 2 V (-xxL and -xxLL versions).

The μPD4364 is packaged in standard and slim 28-pin plastic DIP, as well as plastic miniflat packages that are plug-in compatible with 2764-type EPROMs.

Features

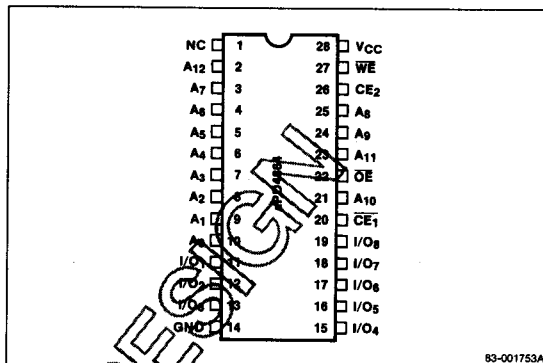
- ☐ Single +5-volt power supply
- ☐ Fully static operation—no clock or refreshing required
- ☐ TTL-compatible—all inputs and outputs
- ☐ Common I/O using three-state outputs
- ☐ One output enable and two chip enable pins for easy application
- ☐ Data retention voltage: 2 V min for -xxL and -xxLL versions
- ☐ Plug-in compatible with 2764-type EPROMs
- ☐ Standard 28-pin plastic DIP
- ☐ 28-pin 300 mil plastic slim DIP
- ☐ 28-pin plastic miniflat package

Pin Identification

Name	Function
A ₀ -A ₁₂	Address input
I/O ₁ -I/O ₈	Data input/output
CE ₁	Chip enable input, active low
CE ₂	Chip enable input, active high
OE	Output enable input
WE	Write enable input
GND	Ground
V _{CC}	+5-volt power supply
NC	No connection

Pin Configuration

28-Pin Plastic DIP or Miniflat



Ordering Information

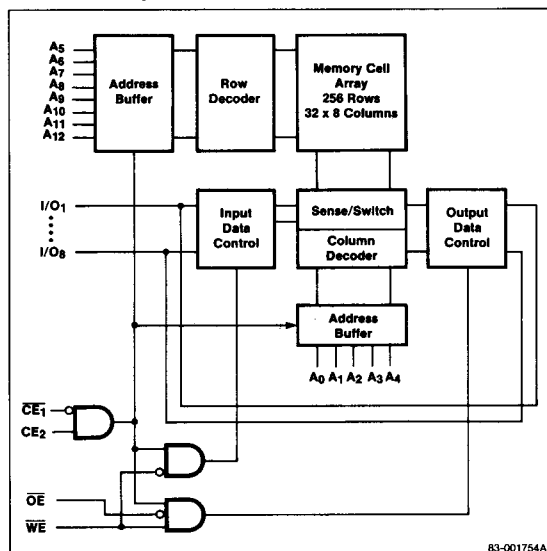
Part Number (Notes 1, 2, 3)	Standby Current (max)	Access Time (max)	Package
μPD4364C-xx	2 mA	(Notes 1, 4)	28-pin DIP
C-xxL	100 μA		
C-xxLL	50 μA		
CX-xx	2 mA	(Notes 1, 5)	28-pin slim DIP
CX-xxL	100 μA		
μPD4364G-xx	2 mA	(Notes 1, 4)	28-pin miniflat
G-xxL	100 μA		
G-xxLL	50 μA		

Notes:

- (1) The symbol "xx" in the part number denotes access time.

xx	Access Time (max)
10	100 ns
12	120 ns
15	150 ns
20	200 ns
- (2) The symbol C, CX, or G in the part number denotes a 28-pin plastic package.
C = 600-mil DIP
CX = 300-mil slim DIP
G = Miniflat
- (3) Part number example: μPD4364CX-12L denotes a 300-mil DIP package, 120-ns maximum access time, and 100-μA maximum standby current.
- (4) Contact your NEC sales representative for availability of a -10LL version.
- (5) A 200-ns access time is not available in the CX package.

Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{CC} (Note 1)	-0.5 to 7.0 V
Input voltage, V_{IN} (Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage, V_{OUT} (Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Operating temperature, T_{OPR}	0 to 70°C
Storage temperature, T_{STG}	-55 to 125°C
Power dissipation, P_D	1.0 W

Notes:

(1) -3.0 V min (pulse width of 50 ns max)

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under Recommended DC Operating Conditions.

Capacitance

 $T_A = 25^\circ\text{C}; f = 1.0\text{ MHz}$

Parameter	Symbol	Limits			Test Conditions
		Min	Typ	Max	
Input capacitance	C_i			(1)	pF $V_i = 0$ V
Input/output capacitance	$C_{i/o}$			8	pF $V_{i/o} = 0$ V

Notes:

- (1) Maximum input capacitance
CX package: 5 pF
C or G package, 100-ns version: 5 pF
C or G package, except 100-ns version: 6 pF

Recommended DC Operating Conditions

$T_A = 0$ to $+70^\circ\text{C}$

Parameter	Symbol	Limits			Unit
		Min	Typ	Max	
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input voltage, low	V _{IL}	-0.3 (Note 1)		0.8	V
Input voltage, high	V _{IH}	2.2		V _{CC} + 0.5	V

Notes:

(1) -3.0 V min (pulse width 50 ns max)

DC Characteristics

$T_A = 0$ to $+70^\circ\text{C}$; $V_{CC} = 5\text{ V} \pm 10\%$

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input leakage current	I_{LI}			1	μA	$V_{IN} = 0 V$ to V_{CC}
Output leakage current	I_{LO}			1	μA	$V_{I/O} = 0 V$ to V_{CC} $CE_1 = V_{IH}$ or $CE_2 = V_{IL}$ or $OE = V_{IH}$ or $WE = V_{IL}$
Operating supply current	I_{CCA1}			(1)	mA	$\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$, $I_{I/O} = 0$, Min cycle
	I_{CCA2}		5	10	mA	$\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$, $I_{I/O} = 0$, DC current
	I_{CCA3}		3	5	mA	$\overline{CE}_1 \leq 0.2 V$, $CE_2 \geq V_{CC} - 0.2 V$, $V_{IL} \leq 0.2 V$, $V_{IH} \geq V_{CC} - 0.2 V$, $f = 1 MHz$, $I_{I/O} = 0$
Standby supply current	I_{SB}			(2)	mA	$\overline{CE}_1 \geq V_{IH}$ or $CE_2 = V_{IL}$
	I_{SB1}			(3)	mA	$\overline{CE}_1 \geq V_{CC} - 0.2 V$ $CE_2 \geq V_{CC} - 0.2 V$
	I_{SB2}			(3)	mA	$CE_2 \leq 0.2 V$
Output voltage, low	V_{OL}			0.4	V	$I_{OL} = 2.1 mA$
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -1.0 mA$

Notes:

- (1) μ PD4364-10/10L: 45 mA max
 μ PD4364-12/12L/12LL: 40 mA max
 μ PD4364-15/15L/15LL: 40 mA max
 μ PD4364-20/20L/20LL: 35 mA max
- (2) μ PD4364-xx: 5 mA max
 μ PD4364-xxL: 3 mA max
 μ PD4364-xxLL: 3 mA max
- (3) μ PD4364-xx: 2 mA max
 μ PD4364-xxL: 100 μ A max
 μ PD4364-xxLL: 50 μ A max

AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5 V ±10%

Parameter	Symbol	Limits								Unit
		μ PD4364 -10/10L		μ PD4364 -12/12L/12LL		μ PD4364 -15/15L/15LL		μ PD4364 -20/20L/20LL		
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle										
Read cycle time	t _{RC}	100		120		150		200		ns
Address access time	t _{AA}		100		120		150		200	ns
$\overline{CE}_1$ access time	t _{C01}		100		120		150		200	ns
CE ₂ access time	t _{C02}		100		120		150		200	ns
Output enable to output valid	t _{OE}		50		60		70		100	ns
Output hold from address change	t _{OH}	10		10		15		15		ns
Chip enable ($\overline{CE}_1$) to output in low-Z	t _{LZ1}	10		10		15		15		ns
Chip enable (CE ₂) to output in low-Z	t _{LZ2}	10		10		15		15		ns
Output enable to output in low-Z	t _{OLZ}	5		5		5		5		ns
Chip enable ($\overline{CE}_1$) to output in high-Z	t _{HZ1}		35		40		50		100	ns
Chip enable (CE ₂) to output in high-Z	t _{HZ2}		35		40		50		100	ns
Output enable to output in high-Z	t _{OHZ}		35		40		50		80	ns
Write Cycle										
Write cycle time	t _{WC}	100		120		150		200		ns
Chip enable ($\overline{CE}_1$) to end of write	t _{CW1}	80		85		100		180		ns
Chip enable (CE ₂) to end of write	t _{CW2}	80		85		100		180		ns
Address valid to end of write	t _{AW}	80		85		100		180		ns
Address setup time	t _{AS}	0		0		0		0		ns
Write pulse width	t _{WP}	60		70		90		140		ns
Write recovery time	t _{WR}	5		5		5		5		ns
Data valid to end of write	t _{DW}	40		50		60		80		ns
Data hold time	t _{DH}	0		0		0		0		ns
Write enable to output in high-Z	t _{WHZ}		35		40		50		100	ns
Output active from end of write	t _{OW}	5		5		10		10		ns

Notes:

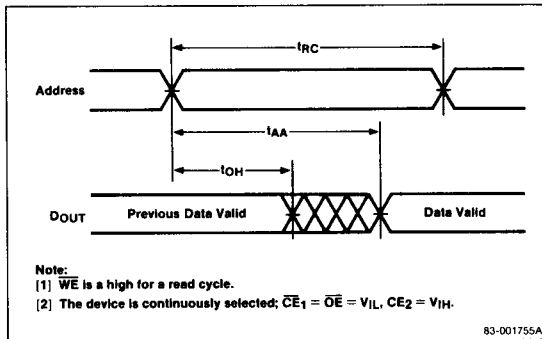
- (1) Input pulse levels: 0.8 to 2.4 V
Input pulse rise and fall times: 5 ns
Timing reference levels: 1.5 V
Output load: 1 TTL gate and C_L = 100 pF

Truth Table

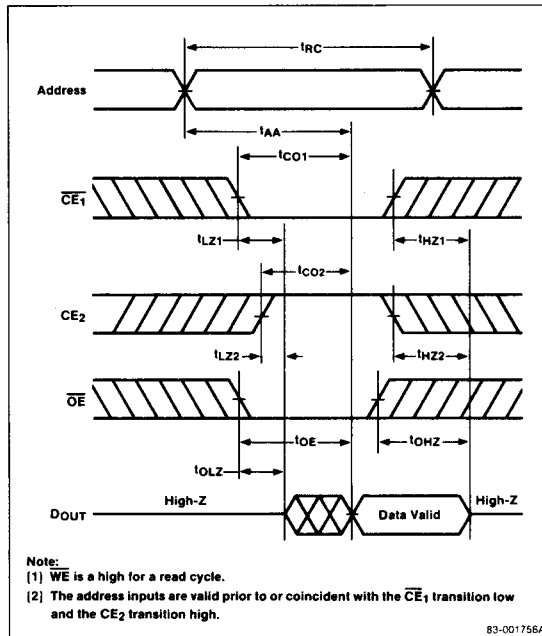
CE ₁	CE ₂	OE	WE	Mode	I/O	I _{CC}
H	X	X	X	Not selected	High-Z	Standby
X	L	X	X	Not selected	High-Z	Standby
L	H	H	H	D _{OUT} disable	High-Z	Active
L	H	L	H	Read	D _{OUT}	Active
L	H	X	L	Write	D _{IN}	Active

Timing Waveforms

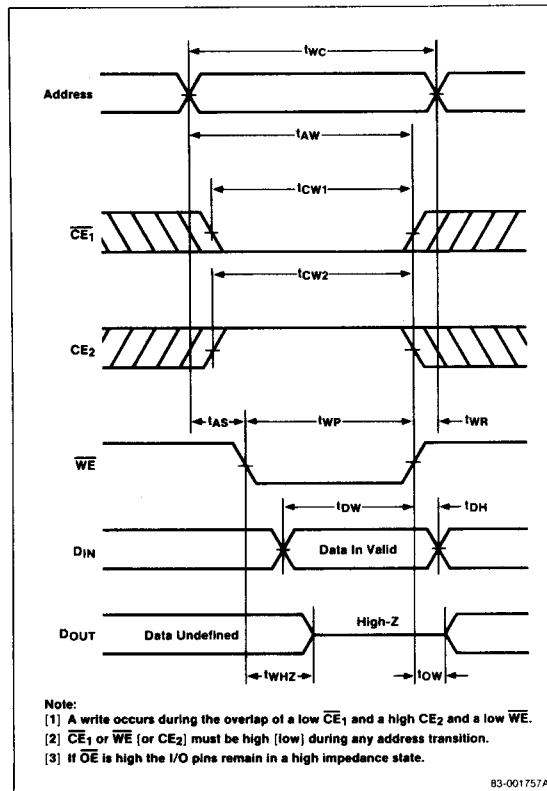
Read Cycle No. 1 (Address Access)



Read Cycle No. 2 (Chip Enable Access)

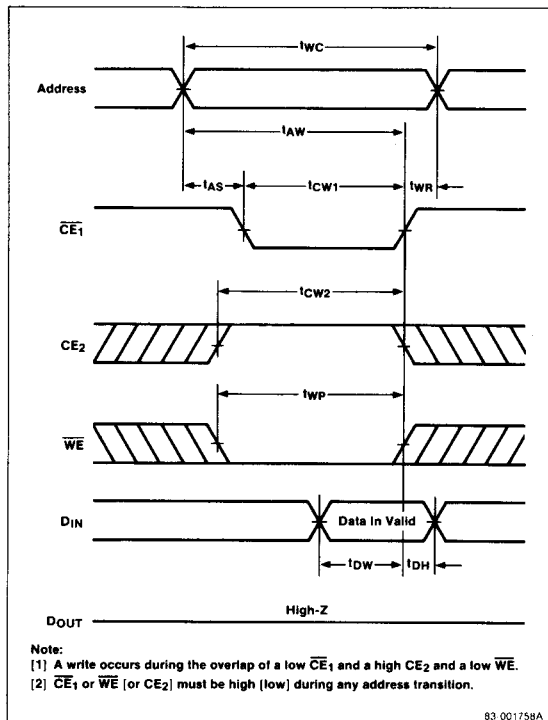


Write Cycle No. 1 ($\overline{WE}$ Controlled)

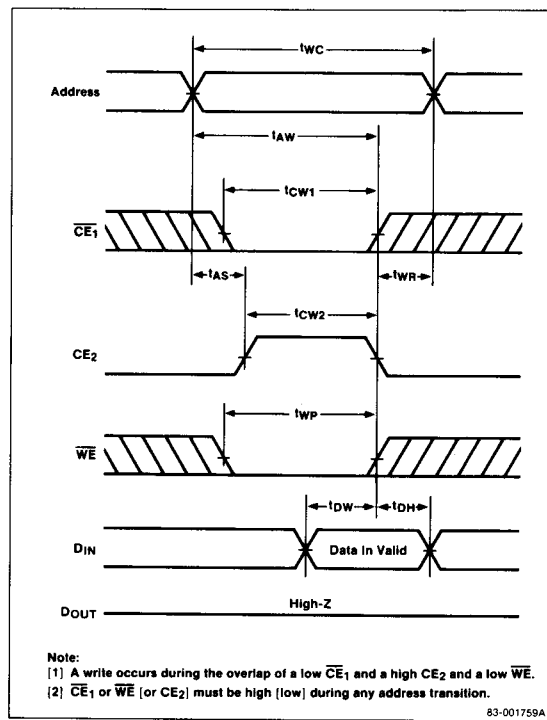


Timing Waveforms (cont)

Write Cycle No. 2 ($\overline{CE}_1$ Controlled)



Write Cycle No. 3 ($\overline{CE}_2$ Controlled)



Low V_{CC} Data Retention Characteristics

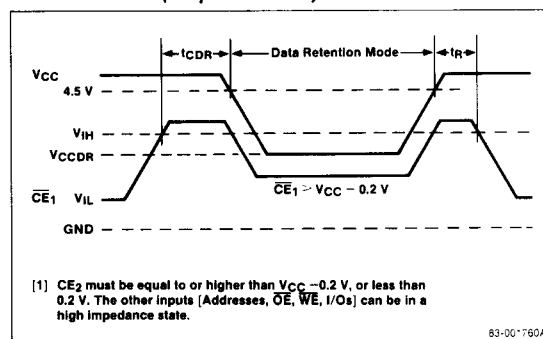
T_A = 0 to +70°C

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Data retention supply voltage	V _{CCDR1}	2.0		5.5	V	$\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ $CE_2 \geq V_{CC} - 0.2 \text{ V}$
	V _{CCDR2}	2.0		5.5	V	$CE_2 \leq 0.2 \text{ V}$
Data retention supply current	I _{CCDR1}		1	(2)	μA	V _{CC} = 3.0 V $\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ $CE_2 \geq V_{CC} - 0.2 \text{ V}$
	I _{CCDR2}		1	(2)	μA	V _{CC} = 3.0 V $CE_2 \leq 0.2 \text{ V}$
Chip deselect to data retention time	t _{CDR}	0			ns	
Operation recovery time	t _R		t _{RC}		ns	Note 3

Notes:

- (1) This table is applicable to μPD4364-xxL and -xxLL only.
- (2) μPD4364-xxL: 50 μA max; 15 μA (0 to 40°C)
μPD4364-xxLL: 20 μA max; 5 μA (0 to 40°C)
- (3) t_{RC} is read cycle time.

Data Retention ($\overline{CE}_1$ Controlled)



Data Retention (CE₂ Controlled)

