NEC
ELECTRON DEVICE

MOS INTEGRATED CIRCUIT

μPD71054

PROGRAMMABLE TIMER/COUNTER

The μPD71054 is a high-performance programmable timer/counter designed for timing control applications in microcomputer systems. The μPD71054 is fabricated by CMOS technology in order to realize low power consumption.

The μPD71054-10 is the latest and the fastest version, which can be directly configured with top-of-line processors such as the μPD70108-10 and the μPD70116-10.

FEATURES

- Compatible with μPD70108 (V20™), μPD70116 (V30™), μPD70208 (V40™), & μPD70216 (V50™)
- Three independently-operated 16-bit counters
- Six count modes available for each counter
- Binary/BDC count operation
- Multiple latch command for easy monitoring
- Count rate: 0 (DC) to 8 MHz; μPD71054
  0 (DC) to 10 MHz; μPD71054-10
- CMOS
- +5 V single power supply

ORDERING INFORMATION

Ordering Code	Package	Speed
μPD71054C	24-pin plastic DIP (600 mil)	8 MHz
μPD71054C-10	24-pin plastic DIP (600 mil)	10 MHz
μPD71054G	44-pin plastic QFP (1.45 mm thick)	8 MHz
μPD71054GB-3B4	44-pin plastic QFP (2.70 mm thick)	8 MHz
μPD71054GB-10-3B4	44-pin plastic QFP (2.70 mm thick)	10 MHz
μPD71054L	28-pin PLCC	8 MHz
μPD71054L-10	28-pin PLCC	10 MHz

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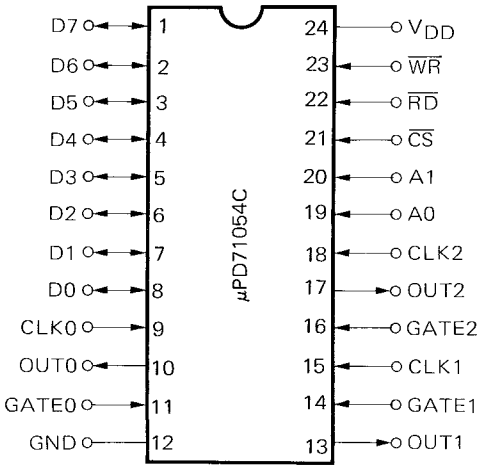
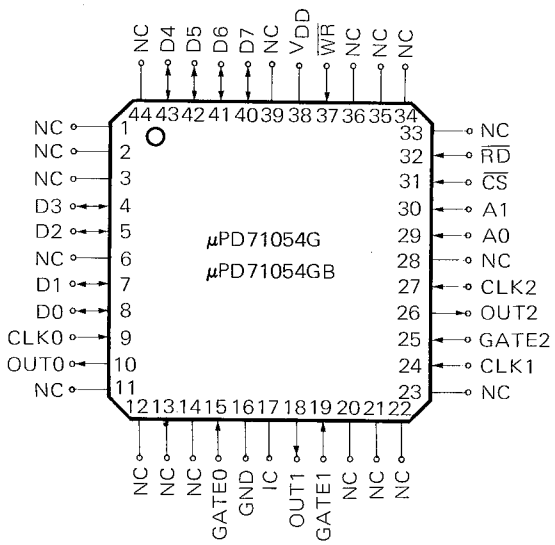
PIN CONFIGURATION (Top View)

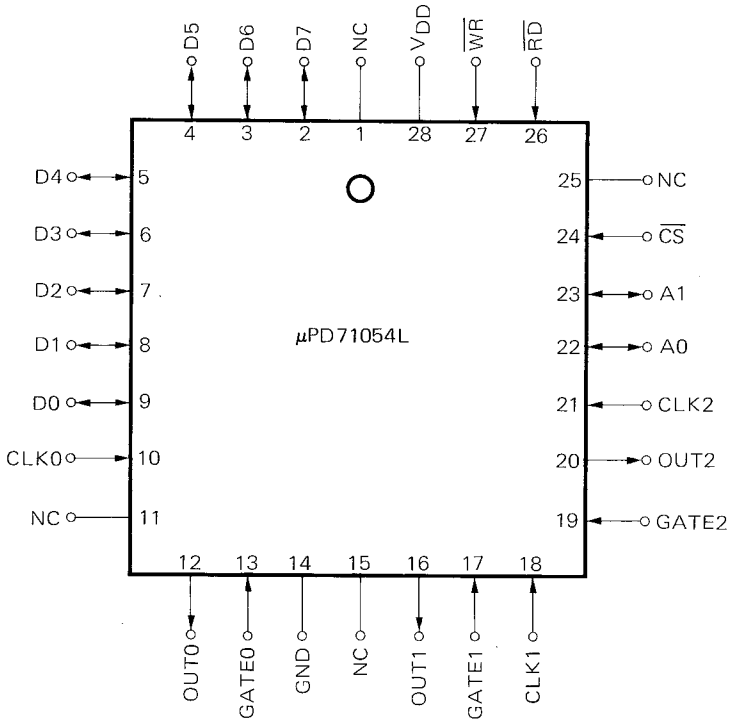
24-pin plastic DIP



44-pin plastic QFP



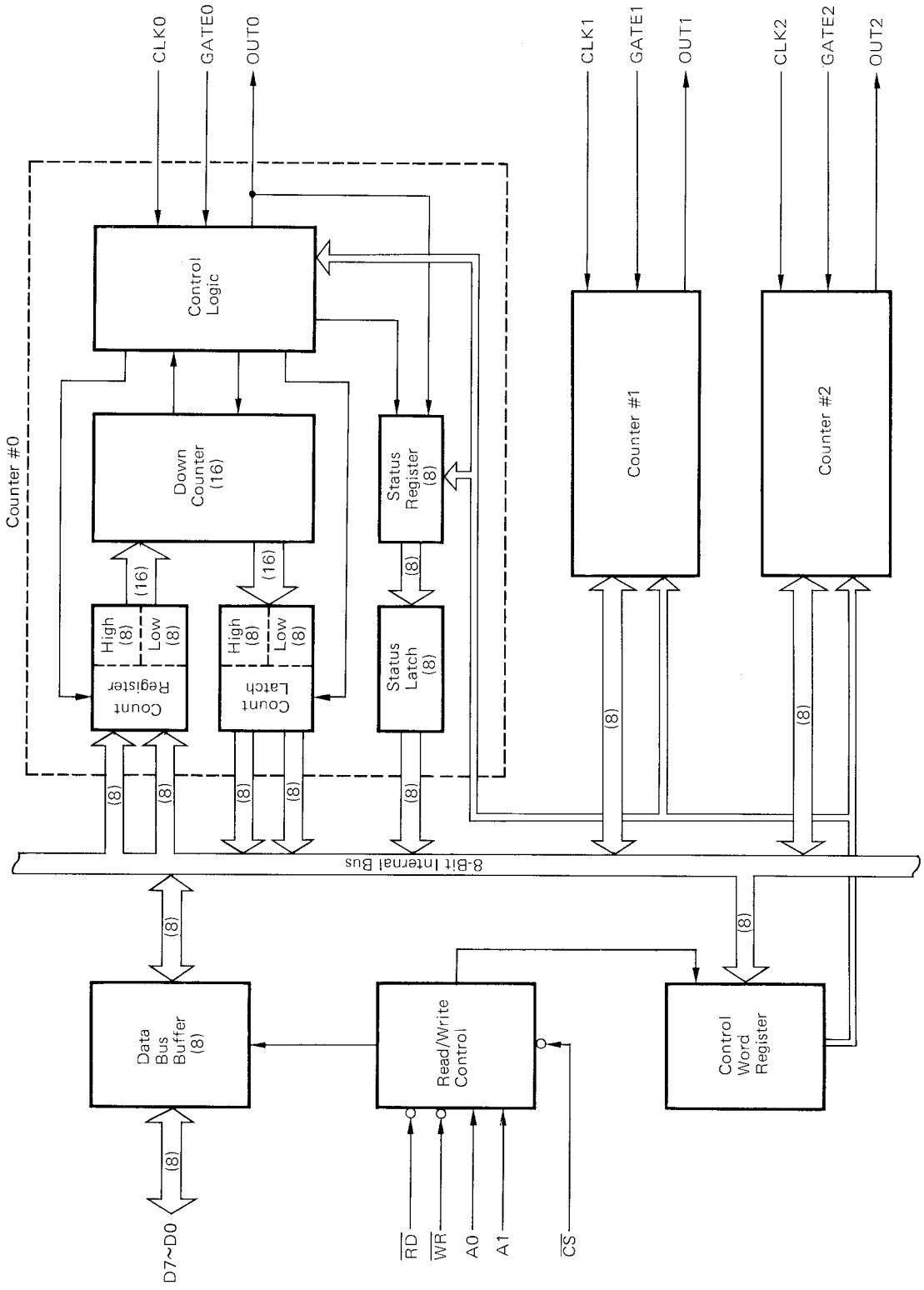
28-pin PLCC



PIN IDENTIFICATION

D7 to D0	:	Data Bus (8 bits)
CLKn	:	Counter Clock Input
OUTn	:	Counter Output
GATEn	:	Counter Gate Input
A1, A0	:	Address
$\overline{CS}$	:	Chip Select
$\overline{RD}$	:	Read Strobe
$\overline{WR}$	:	Write Strobe
V_{DD}	:	Power
GND	:	Ground

BLOCK DIAGRAM



NOTE:

The internal architecture of counters #1 and #2 is the same as counter #0's.

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1. PIN FUNCTIONS

1.1 D7 to D0 (Data Bus) - Three-state Input/Output

These pins form an 8-bit, three-state, bidirectional data bus. They are connected to the system data bus and are used for data communication. These pins become active when $\overline{CS}$=0 and $\overline{RD}$ or $\overline{WR}$=0, otherwise they enter high impedance.

1.2 CLKn (Counter Clock; n=0 to 2) - Input

These pins are the clock input that determines the count rate for counter #n. The clock rate is selected in the range of 0 (DC) to 10 MHz (μPD71054-10).

1.3 OUTn (Counter Output, n=0 to 2) - Output

These pins are the output for counter #n. A wide variety of outputs is available according to the count mode of the counter. When the μPD71054 is used as an interrupt source, these pins function to output an interrupt request signal.

1.4 GATEn (Counter Gate; n=0 to 2) - Output

These output pins are used to control the operation (operation inhibit or initialize) of counter #n according to the mode setting.

1.5 A1, A0, (Address) - Input

The states of A1A0 (i.e., 00, 01, or 10) select counter #0, #1, or #2, respectively. When A1A0=11, the control word register is selected. These pins are normally connected to the system address bus.

1.6 $\overline{CS}$ (Chip Select) - Input

When $\overline{CS}$=1, the read/write control disables both $\overline{RD}$ and $\overline{WR}$ lines, and as a result, all bits of the data bus (D7 to D0) become high impedance. $\overline{CS}$ must therefore be brought down to 0 when accessing the μPD71054.

1.7 $\overline{RD}$ (Read Strobe) - Input

When a read operation is to be performed on the μPD71054,the signal input to this pin should be logic 0.

1.8 $\overline{WR}$ (Write Strobe) - Input

When data are to be written to the μPD71054, the signal input to this pin should be set to 0. The contents of the data bus are then transferred to the μPD71054 on the rising edge (from 0 to 1) of the $\overline{WR}$ signal.

1.9 V_{DD} (Power)

This pin is connected to a positive power supply.

1.10 GND (Ground)

This pin is connected to a 0 V potential.

1.11 IC (Internally Connected)

This pin must be left unconnected.

2. BLOCK FUNCTIONS

The functions of each block of the μPD71054 are explained below.

2.1 Data Bus Buffer

This is an 8-bit, three-state, bidirectional buffer that acts as an interface between the μPD71054 and the system data bus. Data communications are performed via this buffer when the CPU executes IN or OUT commands for the μPD71054.

The data bus buffer handles these four kinds of data:

(1) Control words
(2) Count to be written to the count register
(3) Count data read from the count latch
(4) Status data read from the status latch

2.2 Read/Write Control

The read/write control circuit decodes data input from the system bus and sends control signals to other blocks of the μPD71054.

A1 and A0 are used to select one of the three counters or the control word register, and a low signal on $\overline{RD}$ or $\overline{WR}$ respectively specifies a read or write operation. These operations are enabled only when $\overline{CS}$=0.

2.3 Control Word Register

This is an 8-bit register into which the control words are written to determine the operation mode of the counter.

Data writing to this register is performed by executing an OUT command when A1A0=11. Even if an IN command is executed when A1A0=11, the contents of the control word register cannot be read. A multiple latch command, however, is provided to enable reading the operation mode and status data of each register.

2.4 Counter #n (n=0 to 2)

The μPD71054 consists of three count units capable of binary or BCD operation. Six programmable count modes and three read/write modes are available. These count units (counter #0, counter #1, and counter #2) operate independently and can each be set to a different mode. To perform read/write operations to a counter, address lines A1 and A0 should be used to select the counter. Figure 2-1 shows the internal blocks of the counter.

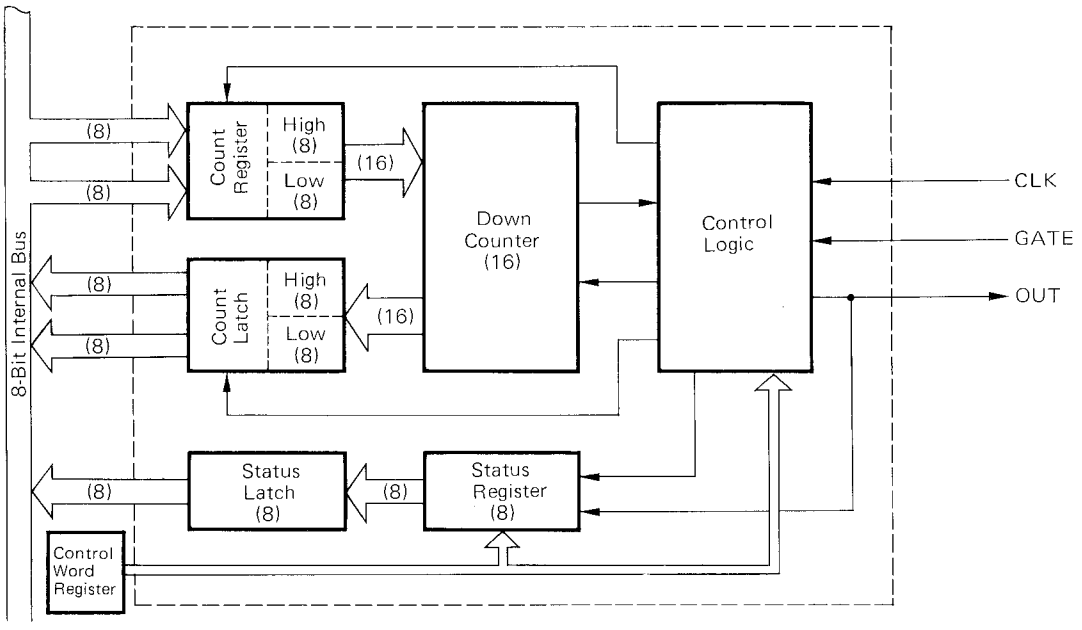


Fig. 2-1 Internal Counter Blocks

The actual count operation within each counter is performed by a 16-bit synchronous down counter. This counter can be preset and selected for either binary or BCD operation.

The count register is a 16-bit register that stores the count. When the count is written to the counter, it is first stored in this register. The count is then transferred to the down counter and a count operation for the specified number of counts begins. When the count is written to the count register, the 8-bit data width of the internal data bus permits transfer of only 8 bits at a time. When the stored data are written from the count register to the down counter, however, all 16 bits can be sent at the same time. When the counts is written to the count register while the counter is set in the read/write 1 byte mode, data 00H is automatically written to the remaining byte of the register.

The count latch normally holds the current value of the down counter. If the contents of the down counter change, the contents of the count latch will also change so that the two values will be identical. In other words, the count latch traces the down counter. When the μPD71054 receives a count latch command, the count latch latches the value of the down counter and holds it until the CPU reads it. Then, when this data has been read, the count latch returns to trace the operation of the down counter.

When mode specification is performed for the counter, the lower 6 bits of the current control word register are copied to the lower 6 bits of the 8-bit status register. The remaining 2 higher bits will show the status of the OUT pin and the count invalid flag.

When the multiple latch command is executed to latch the status of the counter, the current value of the status register will be latched in the status latch. This data is then held in the latch until the CPU reads it.

The control logic controls each internal block based on the currently set mode and the state of the externally connected CLK and GATE pins. The result is output to the OUT pin.

3. SYSTEM CONFIGURATION EXAMPLE

Seen from the CPU, counters #0, #1, #2, and the control word register are regarded as four I/O ports.

The counter and command selection pins A1, A0 are normally connected to the A1, A0 lines of the system address bus. The $\overline{CS}$ signal is generated by decoding the address and IO/$\overline{MEM}$ signals so that it will go low when the address bus is set to the target I/O address, thus the I/O is selected.

The μPD71054 can also be used with memory mapped I/O configurations which is different from the one described here. When this is done, the configuration should be such that the $\overline{CS}$ signal will go low when memory is selected.

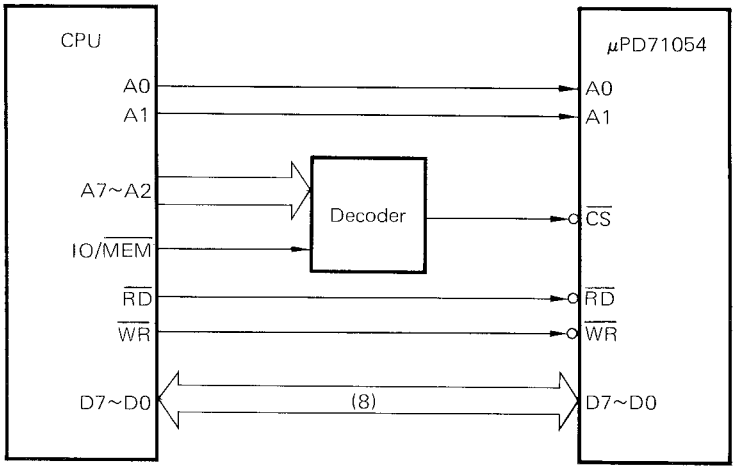


Fig. 3-1 System Configuration Example

4. COUNTER PROGRAMMING & COUNTER READ

When power is applied to the μPD71054, the condition of the internal data is undefined. Before the μPD71054 can be used, the target counter must be programmed and its operation mode specified. Once a mode has been selected for a counter, it will operate in that mode until another mode is set for it. The count is written to the counter and when that data is transferred to the down counter, a new count operation begins. During the count operation, the current count data as well as the current status data (showing the condition of the counter) can be read.

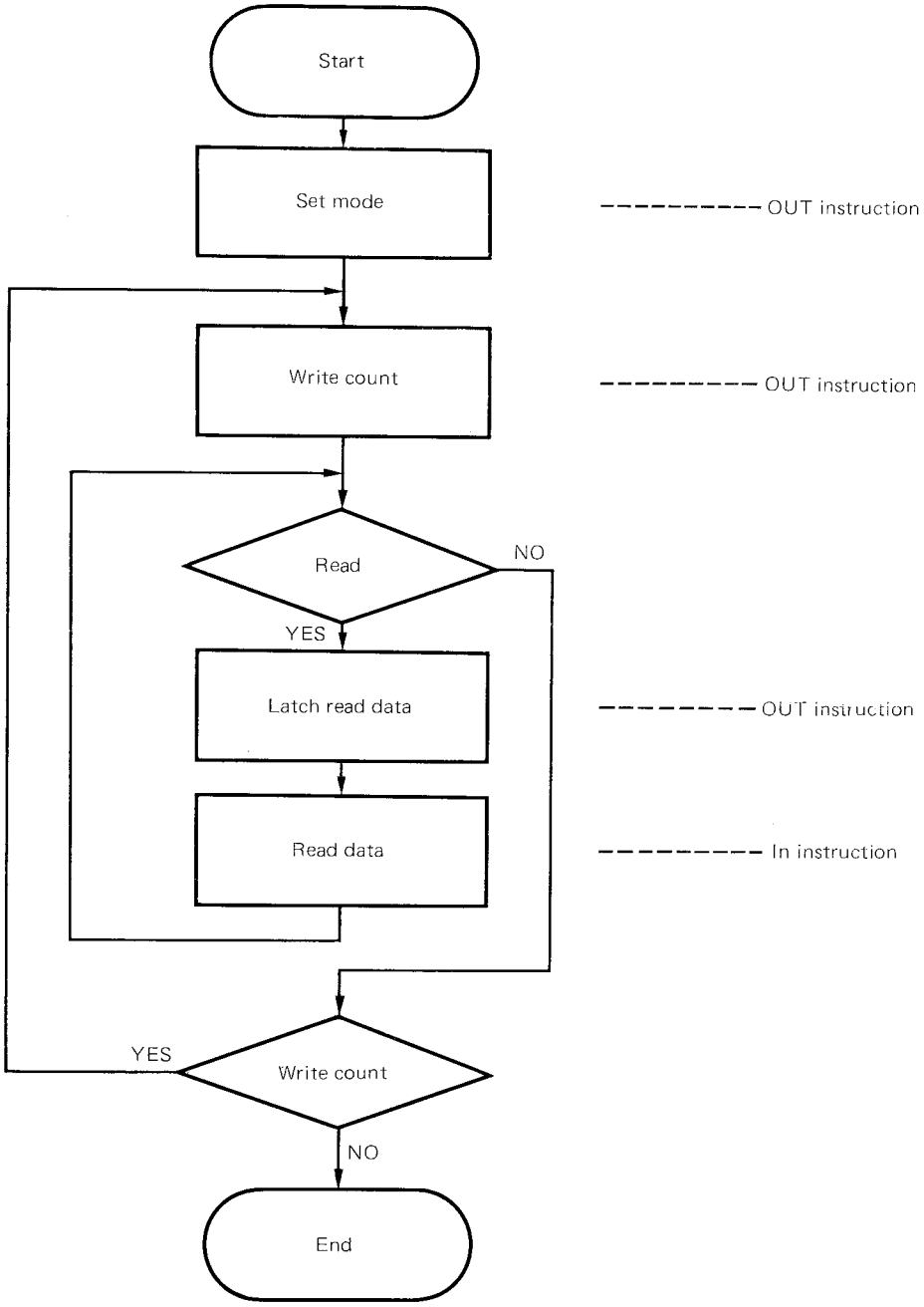


Fig. 4-1 Basic Operating Procedure

4.1 Programming a Counter

The μPD71054 is designed for timing control by the program of a microcomputer system. To operate a counter, the program must do two things: it must first write a control word to set the operation and it must write a count data that determines the duration of the count operation to be performed.

Table 4-1 Write Operations to the μPD71054

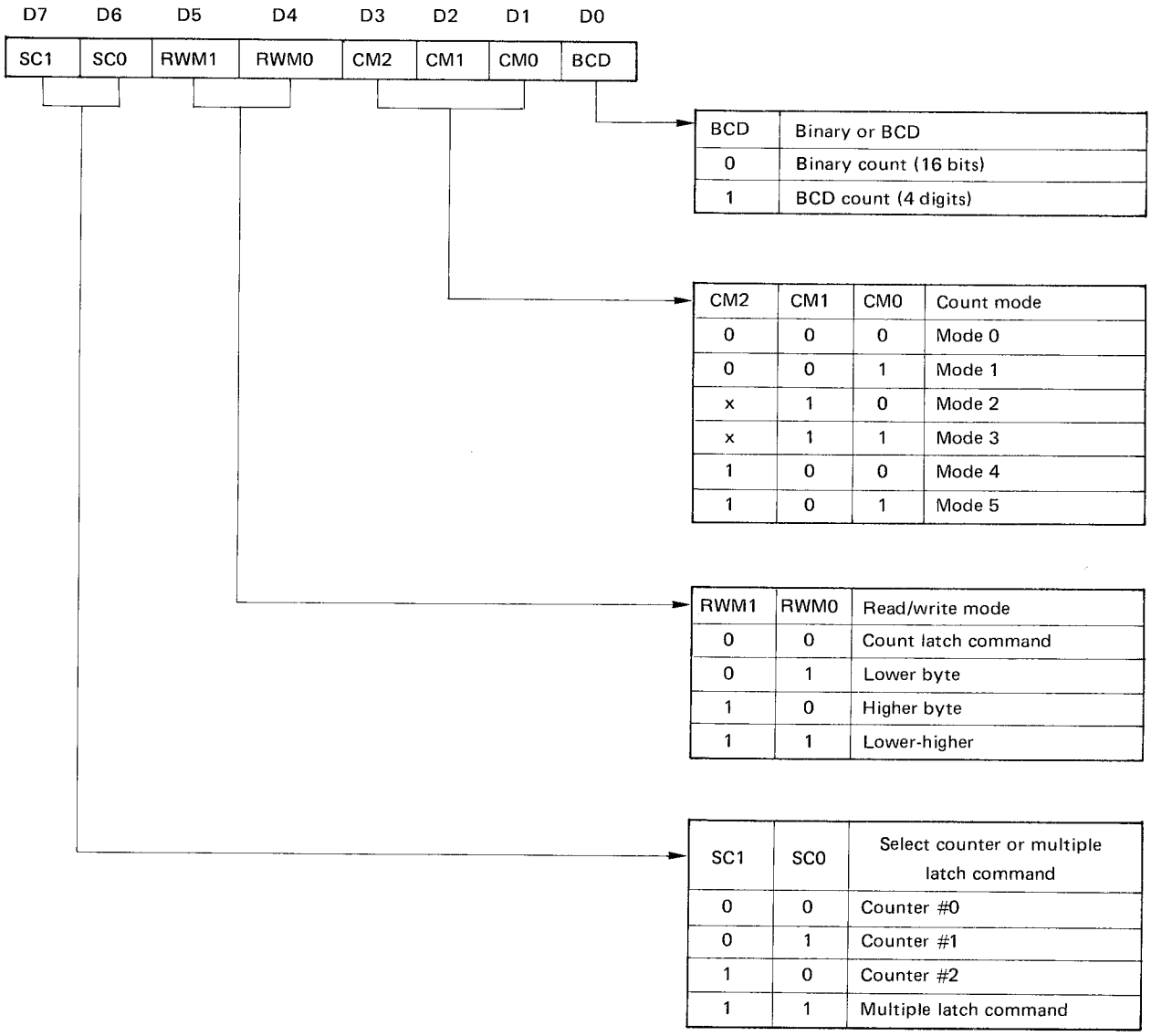
($\overline{CS}$=0, $\overline{RD}$=1)

$\overline{WR}$	A1	A0	Write target
0	0	0	Counter #0
0	0	1	Counter #1
0	1	0	Counter #2
0	1	1	Control word register

(1) Control word and mode setting

To operate a counter, first a control word must be written and the operation mode of the counter is set. If a write operation is performed when A1A0=11, a control word is written to the control word register.

The control word is an 8-bit word that can be broken into four blocks:



BCD	Binary or BCD
0	Binary count (16 bits)
1	BCD count (4 digits)

CM2	CM1	CM0	Count mode
0	0	0	Mode 0
0	0	1	Mode 1
x	1	0	Mode 2
x	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RWM1	RWM0	Read/write mode
0	0	Count latch command
0	1	Lower byte
1	0	Higher byte
1	1	Lower-higher

SC1	SC0	Select counter or multiple latch command
0	0	Counter #0
0	1	Counter #1
1	0	Counter #2
1	1	Multiple latch command

x: don't care

Fig. 4-2 Control Word Format

(i) SC1[D7] to SC0[D6] (Select counter or multiple latch command)

This block specifies one of three counters #0, #1, and #2, or the multiple latch command. When a counter has been specified, the specification of each field described in (b) through (d) below applies to the selected counter. For details of the multiple latch command, see "Reading the Counter".

(ii) RWM1[D5] to RWM0[D4] (Read/write mode)

This block specifies the mode of the read/write operation to the counter (low/high 2-byte, low 1-byte, or high 1-byte). This field can also be used to select the count latch command.

Even in the 1-byte mode, the counter operates as a 2-byte unit.

(iii) CM2[D3] to CM0[D1] (Count mode)

This block is used to set the count mode (0 to 5).

(iv) BCD[D0] (Binary or BCD)

This bit selects between binary and BCD count operations. The permissible range of values for the count data is 0 to FFFFH for binary count and 0 to 9999 for BCD count.

When a control word is written to the counter, in order to the mode, that is, if it is other than the multiple latch command or the counter latch command, the lower 6 bits of the control word (mode data) are copied to the lower 6 bits of the status register of the specific counter selected by SC1 and SC0. The newly-set mode remains in effect until a new mode is set for that counter.

(2) Writing the count

After the mode has been set, the count is written to the counter. A1A0 should be conditioned to specify the target counter and the desired count is written to the counter. A new count can be written to a counter at any time. When writing the count, caution must be taken on the byte-wise read/write mode selected. In higher 1-byte and lower 1-byte mode, the higher or lower byte of the count register is written by the first write operation, after which the write operation completes. Then, data 00H is automatically written to the remaining higher or lower byte. In the lower-higher 2-byte mode, the lower byte is written by the first write operation and the higher byte by the second. For example, if 2-byte data 8801H is inadvertently written to a counter that is currently set in the lower 1-byte mode, the lower byte (01H) will be written followed by the higher byte (88H). The data written to the count register will therefore be 0001H for the first write and 0088H for the second.

Table 4-2 Read/Write Mode and Count Write

Read/write mode	No. of writes	Count register	
		Higher byte	Lower byte
Lower 1-byte	1	00H	xxH
Higher 1-byte	1	xxH	00H
Lower-higher 2-byte	2	xxH (2nd write)	xxH (1st write)

xx: Two-digit hexadecimal value

4.2 Reading a Counter

The μPD71054 is provided with functions that allow the contents of the down counter to be read while the counter continues to operates without affecting the operation. The three methods described below are available to read the contents of the counter. The multiple latch command, in particular, provides added flexibility because it reads not only the current count data but also the counter mode or the state of the OUT pin.

Table 4-3 Read Operations from the μPD71054

($\overline{CS}$=0, $\overline{WR}$=1)

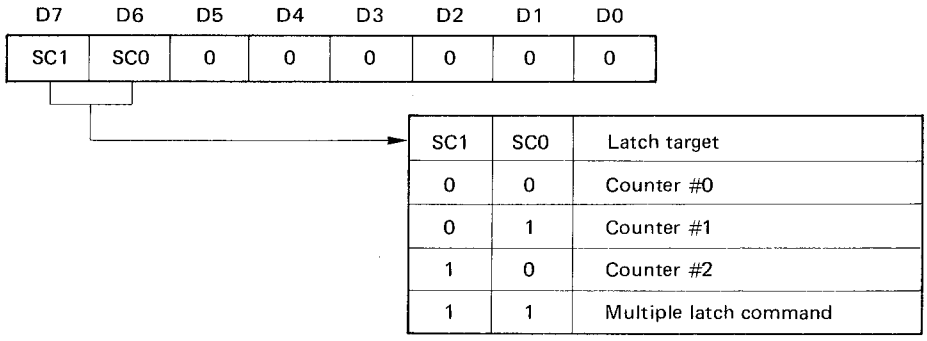
$\overline{RD}$	A1	A0	Read target
0	0	0	Counter #0
0	0	1	Counter #1
0	1	0	Counter #2

(1) Direct read of count data

By reading the counter selected by A1A0, the current value of the count data is obtained. However, since it is, the count latch (which traces the value of the down counter) being read, and the value of the down counter may change while the count latch is being read, this method may not provide an accurate reading. For correct reading, it is highly recommended to control the CLK or GATE input of the counter to stop the count operation and then read the counter.

(2) Count latch command

When the count latch command is executed, the contents of the counter selected by bits SC1 and SC0 of the control word (in other words, the current count data) are latched by the counter latch. Because this data is held by the latch until it is read or until a new mode is set, an accurate reading of the count data at the time of command execution is obtained without stopping or affecting the operation of the counter in any way.



SC1	SC0	Latch target
0	0	Counter #0
0	1	Counter #1
1	0	Counter #2
1	1	Multiple latch command

Fig. 4-3 Control Word Format for Count Latch Command

If the data latched in the count latch by executing the count latch command is not read and before a second count latch command is written, the second command will be ignored. This is because the value latched by the first command is held until the data is read (or the counter mode is reset).

When the data in the count latch is read, the latch is released and returns to trace the value of the down counter.

(3) Multiple latch command

When the multiple latch command is executed, these data for the selected counter are latched: the count data, program status, output status, and the status of the result flags. Once latched, these data can then be read by the CPU. The format of this command is shown in Fig. 4-4.

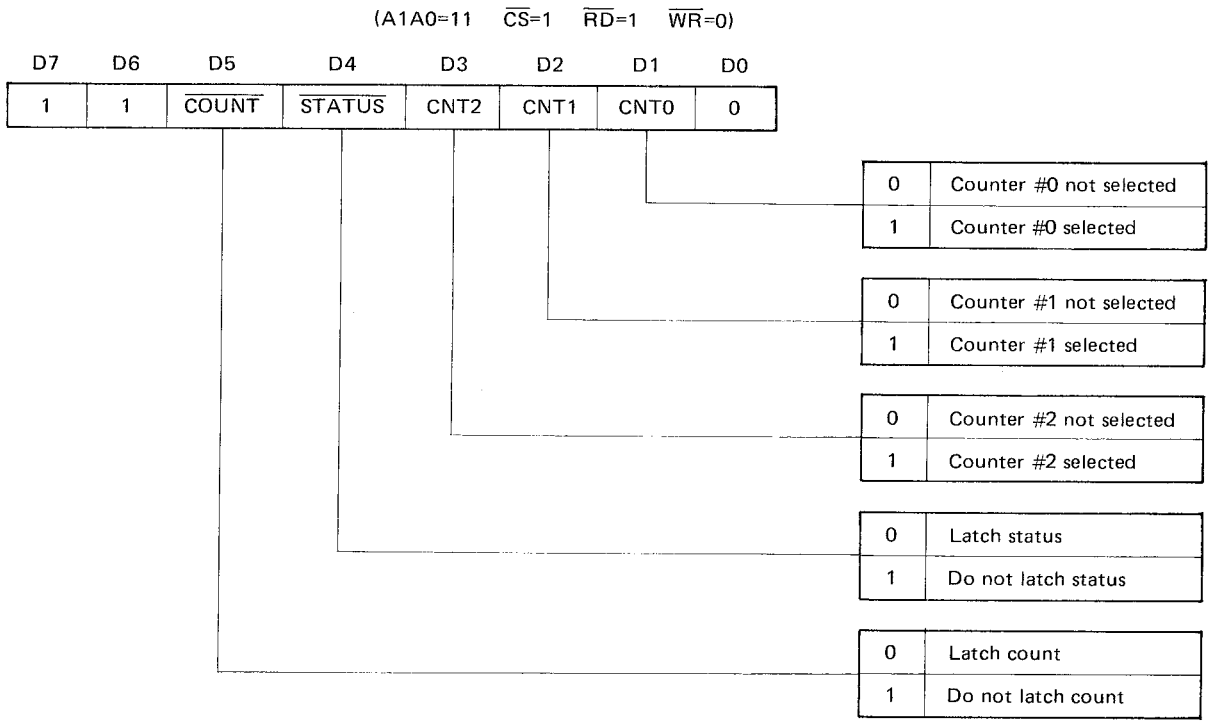


Fig. 4-4 Multiple Latch Command Format

Bits CNT2[D3] to CNT0[D1] correspond to counter #2 to counter #0. This command is effective for all counters whose corresponding bit is 1. In this way, the data for more than one counter can be latched by a single execution of the multiple latch command.

When the $\overline{\text{COUNT}}$ bit [D5] is 0, the count data of the selected counters are latched in the count latches. When the $\overline{\text{STATUS}}$ bit [D4] is 0, the status data (see Fig. 4-5) of the selected counters are latched in the status latches. Bits D5 to D0 of the status data show the mode status of the counter and the OUTPUT bit [D7] shows the state of the OUT pin of that counter. The Null Count (NC) Bit [D6] indicates whether or not the count data is valid. When the count is transferred from the count register to the down counter, this bit changes to 0 showing that the new data is valid (refer to Table 4-4).

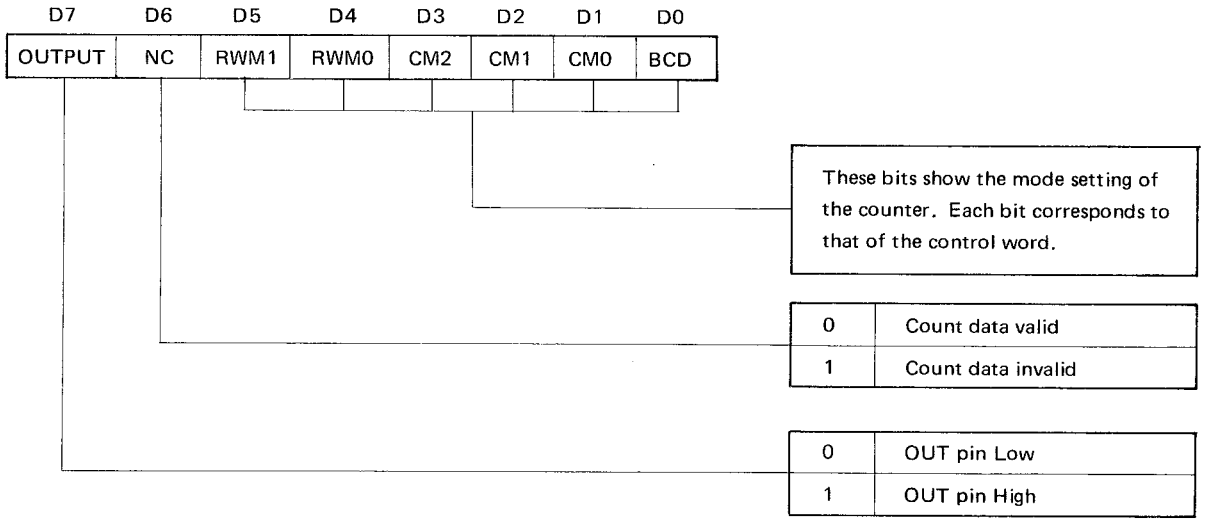


Fig. 4-5 Status Data

Table 4-4 NC Flag Operation

Operation	NC Flag
Write control word for mode set	1
Write count to count register*	1
Transfer count from count register to down counter	0

*: When the 2-byte mode is selected as the read/write mode, the flag becomes 1 when the second byte is written.

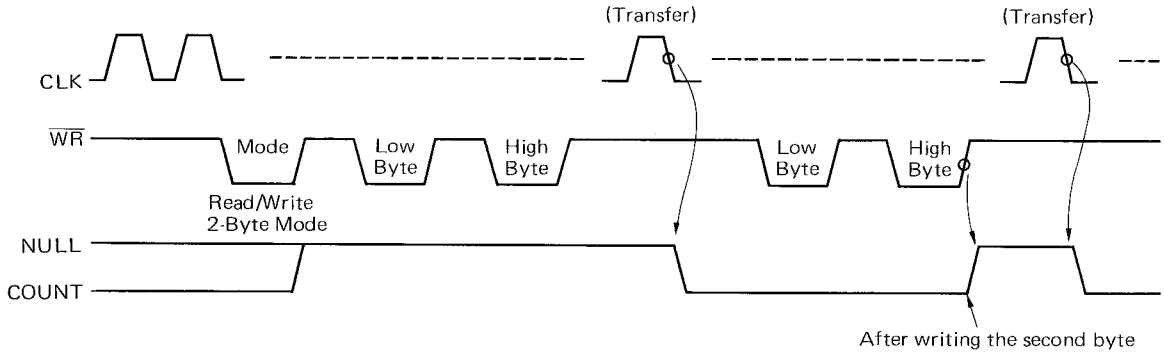


Fig. 4-6 Changing Example of the NC Flag

Because the count and status latched by the multiple latch command are held in the respective latchces until the contents of the latch are read, or until a new mode is set, execution of this command will be invalid (ignored) for the latch whose contents have not yet been read. Examples are shown in Fig. 4-7. Once the contents of the count or status latch are read, that particular latch is released.

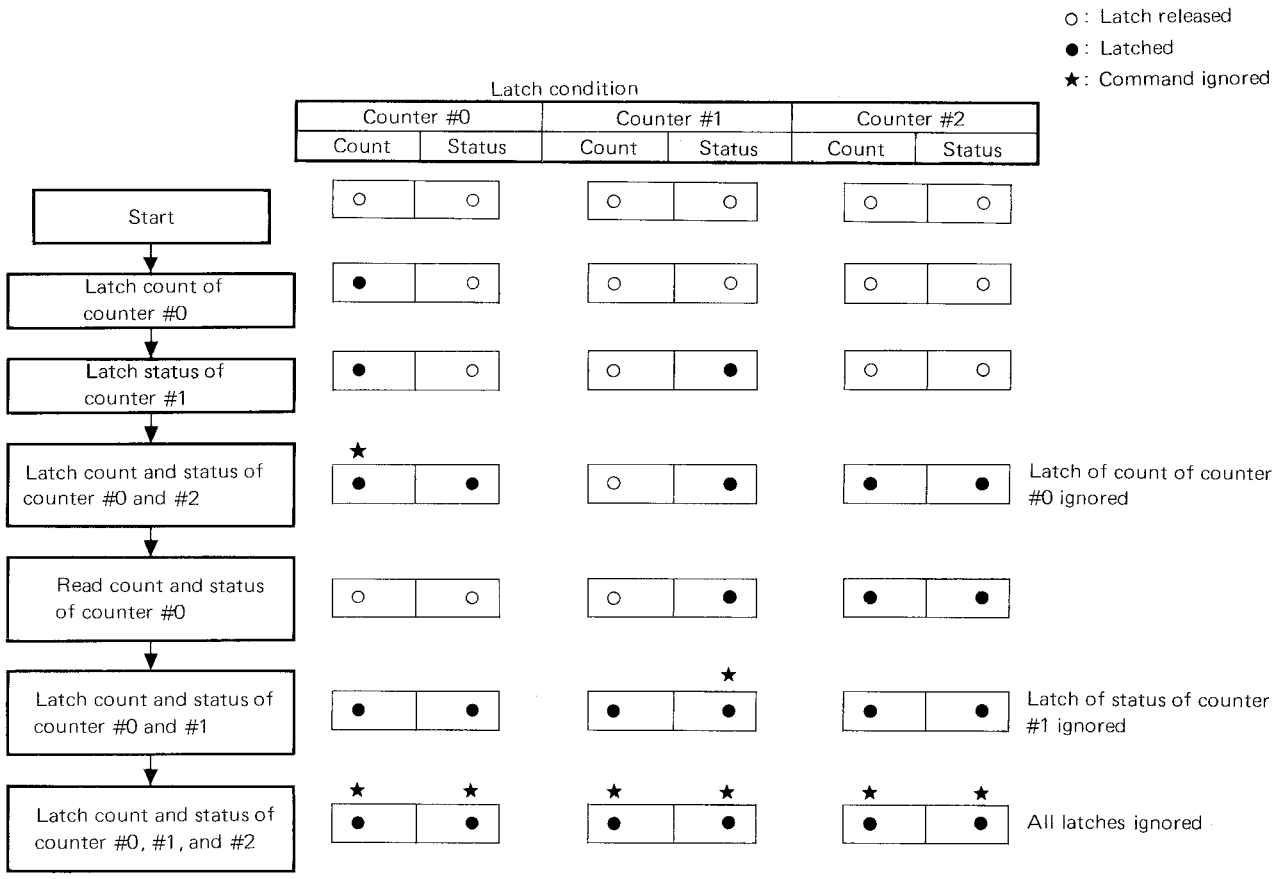


Fig. 4-7 Multiple Latch Command Execution Example

It is possible to latch both the count and status data. When doing this, however, attention must be paid to this point: whether the count or status data is latched first, the status data is always read first. The count data is read by the next read operation (of the one- or two-step read execution as determined by the read/write mode). If the read operation continues, the count data that has not been latched (the contents of the down counter being traced by the count latch) are read.

Read operations must also be performed in accordance with the read/write mode. In lower-higher 2-byte mode, 2 bytes of data must always be read. This does not mean, however, that the second byte must be read immediately after the first; other counter operations may be performed between the two reads. The following operations may be performed on a counter set in the 2-byte mode.

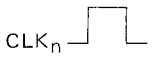
(1) Read lower byte
(2) Write new lower byte
(3) Read higher byte
(4) Write new higher byte

5. COUNT MODES

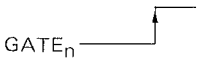
In this Chapter, the six count modes are explained with program examples given for each mode. The terms and concepts given below should be read and understood before reading this chapter.

CLK Pulse: From the rising edge to the falling edge of the CLK n input

Trigger: Rising edge of the GATE n input



CLK pulse



Trigger

GATE: The GATE n input is sampled at each rising edge of the CLK n input. When sampled, the signal sense can either be level sensitive or rising edge (trigger) sensitive. In the latter case, the internal trigger F/F of counter #n is set at the rising edge of the GATE signal, sensed at the rising edge of the next CLK n pulse, and then reset to enable the next operation.

Initial OUT: This is the state of the OUT pin immediately after the mode setting by a control word.

Count transfer: This is transfer of the count from the count register to the down counter.

Decrement: The operation of the down-counter, and is performed at the rising edge of the CLK pulse.

Count ZERO: This is the state when the contents of the down counter becomes 0 as a result of decrement.

PCNT0: I/O port for counter #0 (A1A0=00)

PCNT1: I/O port for counter #1 (A1A0=01)

PCNT2: I/O port for counter #2 (A1A0=10)

PCTRL: I/O port for the control word (A1A0=11)

CW: Control word

LB: Lower byte of the count

HB: Higher byte of the count

In the execution examples (timing charts) in every count mode, counter #0 is set in the read/ write 1 byte mode and binary count. When the GATE signal is omitted from the charts a constant high level signal is assumed. The value shown below the OUT signal is the count value; a question mark there indicates that the count value is undefined in case it is immediately after mode specification, otherwise it is the continuing count from previous one.

The maximum count (10000H for binary count and 10000 for BCD count) is available when 0 is set for the count register of counter.

5.1 Mode 0: Interrupt at the End of Count

In this mode, the OUT output changes from low to high level when the end of the specified count is reached.

Table 5-1 Mode 0 Operation

Initial OUT		Low level
GATE input	High level	Count enable
	Low level	Count disable
Count write		The OUT pin becomes low level (independent of the CLK pulse). In 2-byte read/write mode, count is disabled when the first byte is written, and then the OUT pin becomes low level
Count transfer and operation		When the count is written when GATE is high level: Transfer is performed at the first CLK pulse after the count data is written. The decrement operation of the down counter begins from the first CLK pulse after data transfer. If a count of N is set, the signal at the OUT pin will become low level after N+1 CLK pulses. When the count is written when GATE is low level: Transfer is performed at the first CLK pulse after the count is written. Decrement begins from the first CLK pulse after the GATE signal becomes high level. If a count of N is set, OUT will be low level for a period of N CLKpulses.
Count ZERO		The signal at the OUT pin becomes high level. The count operation itself does not stop and counts down to FFFFH (binary)/9999 (BCD).
Minimum count		1

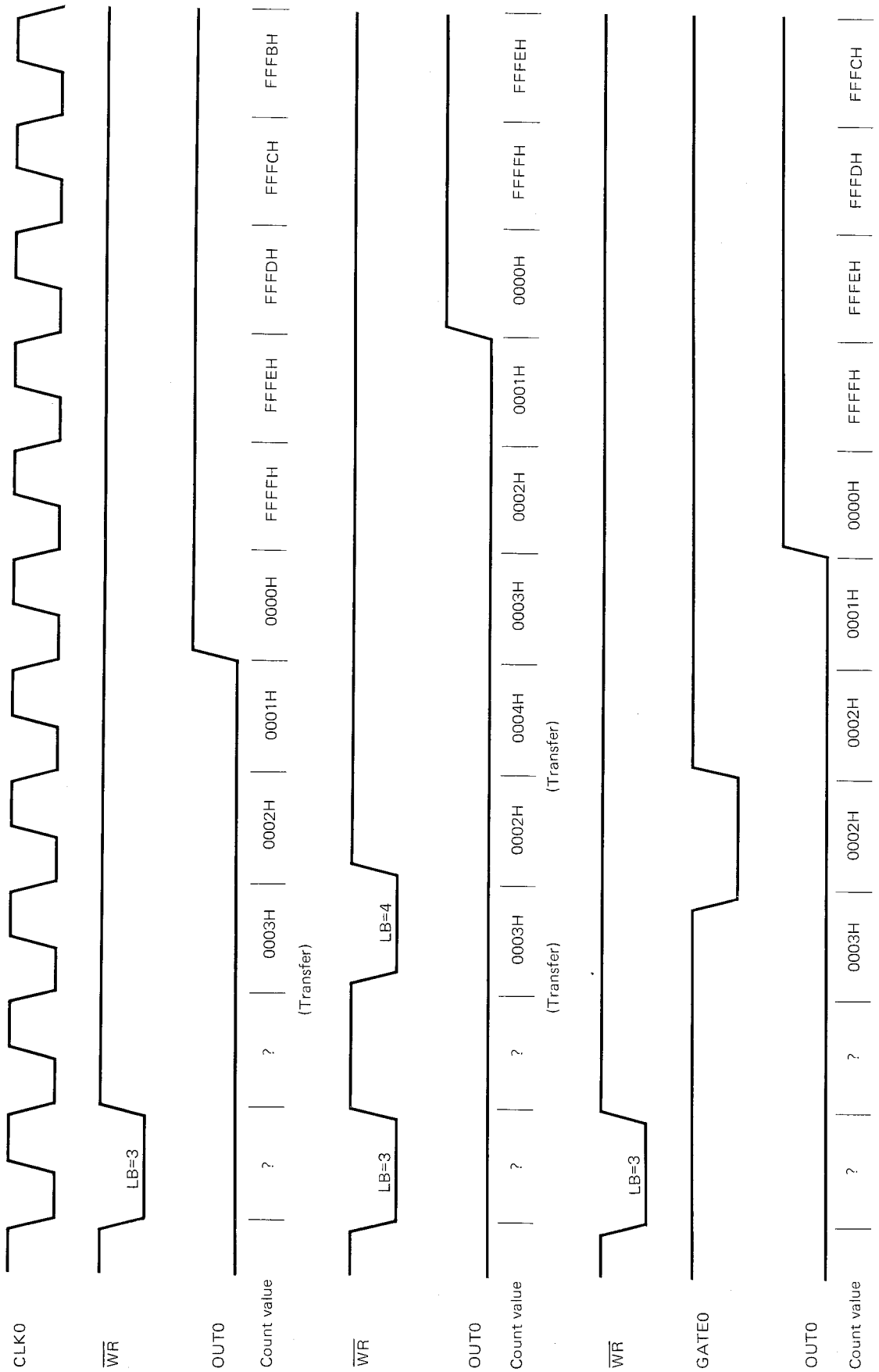


Fig. 5-1 Mode 0 Operation Example

Mode 0 Program Example

This is a subroutine for a delay of 10000 (2710H) CLK pulses. In this program, counter #2 is set to low/high 2-byte read/write mode and binary count.

```
SUBR0:  MOV   AL, 10110000B  }   Mode setting
        OUT   PCTRL, AL      }     ○ Counter #2
                                   ○ High/low 2-byte read/write mode
                                   ○ Count mode 0
                                   ○ Binary
        MOV   AL, 10H        }   Write count 10000
        OUT   PCNT2, AL      }
        MOV   AL, 27H        }
        OUT   PCNT2, AL      }
        RET
```

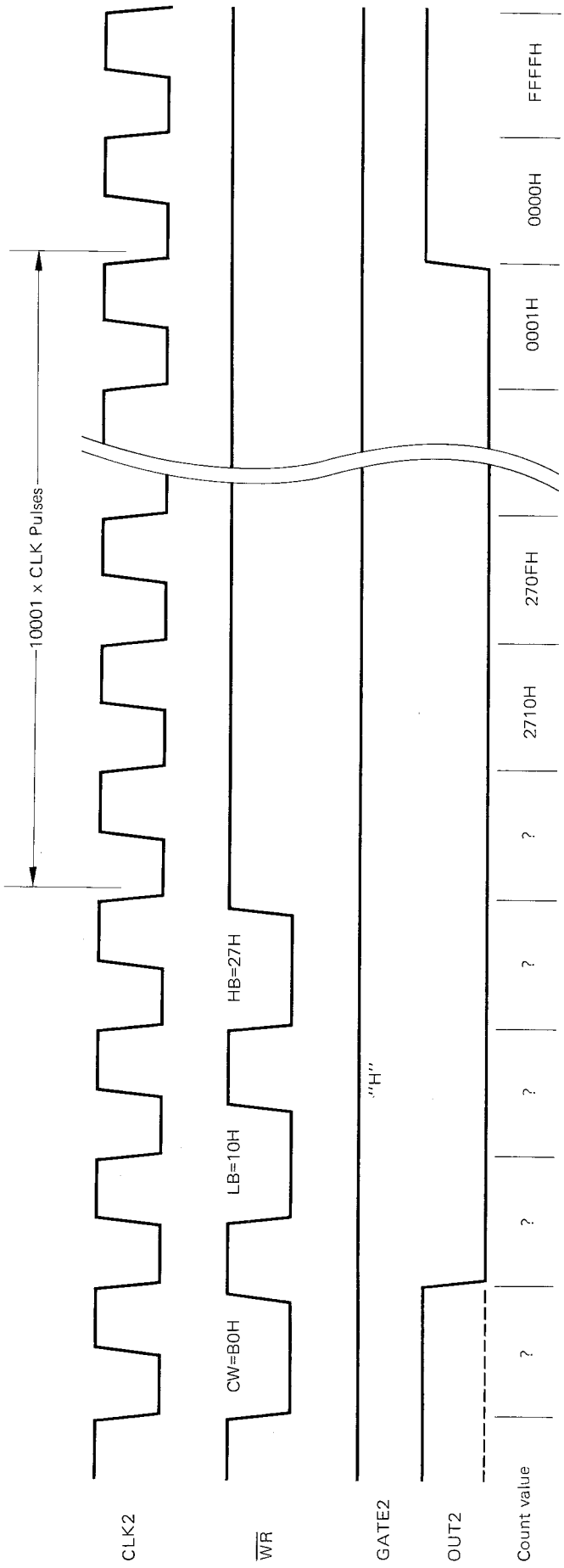


Fig. 5-2 Mode 0 Program Example Operation

5.2 Mode 1: GATE Retriggerable One-Shot

In this mode a low level one-shot pulse (triggered by the GATE input) is output from the OUT pin.

Table 5-2 Mode 1 operation

Initial OUT		High level
GATE	Trigger*	The count data is transferred at the first CLK pulse after the trigger.
Count write		Write count without affecting the current operation
Count transfer and operation		Transfer is performed at the first CLK pulse after the trigger. At the same time, the signal at the OUT pin becomes low level to start a one-shot pulse operation. The count is decremented from the next CLK pulse. If a count of N is set, the one-shot output from the OUT pin will continue for N CLK pulses.
Count ZERO		The signal at the OUT pin becomes high level. The count operation does not stop and counts down to FFFFH (binary)/9999 (BCD).
Minimum count		1

* The trigger is ignored when the count has not yet been written after the mode is set, or when only 1 byte of the count has been written in the 2-byte read/write mode.

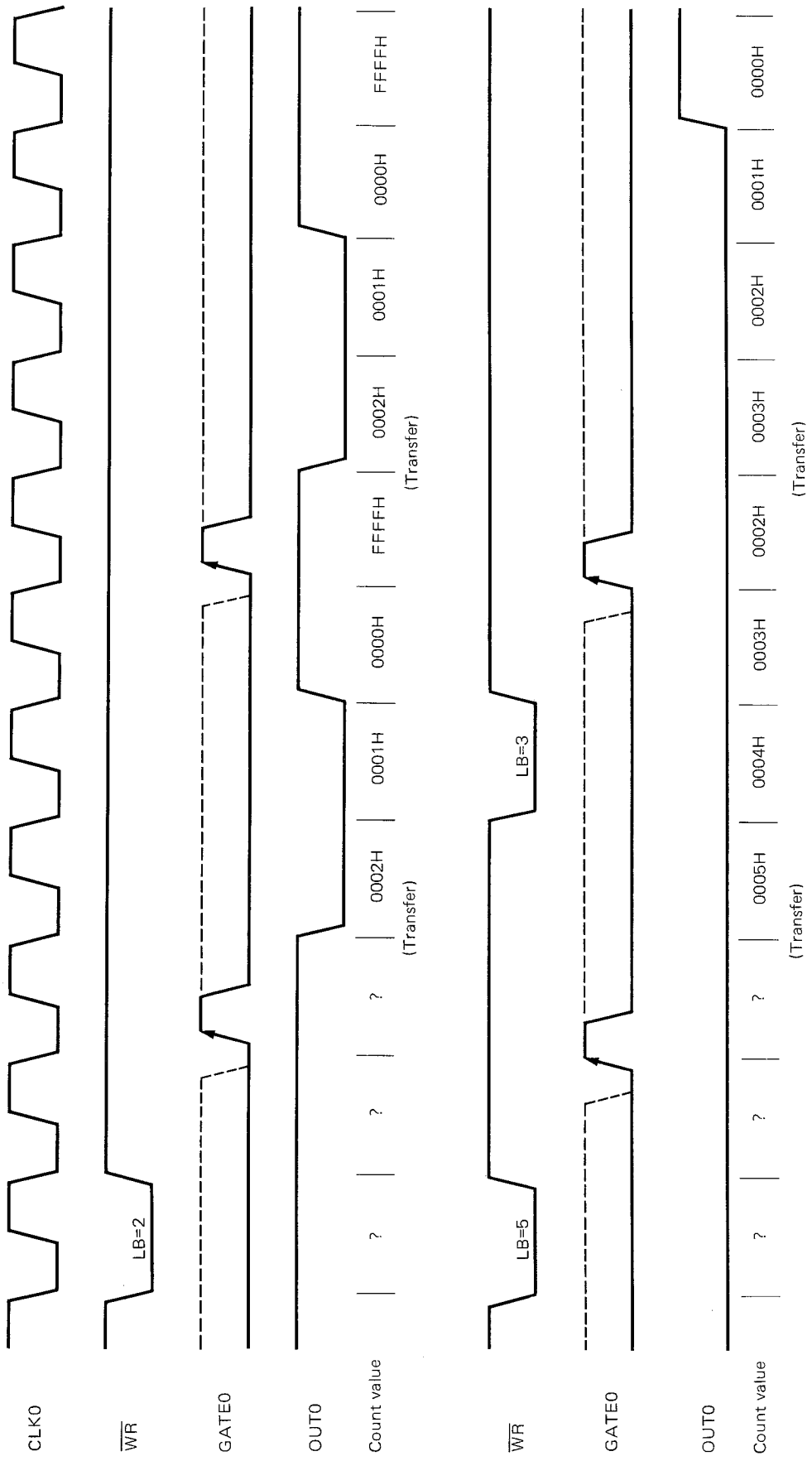
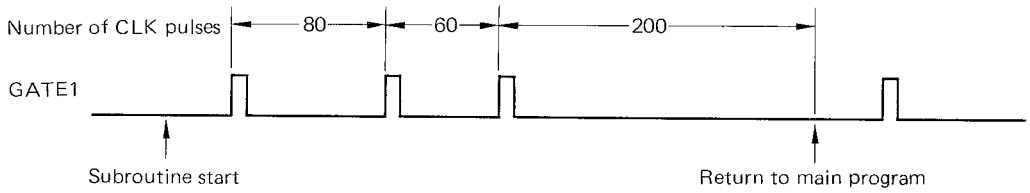


Fig. 5-3 Mode 1 Operation Example

Mode 1 Program Example

This is a subroutine that waits until no trigger is generated for an interval of 200 or more CLK pulses after the first GATE trigger, and then returns to the main program.

Counter #1 is set to the low byte read/write mode and binary count operation.




```
SUBR1:  MOV   AL, 01010010B   }
        OUT   PCTRL, AL       }

        MOV   AL, 200         }
        OUT   PCNT1, AL       }

FSTTRG: MOV   AL, 11100100B   }
        OUT   PCNT1, AL       }

        IN    AL, PCNT1       }
        TEST1 AL, 7           }

        BNZ   FSTTRG

WAIT:   MOV   AL, 11100100B   }
        OUT   PCTRL, AL       }

        IN    AL, PCNT1       }
        TEST1 AL, 7           }
        BZ    WAIT            }

        RET
```

Mode setting
- ○ Counter #1
- ○ Lower byte read/write mode
- ○ Count mode 1
- ○ Binary

Write low byte of count

Multiple latch command
- ○ Counter #1
- ○ Status

Wait for first trigger

Multiple latch command
- ○ Counter #1
- ○ Status

Wait until output becomes high level

5.3 Mode 2: Rate Generator

In this mode, the signal output from the OUT pin cyclically becomes low level during the last one CLK of the specified count. The counter here operates as a frequency divider.

Table 5-3 Mode 2 Operation

Initial OUT		High level
GATE input	High level	Count enable
	Low level	Count disable. If GATE becomes low level when OUT is low level, OUT will become high level (independent of the CLK pulse).
	Trigger*	Transfer is performed at the first CLK pulse after the trigger.
Count write		Write count data without affecting the current operation.
Count transfer and operation		Transfer operation is performed at the first CLK pulse after the count is written following the mode setting. The count is then decremented. Transfer is again performed at the first CLK pulse after the count becomes 1. When the trigger is present, the transfer operation is repeated at the next CLK pulse. When the contents of the down counter become 1, OUT becomes low level for one CLK and then returns to high level. Therefore, if a count of N is set, out will repeat this sequence with a period of N CLK pulses.
Count ZERO		Does not occur in this mode
Minimum count		2

* The trigger is ignored when the count has not yet been written after the mode is set, or when only byte of count has been written in the 2-byte read/write mode.

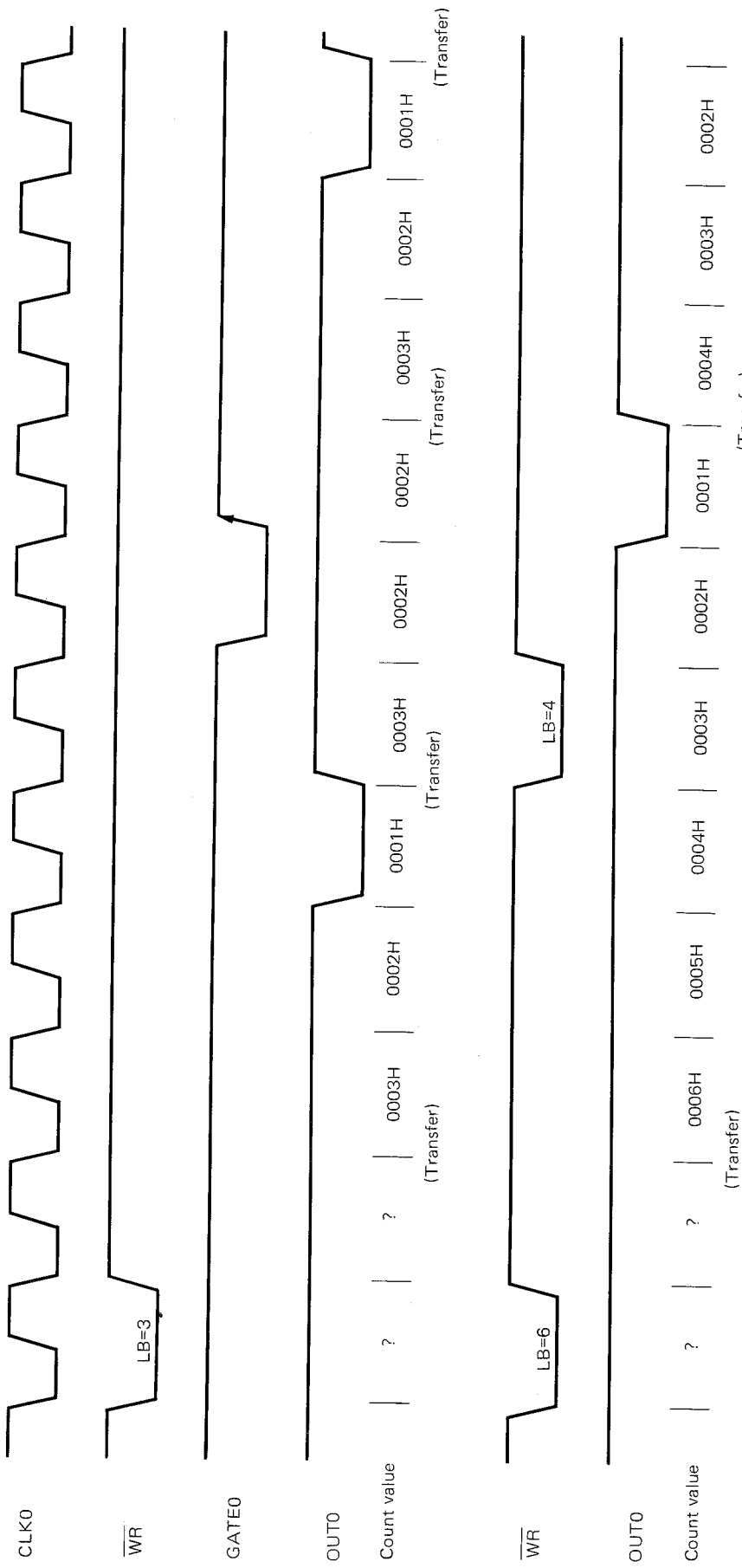


Fig. 5-4 Mode 2 Operation Example

Mode 2 Program example

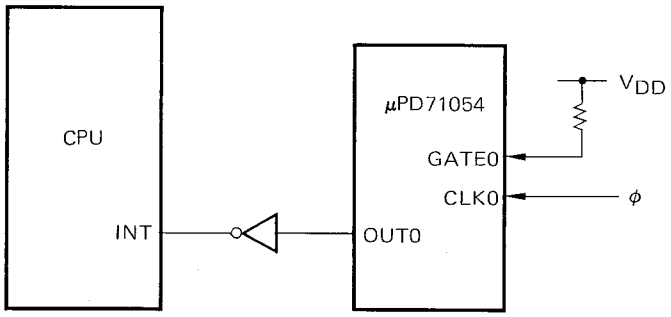
This is a subroutine that generates an interrupt to the CPU each time a fixed period elapses. Counter #0 is set in the lower-higher 2-byte read/write mode and performs binary counting.

```
SUBR3:  MOV   AL, 00110100B   }
        OUT   PCTRL, AL       }

        MOV   AL, 10H         }
        OUT   PCNT0, AL       }
        MOV   AL, 27H         }
        OUT   PCNT0, AL       }

        RET
```

Mode setting

- ○ Counter #0
- ○ Lower-higher 2-byte read/write mode
- ○ Count mode 2
- ○ Binary

Write count 10000



5.4 Mode 3: Square Wave Generator

This is a frequency divider like that shown for mode 2. Only the duty cycles of these two modes are different.

Table 5-4 Mode 3 Operation

Initial OUT		High level
GATE input	High level	Count enable
	Low level	Count disable. If GATE becomes low level when OUT is low level, OUT will become low level (independent of the CLK pulse).
	Trigger*	Transfer is performed at the first CLK pulse after the trigger.
Count write		The current operation is not affected. The count is transferred at the end of the half-period of the current square wave. At the same time, the OUT pin becomes high level.
Count transfer and operation		Count data is transferred at the first CLK pulse after the count write following the mode setting. Transfer is performed at the end of the current half cycle and the output of the OUT pin is inverted. Transfer is also performed at the CLK pulse after the trigger is input. The operation performed will differ depending on whether count N is even or odd. When N is even, the count is decremented by twos. After the count becomes 2, transfer will be performed at the next CLK pulse and the state of the OUT pin will be inverted. This is taken as a half cycle and is repeated thereafter. When N is odd, N-1 is transferred and the count is decremented by twos. The half cycle when the OUT pin is high level continues until the count value becomes 0 and N-1 is transferred again at the next CLK pulse. The half cycle while OUT is low level continues only until the count becomes 2. For this reason, the half cycle with OUT=1 is one CLK longer than the one with OUT=0.
Count ZERO		Occurs only when the count is odd.
Minimum count		2

* The trigger is ignored when the count has not yet been written after the mode is set, or when only 1 byte of count has been written in the 2-byte read/write mode.

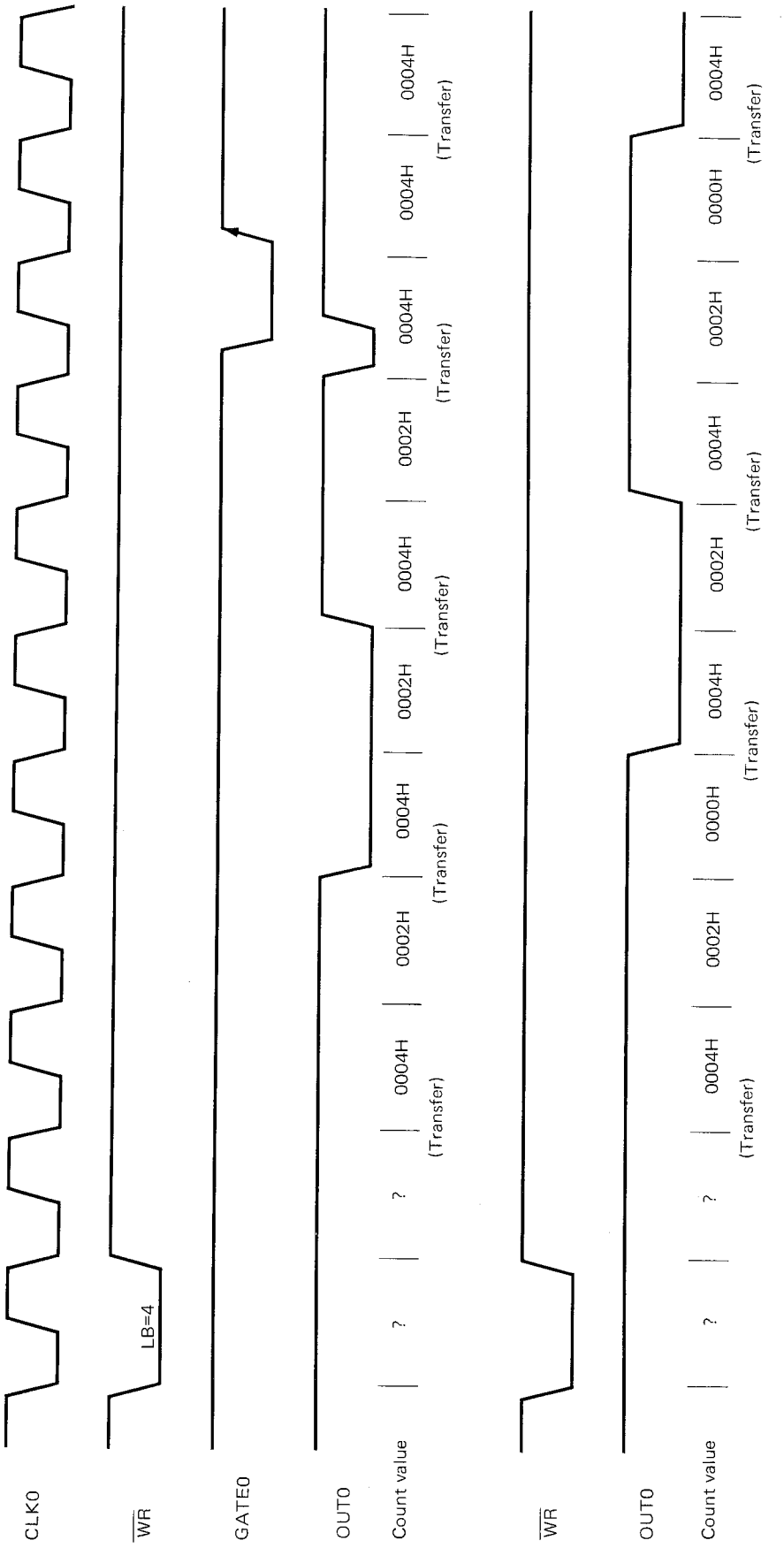


Fig. 5-5 Mode 3 Operation Example

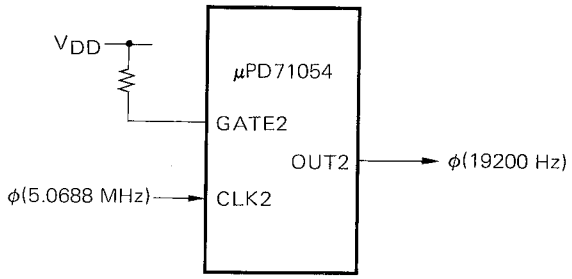
Mode 3 Program example

This is a subroutine that divides the input CLK frequency (5.0688 MHz) by 264 (108H) to obtain an 19,200 Hz clock. Counter #2 is used in the low/high 2-byte read/write mode to perform binary count operation.

```
SUBR4:  MOV   AL, 10110110B   }
        OUT   PCTRL, AL       }

        MOV   AL, 08H         }
        OUT   PCNT2, AL       }
        MOV   A, 01H          }
        OUT   PCNT2, AL       }
        RET
```

Mode specification
- ○ Counter #2
- ○ Low/high 2-byte read/write mode
- ○ Count mode 3
- ○ Binary

264 frequency division specification



5.5 Mode 4: Software-Triggered strobe

When the specified count is up, OUT will become low level for one CLK pulse only. The strobe is generated only once per a transfer of a count number.

Table 5-5 Mode 4 Operation

Initial OUT		High level
GATE input	High level	Count enable
	Low level	Count disable
Count write		When the count is written, the data is transferred at the next CLK pulse. In the 2-byte read/write mode, transfer is performed after the second byte is written.
Count transfer and operation		Data transfer is performed at the first CLK pulse following the count write. If GATE is high level, the down counter will start to decrement from the next CLK pulse, and if GATE is low level, decrement operation will start at the first CLK pulse after GATE becomes high level.
Count ZERO		The OUT pin is low level for one CLK and then becomes high level again. The down counter counts to FFFFH (binary) or 9999 (BCD) without stopping the counter operation.
Minimum count		1

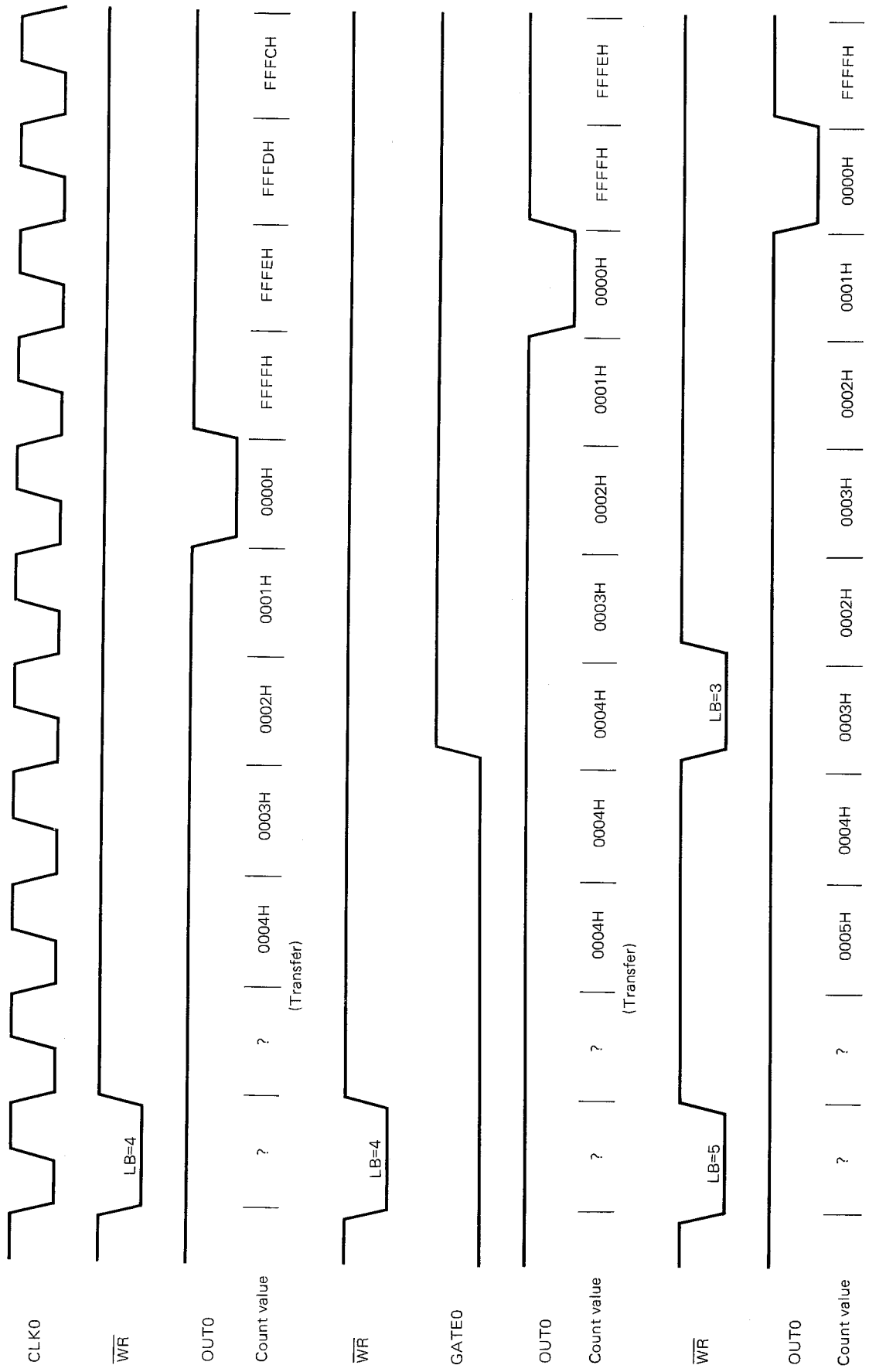


Fig. 5-6 Mode 4 Operation Example

5.6 Mode 5: Hardware-Triggered Strobe (Retriggerable)

The operation is identical to mode 4 except it is started by the GATE input and can be retriggered. The strobe is generated only once per transferring a count number.

Table 5-6 Mode 5 Operation

Initial OUT		High level
GATE input	Trigger*	The count is transferred at the CLK pulse after the trigger.
Count write		Write count without affecting the current operation.
Count transfer and operation		With a trigger, transfer is performed at the next CLK pulse. Decrement operation starts from the first CLK pulse after data transfer. If a count of N is set, the OUT pin will not become low level for N+1 CLK pulses after the trigger.
Count ZERO		The OUT pin is low level for one CLK and then becomes high level again. The down counter counts to FFFFH (binary) or 9999 (BCD) without stopping the counter operation.
Minimum count		1

* The trigger is ignored when the count has not yet been written after the mode is set, or when only 1 byte of count has been written in the 2-byte read/write mode.

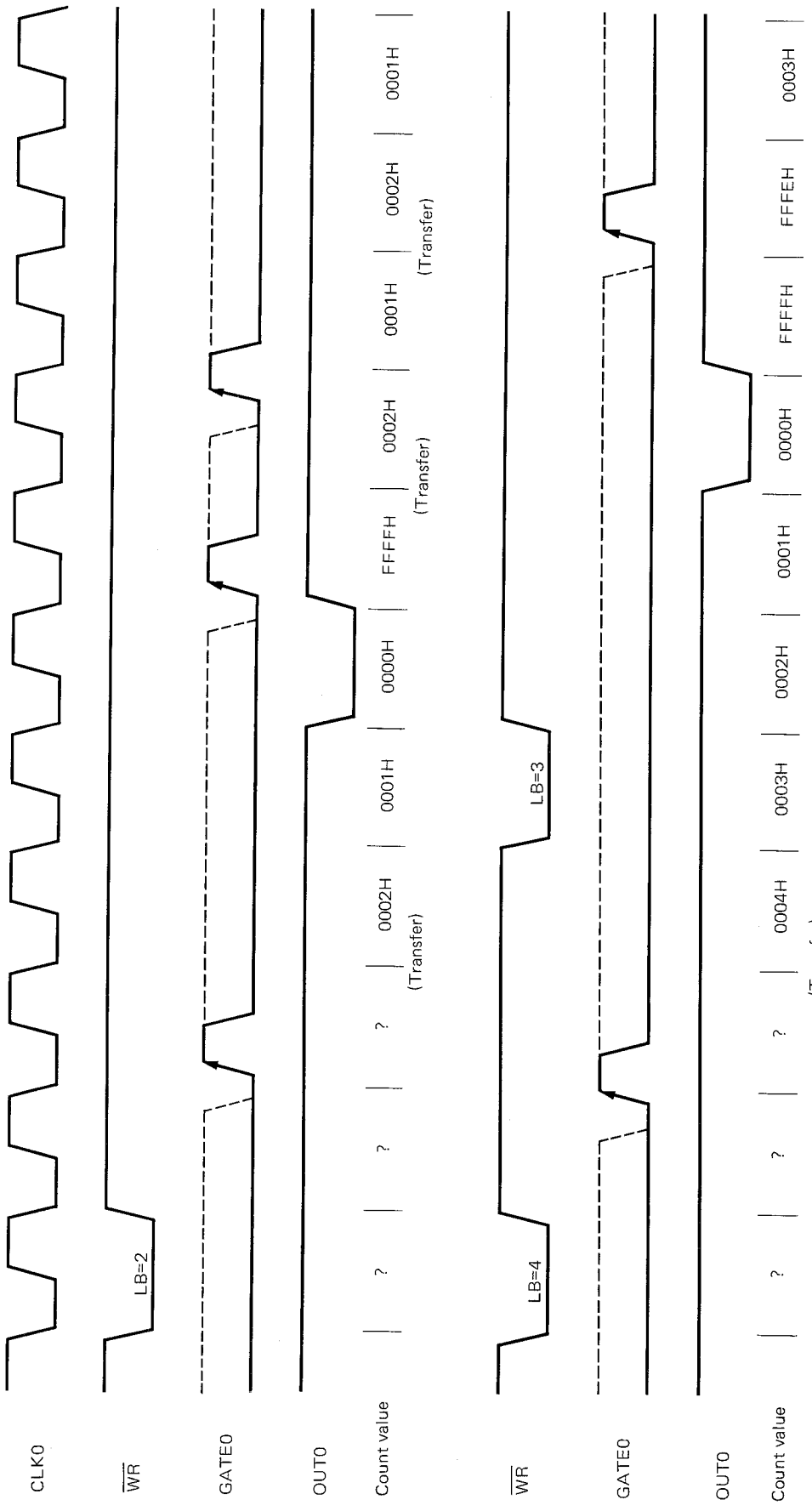


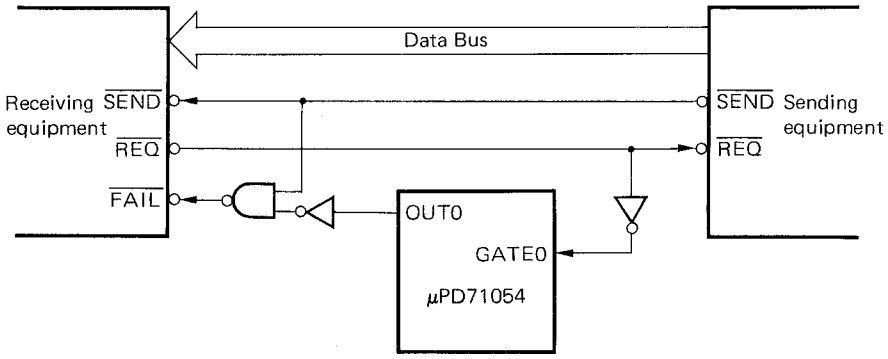
Fig. 5-7 Mode 5 Operation Example

Mode 5 Program Example

Mode 5 can be used to add a fail-safe function to the interface below.

The reception unit requests data send by issuing a $\overline{REQ}$ signal to the transmission unit. The transmission unit responds by outputting data onto the data bus and returning a $\overline{SEND}$ signal to inform the reception unit. In such a system, if there is a malfunction in the transmission unit and no $\overline{SEND}$ signal is sent, the reception unit will wait indefinitely for the $\overline{SEND}$ signal and the operation of the entire system will come to a halt. The example below is designed as a countermeasure for such situations. If no $\overline{SEND}$ signal is output within a fixed period (50 CLK cycles in this example) after the $\overline{REQ}$ signal is output, a malfunction in the transmission unit will be detected and a $\overline{FAIL}$ signal will be sent to the reception unit.

```
SUBR5:  MOV     AL,00011010B    ; Mode setting
                                ;  o Counter #0
        OUT     PCTRL,AL        ;  o Low 1-byte read/write mode
                                ;  o Count mode 5
        MOV     AL,50           ;  o Binary
        OUT     PCNT0,AL        ; Interval setting
        RET                     ; (50 CLK pulses)
```



6. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_a = 25 °C)

Power Supply Voltage	V_{DD}	-0.5 to +7.0	V
Input Voltage	V_I	-0.5 to V_{DD} +0.3	V
Output Voltage	V_O	-0.5 to V_{DD} +0.3	V
Operating Temperature	T_{opt}	-40 to +85	°C
Storage Temperature	T_{stg}	-65 to +150	°C

DC Characteristics (T_a=−40 °C to +85 °C, V_{DD}=+5 V ±10 %)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Input High Voltage	V_{IH}	2.2		V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	−0.5		0.8	V	
Output High Voltage	V_{OH}	0.7XV_{DD}			V	I_{OH}=−400 μA
Output Low Voltage	V_{OL}			0.4	V	I_{OL}=2.5 mA
Input Leakage High	I_{LIH}			10	μA	V_I=V_{DD}
Input Leakage Low	I_{LIL}			−10	μA	V_I=0 V
Output Leakage High	I_{LOH}			10	μA	V_O=V_{DD}
Output Leakage Low	I_{LOL}			−10	μA	V_O=0 V
Supply Current	I_{DD1}			30	mA	μPD71054 (at 8 MHz)
			10	20		μPD71054-10 (at 10 MHz)
	I_{DD2}		2	50	μA	Standby Mode: Input Pins; V_{IH}=V_{DD}−0.1 V, V_{IL}=0.1 V; Output Pins; Open

Capacitance (T_a = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz; Unmeasured pins returned to 0 V
I/O Capacitance	$C_{I/O}$			20	pF	

AC Characteristics (T_a=−40 °C to +85 °C, V_{DD}=5 V ±10 %)

Read Cycle

Parameter	Symbol	μPD71054		μPD71054-10		Unit	Condition
		MIN.	MAX.	MIN.	MAX.		
Address Setup Time (Against $\overline{RD}$↓)	t_{SAR}	30		20		ns	
Address Hold Time (Against $\overline{RD}$↑)	t_{HRA}	10		0		ns	
$\overline{CS}$ Setup Time (Against $\overline{RD}$↓)	t_{SCR}	0		0		ns	
$\overline{RD}$ Pulse Width	t_{RRL}	150		95		ns	
Data Delay Time (From $\overline{RD}$↓)	t_{DRD}		120		85	ns	C_L=150 pF
Data Float Time (From $\overline{RD}$↑)	t_{FRD}	10	85	10	65	ns	C_L=20 pF, R_L=2 kΩ
Data Delay Time (From Address)	t_{DAD}		220		185	ns	C_L=150 pF
Read Recovery Time	t_{RV}	200		165			

Write Cycle

Parameter	Symbol	μPD71054		μPD71054-10		Unit	Condition
		MIN.	MAX.	MIN.	MAX.		
Address Setup Time (Against $\overline{WR}$↓)	t_{SAW}	0		0		ns	
Address Hold Time (Against $\overline{WR}$↑)	t_{HWA}	0		0		ns	
$\overline{CS}$ Setup Time (Against $\overline{WR}$↓)	t_{SCW}	0		0		ns	
$\overline{WR}$ Pulse Width	t_{WWL}	160		95		ns	
Data Setup Time (Against $\overline{WR}$↑)	t_{SDW}	120		95		ns	
Data Hold Time (Against $\overline{WR}$↑)	t_{HWD}	0		0		ns	
Write Recovery Time	t_{RV}	200		165		ns	

AC Characteristics (Continued)

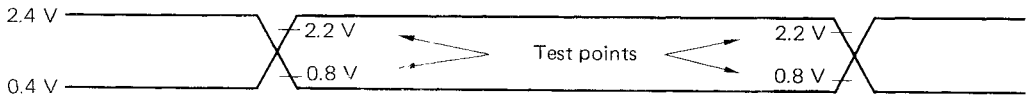
CLK & GATE Timing

Parameter	Symbol	μPD71054		μPD71054-10		Unit	Condition
		MIN.	MAX.	MIN.	MAX		
Clock Cycle Time	t_{CLK}	125	DC	100	DC	ns	
CLK High Level	t_{KKH}	60		30		ns	
CLK Low Level	t_{KKL}	60		45		ns	
CLK Rise Time	t_{KR}		25		25	ns	
CLK Fall Time	t_{KF}		25		25	ns	
GATE High Level	t_{GGH}	50		50		ns	
GATE Low Level	t_{GGL}	50		50		ns	
GATE Setup Time (Against CLK↑)	t_{SGK}	50		40		ns	
GATE Hold Time (Against CLK↑)	t_{HKG}	50		50		ns	
CLK Delay Time (From $\overline{WR}$↑): For Count Value Write	t_{DWK}	100		40		ns	$t_{KKH} \geqq 125$ ns
		225-t_{KKH}					$t_{KKH} \leqq 125$ ns
CLK Setup Time (Against $\overline{WR}$↑): For Latch Command Write	t_{SKW}	85		60		ns	
GATE Delay Time (From $\overline{WR}$↑)	t_{DWG}	0		0		ns	
OUT Delay Time (From GATE↓)	t_{DGO}		120		100	ns	
OUT Delay Time (From CLK↓)	t_{DKO}		150		100	ns	C_L=150 pF
OUT Delay Time (From $\overline{WR}$↑): Initial OUT	t_{DWO}		295		240	ns	

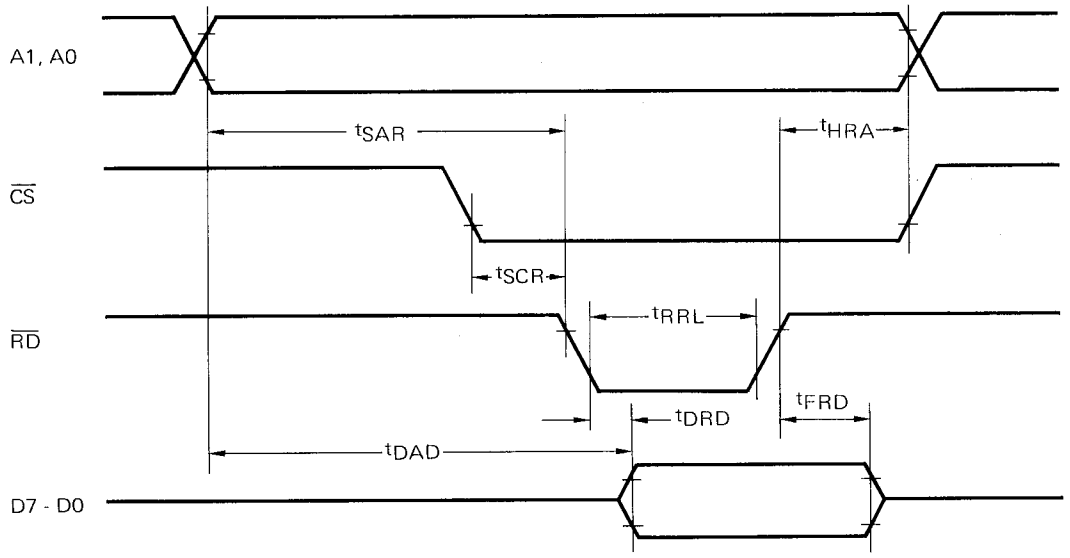
Note: AC timing test points for output

V_{OH} = 2.2 V, V_{OL} = 0.8 V

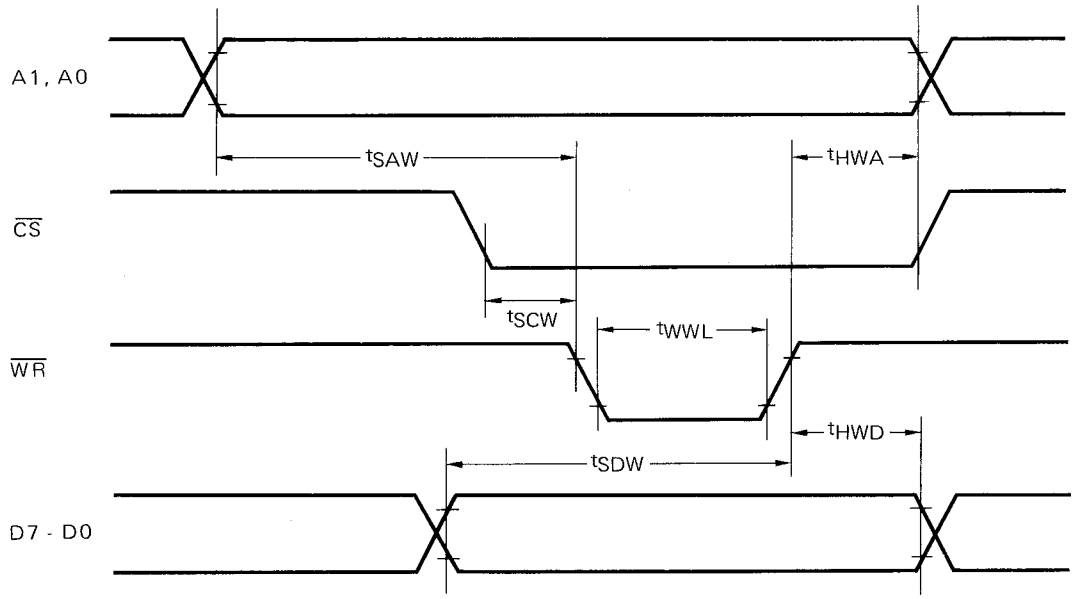
AC Test Input Waveforms



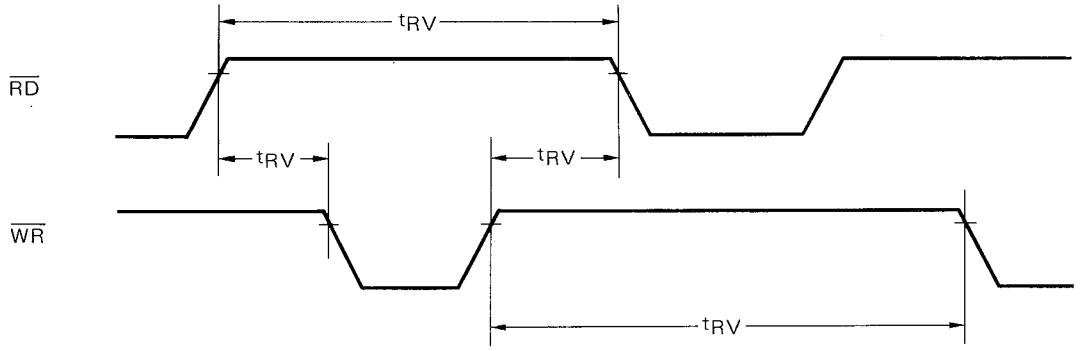
Read Cycle Timing

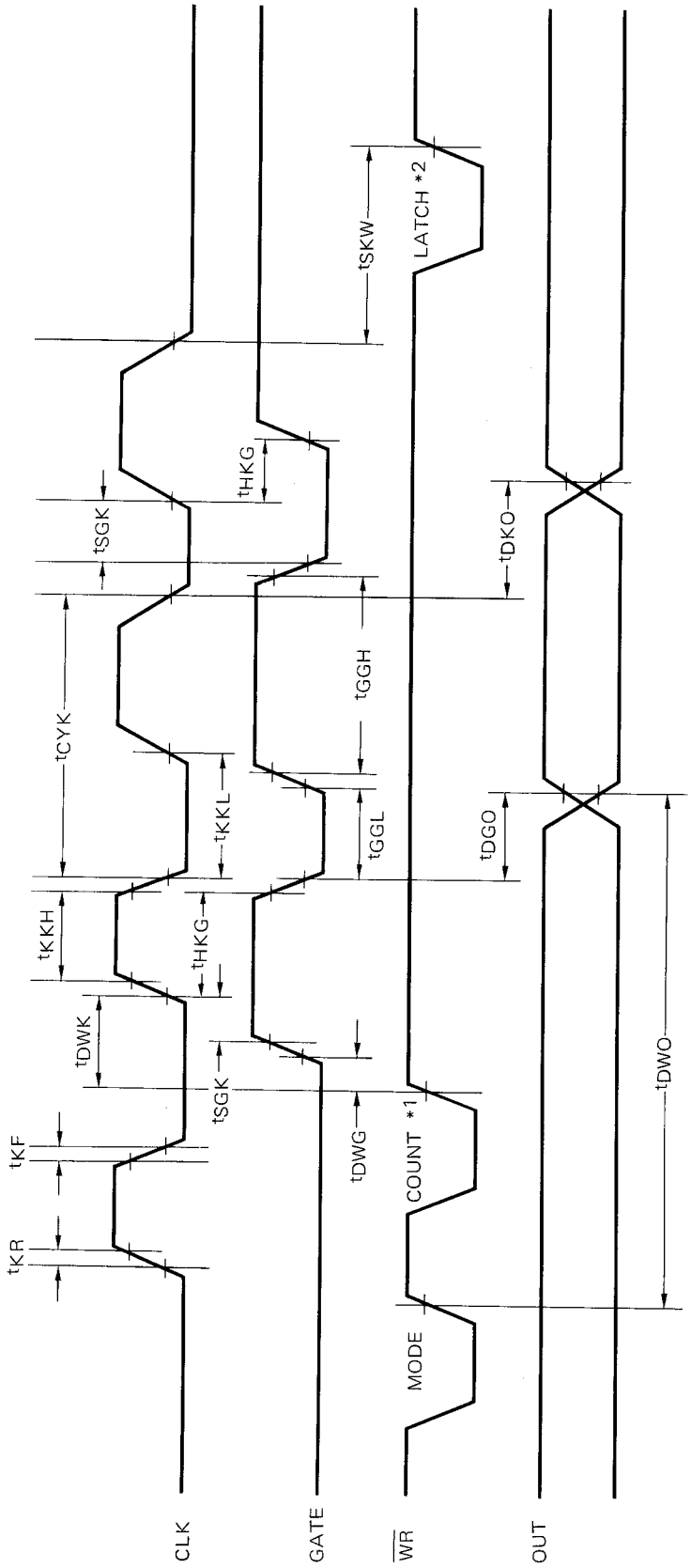


Write Cycle Timing



Read/Write Recovery Time



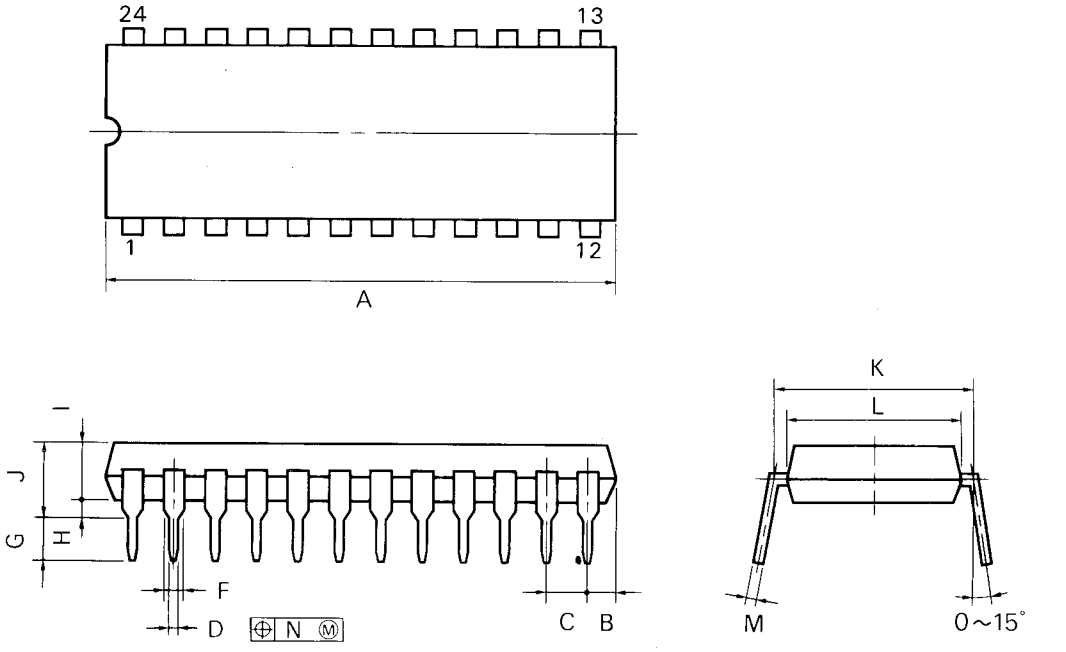


*1: The last 1 byte of count number writing

*2: Count latch command or multiple latch command

7. PACKAGE DIMENSIONS

24-pin Plastic DIP (600 mil)



P24C-100-600

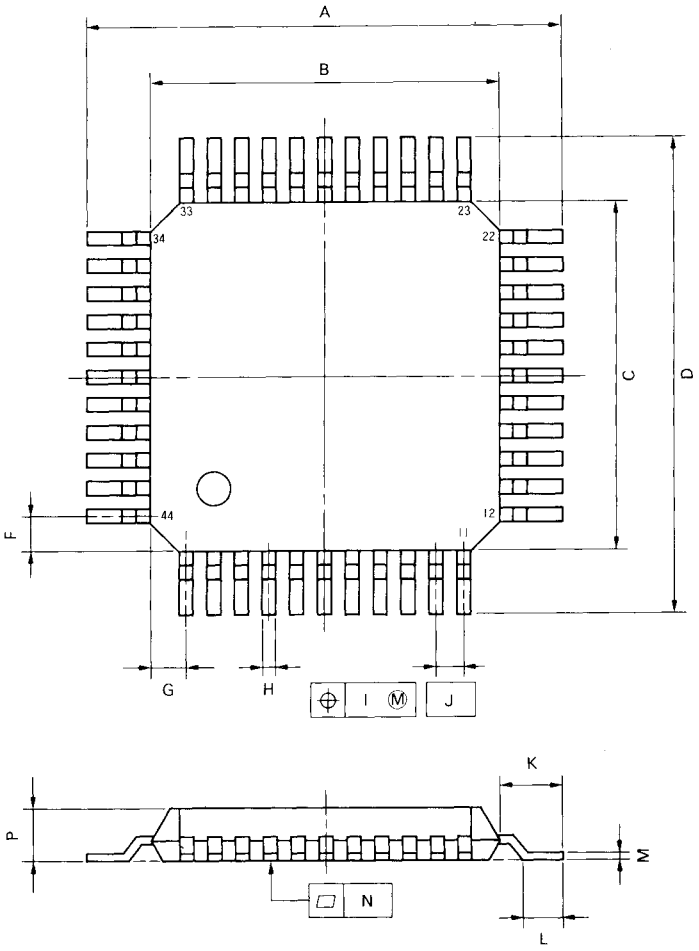
NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

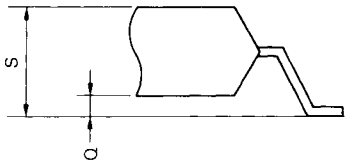
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	33.02 MAX.	1.300 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	$3.5^{\pm 0.3}$	$0.138^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01

44-pin Plastic QFP



detail of lead end



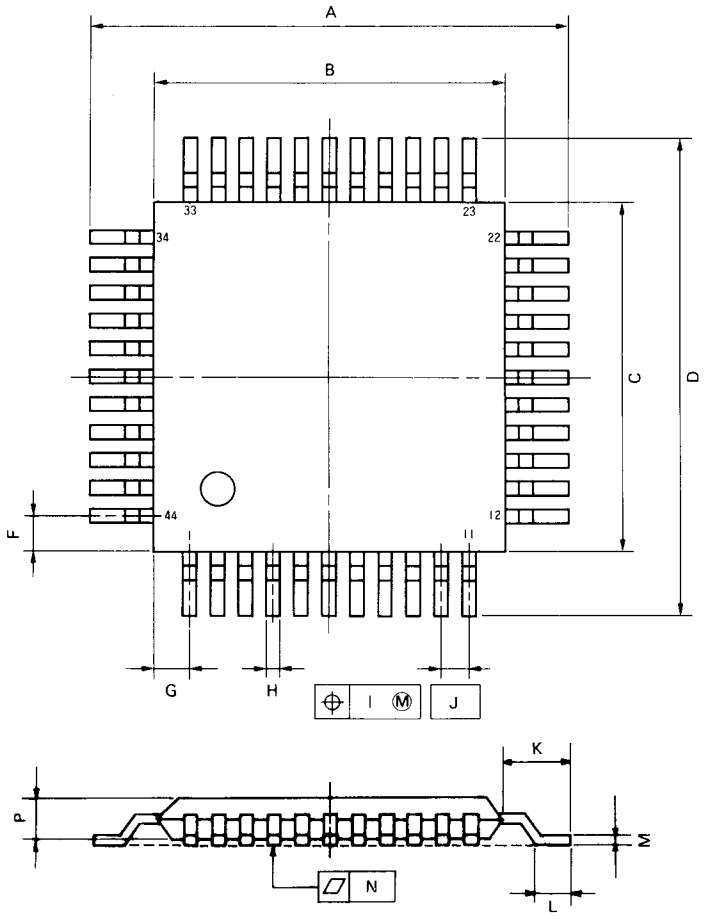
P44G-80-22

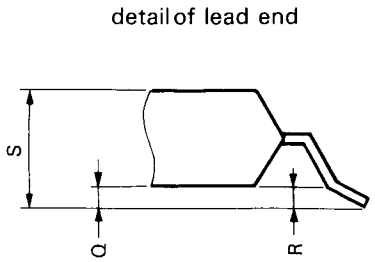
NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$13.6^{\pm 0.4}$	$0.535^{+0.017}_{-0.016}$
B	$10^{\pm 0.2}$	$0.394^{+0.008}_{-0.009}$
C	$10^{\pm 0.2}$	$0.394^{+0.008}_{-0.009}$
D	$13.6^{\pm 0.4}$	$0.535^{+0.017}_{-0.016}$
F	1.0	0.039
G	1.0	0.039
H	$0.35^{+0.20}_{-0.10}$	$0.014^{+0.008}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	$1.8^{\pm 0.2}$	$0.071^{+0.008}_{-0.009}$
L	$1.0^{\pm 0.2}$	$0.039^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	$1.45^{\pm 0.1}$	$0.057^{+0.005}_{-0.004}$
Q	$0.0^{\pm 0.1}$	$0.000^{\pm 0.004}$
S	1.65 MAX.	0.065 MAX.

44-pin Plastic QFP





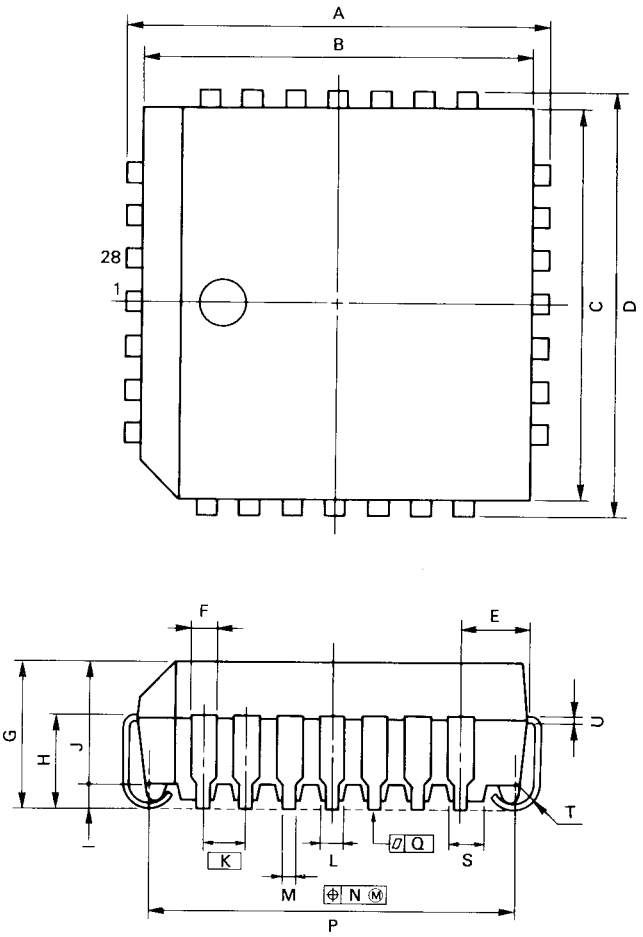
P44GB-80-3B4

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$13.6^{\pm 0.4}$	$0.535^{+0.017}_{-0.016}$
B	$10^{\pm 0.2}$	$0.394^{+0.008}_{-0.009}$
C	$10^{\pm 0.2}$	$0.394^{+0.008}_{-0.009}$
D	$13.6^{\pm 0.4}$	$0.535^{+0.017}_{-0.016}$
F	1.0	0.039
G	1.0	0.039
H	$0.35^{\pm 0.10}$	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	$1.8^{\pm 0.2}$	$0.071^{+0.008}_{-0.009}$
L	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

28-pin PLCC



P28L-50A

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$12.45^{\pm 0.2}$	$0.490^{\pm 0.008}$
B	11.50	0.453
C	11.50	0.453
D	$12.45^{\pm 0.2}$	$0.490^{\pm 0.008}$
E	$1.94^{\pm 0.15}$	$0.076^{+0.007}_{-0.006}$
F	0.6	0.024
G	$4.4^{\pm 0.2}$	$0.173^{+0.009}_{-0.008}$
H	$2.8^{\pm 0.2}$	$0.110^{+0.009}_{-0.008}$
I	0.7 MIN.	0.028 MIN.
J	3.6	0.142
K	1.27 (T.P.)	0.050 (T.P.)
L	0.7	0.028
M	$0.40^{\pm 0.10}$	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	$10.42^{\pm 0.20}$	$0.410^{+0.009}_{-0.008}$
Q	0.15	0.006
S	1.0	0.040
T	R 0.8	R 0.031
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

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