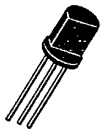
2N4991, 2N4992

Silicon Bilateral Switch



TO-98

The GE/RCA 2N4991, 2N4992 SBSs are planar monolithic silicon integrated circuits having the electrical characteristics of a bilateral thyristor. The device is designed to switch at 8V with a 0.02%/°C temperature coefficient and excellently matched characteristics in both directions. A gate lead is provided to eliminate rate effect and to obtain trigggering at lower voltages.

The silicon bilateral switches are specifically designed and characterized for applications where stability of switching voltage over a wide temperature range and well matched bilateral characteristics are an asset. They are ideally suited for half wave and full wave triggering in low voltage SCR and Triac phase control circuits. These types are supplied in JEDEC TO-98 package

Devices in TO-98 package are supplied with and without seating flange (see Dimensional Outline).

3

MAXIMUM RATINGS, *Absolute-Maximum Values:*

PEAK RECURRENT FORWARD CURRENT (1% duty cycle, 10 μs pulse width, T_A = 100°C)	1 A
PEAK NON-RECURRENT FORWARD CURRENT (10 μs pulse width)	5 A
DC FORWARD ANODE CURRENT (Note 1)	175 mA
DC GATE CURRENT (Notes 1 and 2)	5 mA
POWER DISSIPATION (Note 1)	300 mW
OPERATING JUNCTION TEMPERATURE RANGE	−55° to +125°C
STORAGE TEMPERATURE RANGE	−65° to +150°C

NOTES:
1. Derate linearly to zero at 125°C.
2. This rating applicable only in OFF state.
   Maximum gate current in conducting state limited by maximum power rating.

TERMINAL CONNECTIONS

Lead 1 - Anode 1
Lead 2 - Gate
Lead 3 - Anode 2

File Number **2048**

2N4991, 2N4992

ELECTRICAL CHARACTERISTICS, At Ambient Temperature (T_A) = 25°C Unless Otherwise Specified

CHARACTERISTICS	SYMBOL	LIMITS						UNITS
		2N4991			2N4992			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX	
Forward Voltage Drop (on state)(I_F = 175 mA)	V_F	–	–	1.7	–	–	1.7	V
Switching Voltage	V_S	6	–	10	7.5	–	9	
Forward Current (off state) (V_F = 5V, T_A = 25°C)	I_B	–	–	1	–	–	0.1	μA
(V_F = 5V, T_A = 85°C	I_B	–	–	10	–	–	10	
Switching Current	I_S	–	–	500	–	–	120	
Absolute Switching Voltage Difference	$\lvert V_{S2}-V_{S1}\rvert$	–	–	0.5	–	–	0.2	V
Absolute Switching Current Difference	$\lvert I_{S2}-I_{S1}\rvert$	–	–	100	–	–	10	μA
Holding Current	I_H	–	–	1.5	–	–	0.5	mA
Forward Gate Current to Trigger (V_F = 5V., RL = 1kΩ)	I_{GF}	–	–	–	–	–	100	μA
Temperature Coefficient of Switching Voltage (T_A = −55°C to +85°C	T_C	–	±0.02	–	–	±0.05	–	%/°C
Turn-on Time (See Circuit 10)	t_{on}	–	–	1	–	–	1	μs
Turn-off Time (See Circuit 11)	t_{off}	–	–	30	–	–	30	
Peak Pulse Voltage (See Circuit 12)	V_O	3.5	–	–	3.5	–	–	V

NOTES:

1. This device is a symmetrical negative resistance diode. All electrical limits shown apply in either direction of current flow.

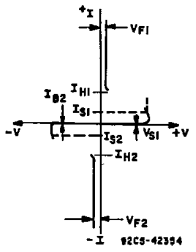


Fig. 1—Static characteristics waveform.

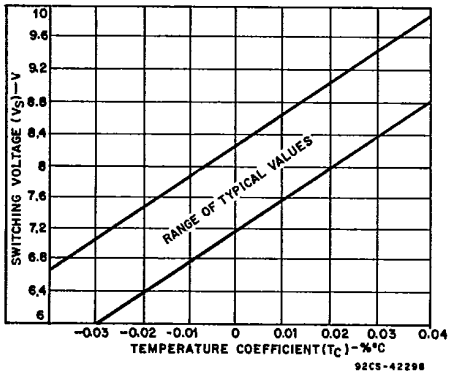


Fig. 2—Typical switching voltage characteristics.

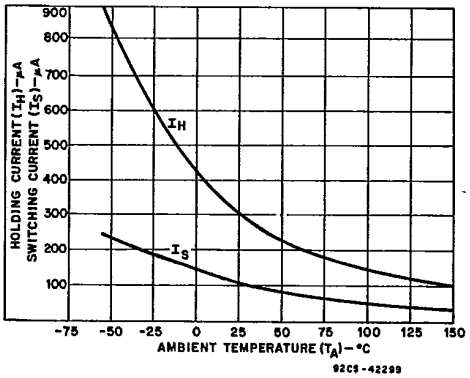


Fig. 3—Typical holding and switching current characteristics.

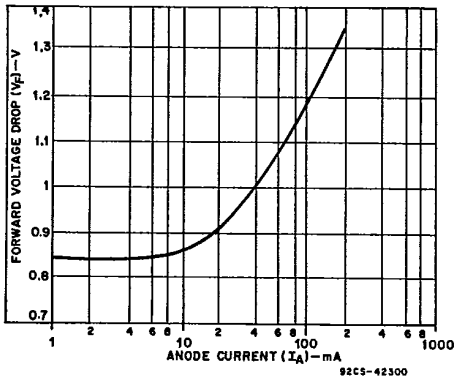


Fig. 4—Typical forward voltage drop characteristic.

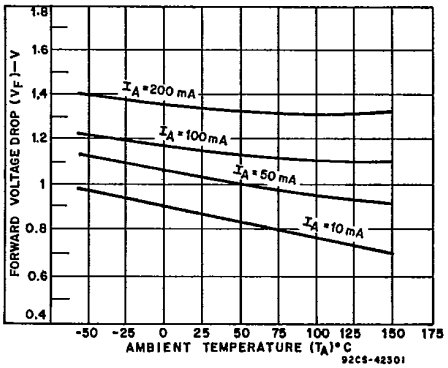


Fig. 5—Typical forward voltage drop characteristic.

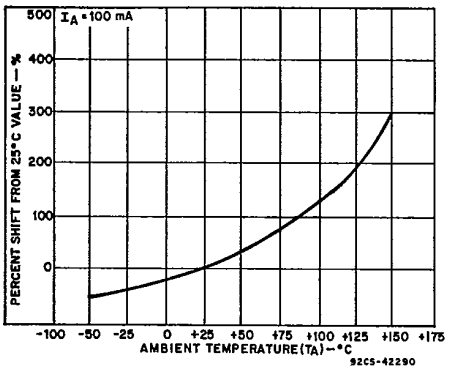


Fig. 6—Typical turn-off time shift characteristic.

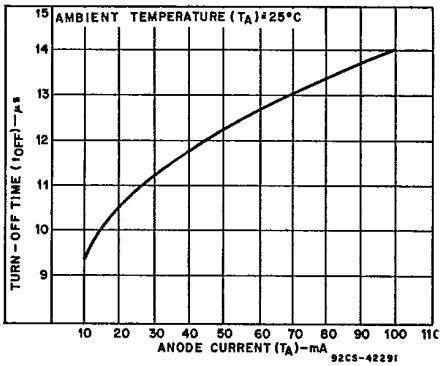


Fig. 7—Typical turn-off time characteristic.

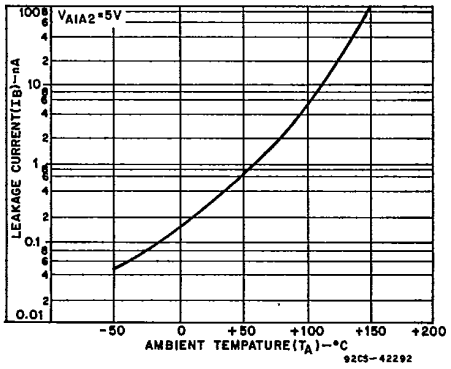


Fig. 8—Typical leakage current characteristic.

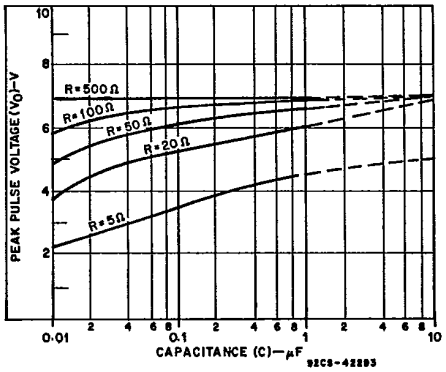


Fig. 9—Typical peak pulse voltage characteristics. (See circuit, Fig. 12)

TEST CIRCUITS

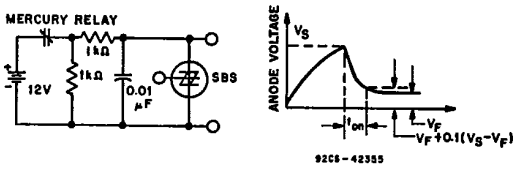


Fig. 10—Turn-on time test circuit and waveform.

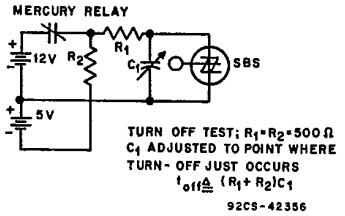


Fig. 11—Turn-off time test circuit.

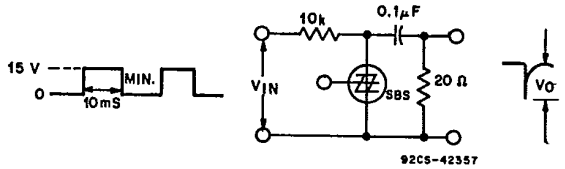


Fig. 12—Peak pulse voltage test circuit and waveforms. (See Fig. 9 for curve)

APPLICATION IN HYSTERESIS-FREE PHASE CONTROL CIRCUIT

The circuit in Figure 13 is a simple hysteresis-free phase control circuit intended for lamp dimming and similar applications. The circuit requires only one RC phase lag network. To avoid the hysteresis (or "snap-on") effect, the capacitor, C, is reset to approximately 0 volts at the end of every positive half cycle (for pot values such that no power is applied to the load). This is accomplished using the gate lead. At the end of the positive half, as the line voltage drops below the capacitor voltage, gate current flows from C out through the gate, D1 and 47kΩ resistor. The SBS fires and discharges C to 0 volts. In the negative half cycle diodes D2 and D1 clamp the gate voltage to ground and block the flow of gate current respectively. Electrical requirements of D1 and D2 are easily met. Any diode with $V_R > 10$ volts works fine. Forward conductance must be fairly good since the voltage across D2 at 3mA must be smaller than the drop across the Triac gate, the SBS gate, and D1 at the trigger current of the SBS.

Figure 14 shows the excellent degree of phase control available in the circuit. For the worst case unit, $\phi max = 155°$ (V_S = 7.5 volts, I_S = 120μA).

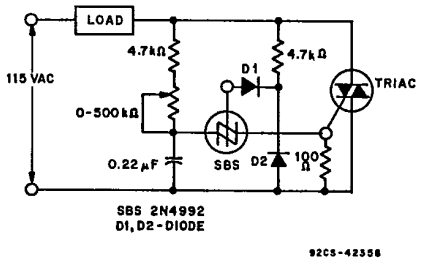


Fig. 13—Typical phase-control circuit for lamp dimming and similar applications.

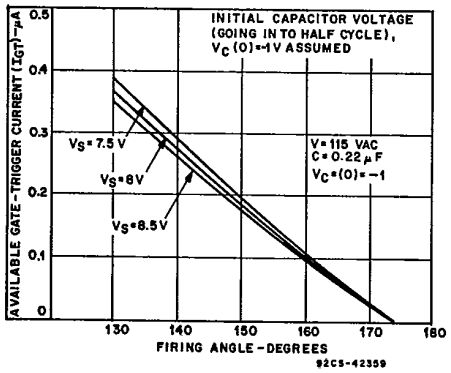


Fig. 14—Typical gate-trigger current characteristic.