File Number **892**

2N6400—2N6404

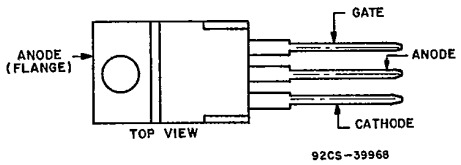
16-A Silicon Controlled Rectifiers

For Power Switching, Power Control, and Ignition Applications

Features:

- *High dv/dt capability*
- *Low thermal resistance*
- *Low on-state voltage at high current levels*

TERMINAL DESIGNATIONS



92CS-39968

JEDEC TO-220AB

The RCA-2N6400 to 2N6404, inclusive, are all-diffused silicon controlled rectifiers (reverse-blocking triode thyristors) designed for switching ac and dc currents.

The TO-220AB package provides easy package mounting and low thermal resistance, allowing operation at high case temperatures and permitting reduced heat-sink size.

MAXIMUM RATINGS, *Absolute-Maximum Values:*	**2N6400**	**2N6401**	**2N6402**	**2N6403**	**2N6404**	
*V_{RSOM}†	75	125	250	450	650	V
V_{DSOM}†	75	125	250	450	650	V
*V_{RROM}†	50	100	200	400	600	V
*V_{DROM}†	50	100	200	400	600	V
$I_{T(RMS)}$ (T_C = 100°C, θ = 180°)			16			A
I_{TSM}: For one full cycle of applied principal						
*voltage 60-Hz‡			160			A
50-Hz‡			135			A
For more than one full cycle of applied principal voltage			See Fig. 4			
di/dt:						
$V_D = V_{DROM}$, I_{GT} = 80 mA, t_r = 0.1 μs (See Fig. 13)			100			A/μs
I^2t:						
T_J = -40 to 125°C, t = 1 to 8.3 ms			100			A^2s
P_{GM}■:						
Peak forward for 10μs max.			16#			W
Peak reverse			See Fig. 7			
*$P_{G(AV)}$■:						
Averaging time = 8 ms maximum			0.5			W
I_{GM}: (forward)			2			A
*T_{stg}			-40 to 150			°C
*T_C			-40 to 125			°C
T_T:						
During soldering for 10 s maximum (terminal and case)			250			°C

* In accordance with JEDEC registration data format (JS-22, RDF-1) filed for the JEDEC (2N series) types.

† These values do not apply if there is a positive gate signal. Gate must be open or negatively biased.

‡ At $I_{T(RMS)}$ = 16 A and T_C = 100°C.

■ Any product of gate current and gate voltage which results in a gate power less than the maximum is permitted.

\# JEDEC registered value is 10 W.

2N6400—2N6404

ELECTRICAL CHARACTERISTICS

As Maximum Ratings Unless Otherwise Specified and at Indicated Case Temperature (T_C)

CHARACTERISTIC	LIMITS FOR ALL TYPES MIN.	TYP.	MAX.	UNITS
I_{DOM} or I_{ROM}: $V_D = V_{DROM}$ or $V_R = V_{RROM}$, $T_C = 125^oC$	–	0.1	2*	mA
v_T: i_T = 32 A (peak), $T_C = 25^oC$ (See Fig. 5)	–	1.4	1.7*	V
i_{HO}: (See Fig. 10) $T_C = 25^oC$ ..... $T_C = -40^oC$	– –	10 –	35 60*	mA
dv/dt: $V_D = V_{DROM}$, exponential voltage rise, $T_C = 125^oC$ (See Fig. 13)	50	–	–	V/μs
I_{GT}: (See Fig. 8) V_D = 12 V (dc), R_L = 50 Ω, $T_C = 25^oC$ ..... V_D = 12 V (dc), R_L = 50 Ω, $T_C = -40^oC$	– –	8 –	30 60*	mA
V_{GT}: (See Fig. 9) V_D = 12 V (dc), R_L = 50 Ω, $T_C = 25^oC$ ..... V_D = 12 V (dc), R_L = 50 Ω, $T_C = -40^oC$	– –	0.7 –	1.5 2.5*	V
V_{GRD}: $V_D = V_{DROM}$, $T_C = 125^oC$	0.2	–	–	V
t_{gt}: $V_D = V_{DROM}$, i_T = 32 A (peak), I_{GT} = 200 mA, t_r = 0.02 μs, $T_C = 25^oC$ (See Figs. 13 & 14)	–	–	2*	μs
tq: Rectangular Pulse $V_D = V_{DROM}$, i_T = 16 A, pulse duration = 50 μs, dv/dt = 50 V/μs, −di/dt = −10A/μs, I_{GT} = 80 mA at turn-on, V_R = 20 V minimum, V_{GK} = 0 V at turn-off, $T_C = 75^oC$ (See Fig. 16)	–	35	75	μs
$R_{\theta JC}$ ..... $R_{\theta JA}$	– –	– –	1.5* 50*	°C/W

* In accordance with JEDEC registration data format (JS-22, RDF-1) filed for the JEDEC (2N series) types.

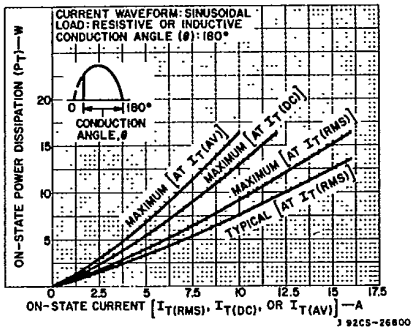


Fig. 1 — On-state power dissipation vs. on-state current.

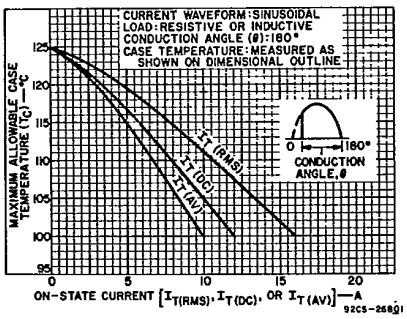


Fig. 2 — Maximum allowable case temperature vs. on-state current.

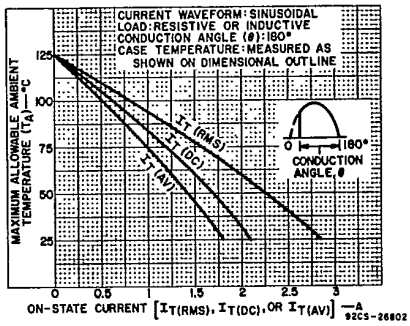


Fig. 3 — Maximum allowable ambient temperature vs. on-state current — no heat sinking.

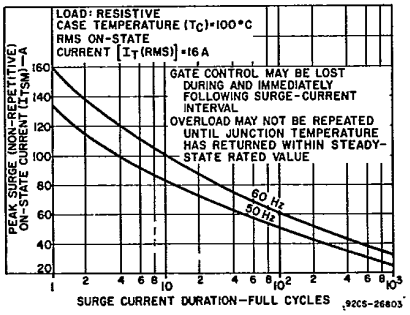


Fig. 4 — Allowable peak surge on-state current vs. surge duration.

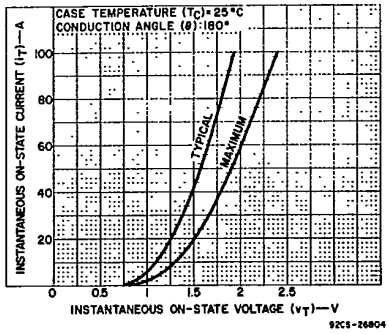


Fig. 5 — Instantaneous on-state current vs. instantaneous on-state voltage.

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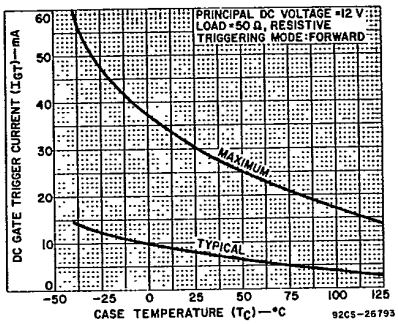

Fig. 6 — DC gate trigger current vs. case temperature.

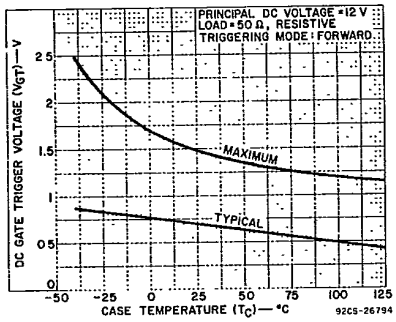

Fig. 7 — DC gate trigger voltage vs. case temperature.

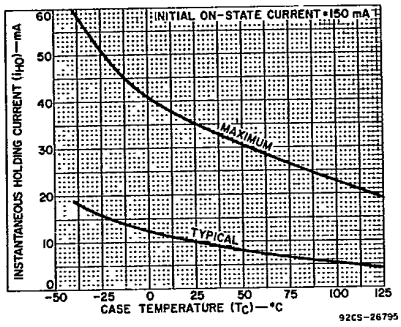

Fig. 8 — Instantaneous holding current vs. case temperature.

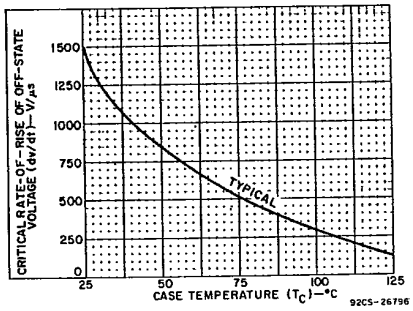

Fig. 9 — Critical rate of rise of off-state voltage vs. case temperature.

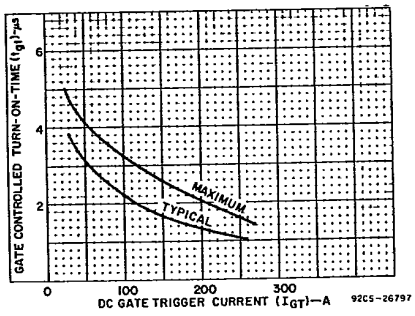

Fig. 10 — Typical gate-controlled turn-on time vs. gate trigger current.

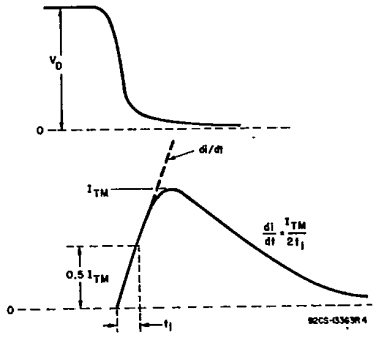

Fig. 11 — Rate of change of on-state current with time (defining di/dt).

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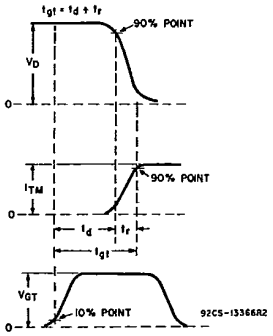

Fig. 12 — Relationship between off-state voltage, on-state current, and gate-trigger voltage showing reference points for definition of turn-on time (t_{gt}).

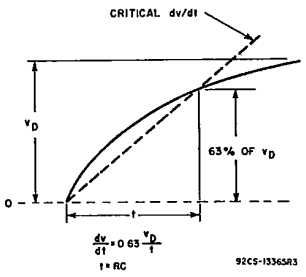

Fig. 13 — Rate of rise of off-state voltage with time (defining critical dv/dt).

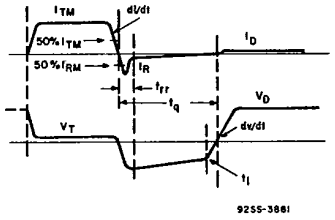

Fig. 14 — Relationship between instantaneous on-state current and voltage, showing reference points for definition of circuit-commutated turn-off time (t_q).