

File Number 1824

IRF150, IRF151, IRF152, IRF153

**Power MOS Field-Effect Transistors**

**N-Channel Enhancement-Mode Power Field-Effect Transistors**

33 A and 40 A, 60 V - 100 V  
 $r_{DS(on)} = 0.055 \Omega$  and  $0.08 \Omega$

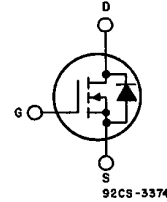
**Features:**

- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance
- Majority carrier device

The IRF150, IRF151, IRF152 and IRF153 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

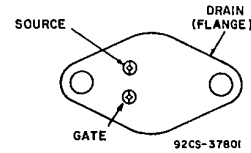
The IRF-types are supplied in the JEDEC TO-204AE metal package.

**N-CHANNEL ENHANCEMENT MODE**



**TERMINAL DIAGRAM**

**TERMINAL DESIGNATION**



**JEDEC TO-204AE**

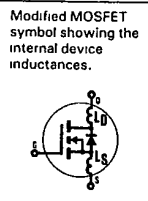
**Absolute Maximum Ratings**

Parameter	IRF150	IRF151	IRF152	IRF153	Units
$V_{DS}$ Drain - Source Voltage ①	100	60	100	60	V
$V_{DGR}$ Drain - Gate Voltage ( $R_{GS} = 20 \text{ k}\Omega$ ) ①	100	60	100	60	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	40	40	33	33	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current	25	25	20	20	A
$I_{DM}$ Pulsed Drain Current ②	160	160	132	132	A
$V_{GS}$ Gate - Source Voltage	$\pm 20$				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	150		(See Fig. 14)		W
Linear Derating Factor	1.2		(See Fig. 14)		W/K
$I_{LM}$ Inductive Current, Clamped	160	160	132	132	A
$T_J$ Operating Junction and $T_{stg}$ Storage Temperature Range	-55 to 150				$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

**IRF150, IRF151, IRF152, IRF153**

**Electrical Characteristics @ T<sub>C</sub> = 25°C (Unless Otherwise Specified)**

Parameter	Type	Min.	Typ	Max.	Units	Test Conditions
BV <sub>DSS</sub> Drain-Source Breakdown Voltage	IRF150 IRF152	100	-	-	V	V <sub>GS</sub> = 0V I <sub>D</sub> = 250μA
	IRF151 IRF153	60	-	-	V	
V <sub>GS(th)</sub> Gate Threshold Voltage	ALL	2.0	-	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
I <sub>GSS</sub> Gate-Source Leakage Forward	ALL	-	-	100	nA	V <sub>GS</sub> = 20V
I <sub>GSS</sub> Gate-Source Leakage Reverse	ALL	-	-	-100	nA	V <sub>GS</sub> = -20V
I <sub>DSS</sub> Zero Gate Voltage Drain Current	ALL	-	-	250	μA	V <sub>DS</sub> = Max. Rating, V <sub>GS</sub> = 0V V <sub>DS</sub> = Max. Rating x 0.8, V <sub>GS</sub> = 0V, T <sub>C</sub> = 125°C
	ALL	-	-	1000	μA	
I <sub>D(on)</sub> On-State Drain Current ②	IRF150 IRF151	40	-	-	A	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)</sub> max., V <sub>GS</sub> = 10V
	IRF152 IRF153	33	-	-	A	
R <sub>DS(on)</sub> Static Drain-Source On-State Resistance ②	IRF150 IRF151	-	0.045	0.055	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 20A
	IRF152 IRF153	-	0.06	0.08	Ω	
g <sub>fs</sub> Forward Transconductance ②	ALL	9.0	11	-	S (ft)	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)</sub> max., I <sub>D</sub> = 20A
C <sub>iss</sub> Input Capacitance	ALL	-	2000	3000	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V, f = 1.0 MHz See Fig. 10
C <sub>oss</sub> Output Capacitance	ALL	-	1000	1500	pF	
C <sub>rss</sub> Reverse Transfer Capacitance	ALL	-	350	500	pF	
t <sub>d(on)</sub> Turn-On Delay Time	ALL	-	-	35	ns	V <sub>DD</sub> = 24V, I <sub>D</sub> = 20A, Z <sub>0</sub> = 4.7Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)
t <sub>r</sub> Rise Time	ALL	-	-	100	ns	
t <sub>d(off)</sub> Turn-Off Delay Time	ALL	-	-	125	ns	
t <sub>f</sub> Fall Time	ALL	-	-	100	ns	
Q <sub>g</sub> Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	-	63	120	nC	
Q <sub>gs</sub> Gate-Source Charge	ALL	-	27	-	nC	V <sub>GS</sub> = 10V, I <sub>D</sub> = 50A, V <sub>DS</sub> = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q <sub>gd</sub> Gate-Drain ("Miller") Charge	ALL	-	36	-	nC	
L <sub>D</sub> Internal Drain Inductance	ALL	-	5.0	-	nH	
L <sub>S</sub> Internal Source Inductance	ALL	-	12.5	-	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.



**Thermal Resistance**

R <sub>thJC</sub> Junction-to-Case	ALL	-	-	0.83	K/W	
R <sub>thCS</sub> Case-to-Sink	ALL	-	0.1	-	K/W	Mounting surface flat, smooth, and greased.
R <sub>thJA</sub> Junction-to-Ambient	ALL	-	-	30	K/W	Free Air Operation

**Source-Drain Diode Ratings and Characteristics**

I <sub>S</sub> Continuous Source Current (Body Diode)	IRF150 IRF151	-	-	40	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
	IRF152 IRF153	-	-	33	A	
I <sub>SM</sub> Pulse Source Current (Body Diode) ③	IRF150 IRF151	-	-	160	A	
	IRF152 IRF153	-	-	132	A	
V <sub>SD</sub> Diode Forward Voltage ②	IRF150 IRF151	-	-	2.5	V	T <sub>C</sub> = 25°C, I <sub>S</sub> = 40A, V <sub>GS</sub> = 0V
	IRF152 IRF153	-	-	2.3	V	T <sub>C</sub> = 25°C, I <sub>S</sub> = 33A, V <sub>GS</sub> = 0V
t <sub>rr</sub> Reverse Recovery Time	ALL	-	600	-	ns	T <sub>J</sub> = 160°C, I <sub>F</sub> = 40A, dI <sub>F</sub> /dt = 100A/μs
Q <sub>RR</sub> Reverse Recovered Charge	ALL	-	3.3	-	μC	T <sub>J</sub> = 150°C, I <sub>F</sub> = 40A, dI <sub>F</sub> /dt = 100A/μs
t <sub>on</sub> Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L <sub>S</sub> + L <sub>D</sub> .				

① T<sub>J</sub> = 25°C to 160°C. ② Pulse Test: Pulse width < 300μs, Duty Cycle < 2%. ③ Repetitive Rating: Pulse width limited by max junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

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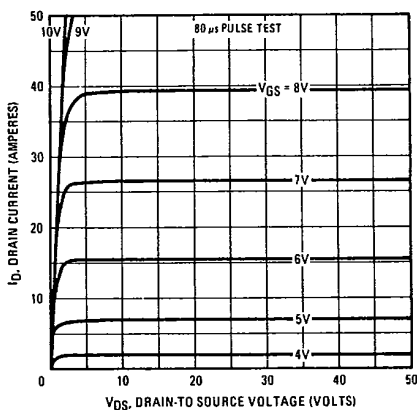


Fig. 1 - Typical Output Characteristics

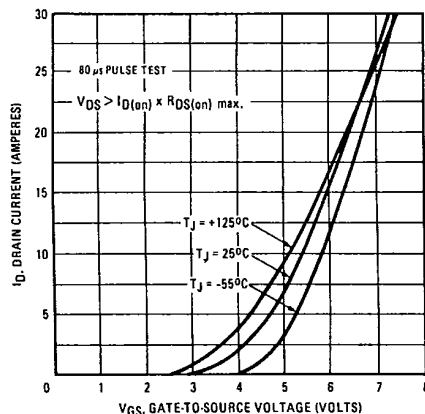


Fig. 2 - Typical Transfer Characteristics

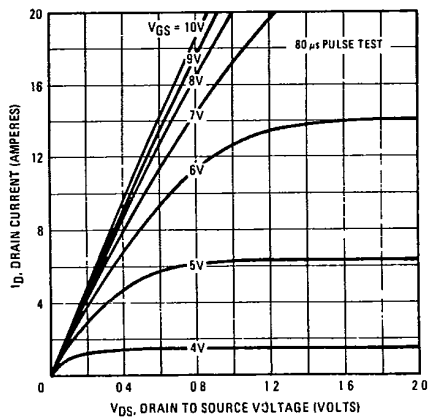


Fig. 3 - Typical Saturation Characteristics

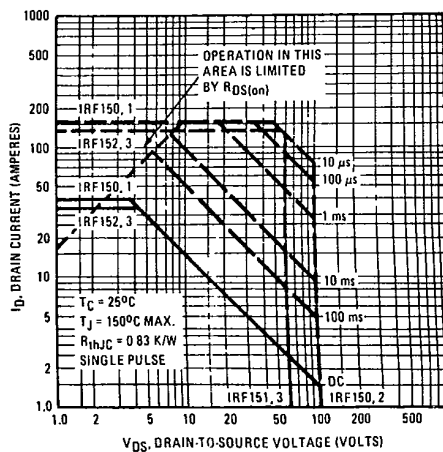


Fig. 4 - Maximum Safe Operating Area

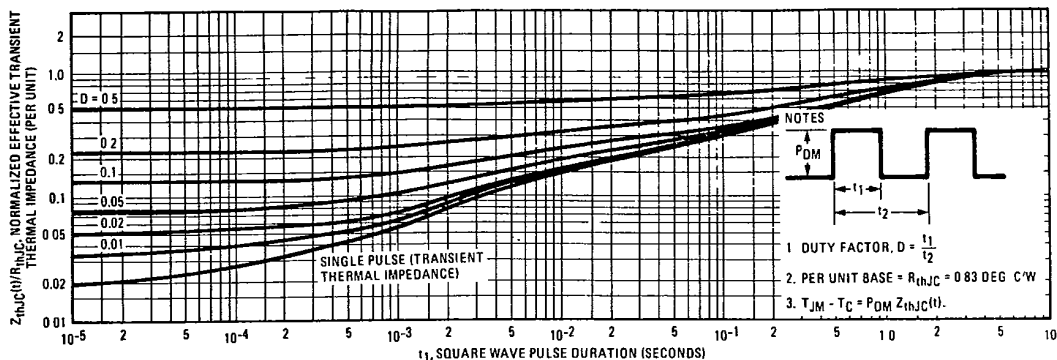


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

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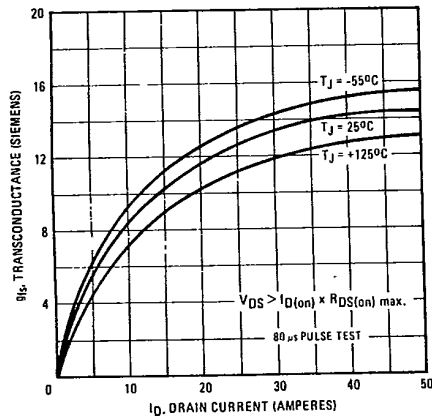


Fig. 6 - Typical Transconductance Vs. Drain Current

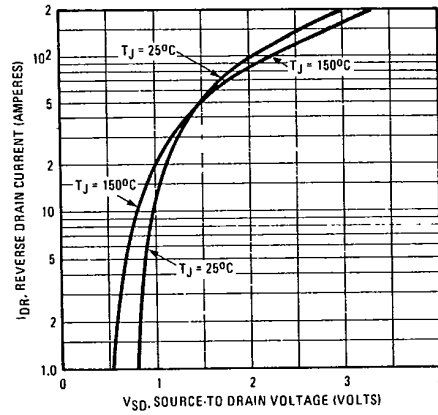


Fig. 7 - Typical Source-Drain Diode Forward Voltage

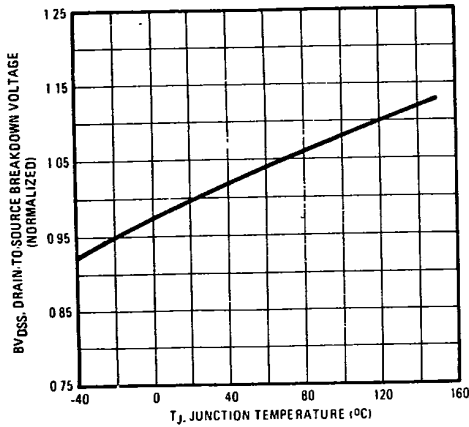


Fig. 8 - Breakdown Voltage Vs. Temperature

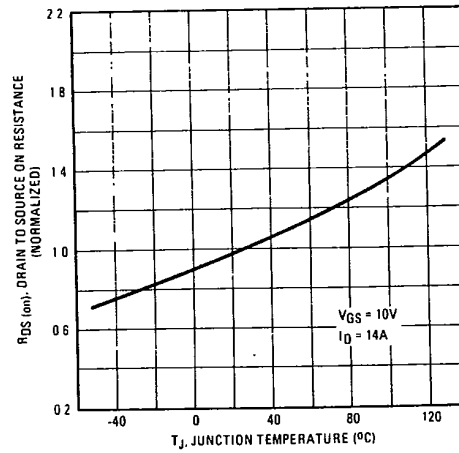


Fig. 9 - Normalized On-Resistance Vs. Temperature

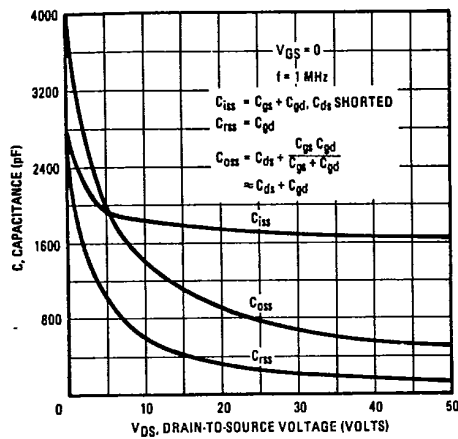


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

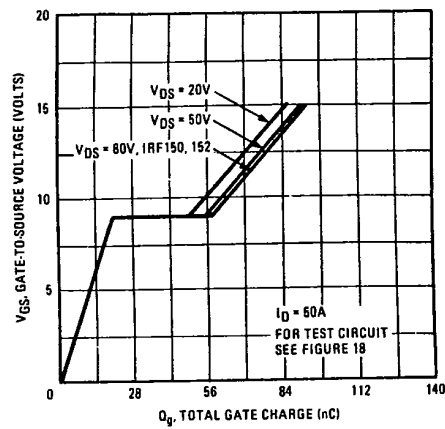


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

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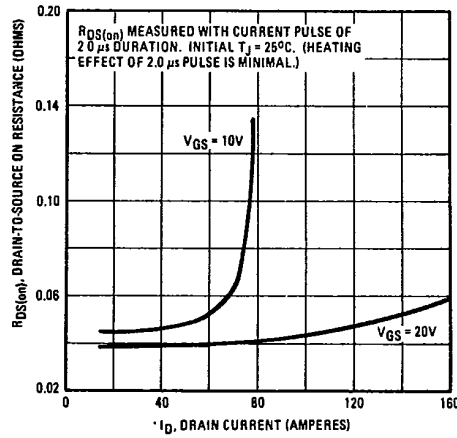


Fig. 12 - Typical On-Resistance Vs. Drain Current

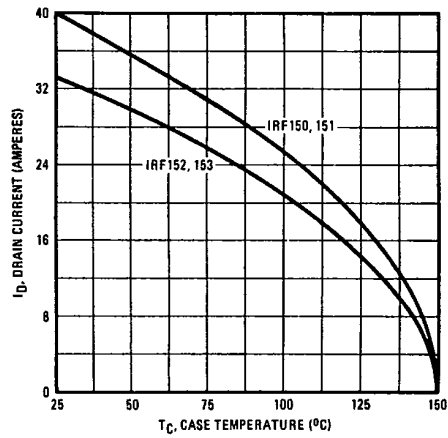


Fig. 13 - Maximum Drain Current Vs. Case Temperature

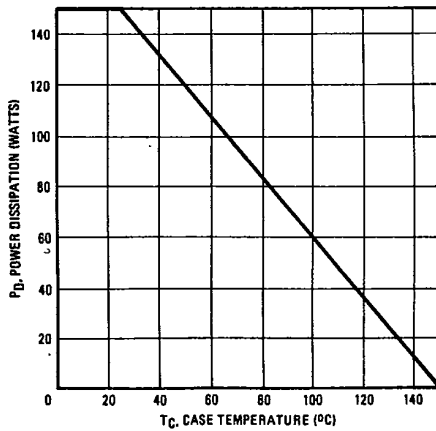


Fig. 14 - Power Vs. Temperature Derating Curve

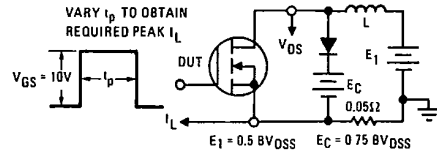


Fig. 15 - Clamped Inductive Test Circuit

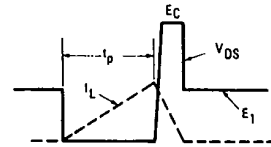


Fig. 16 - Clamped Inductive Waveforms

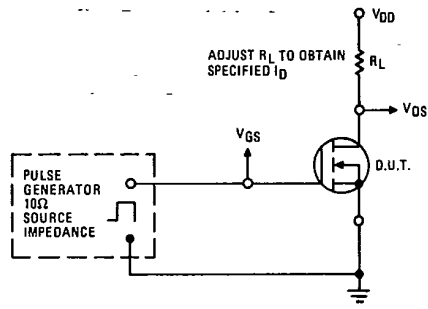


Fig. 17 - Switching Time Test Circuit

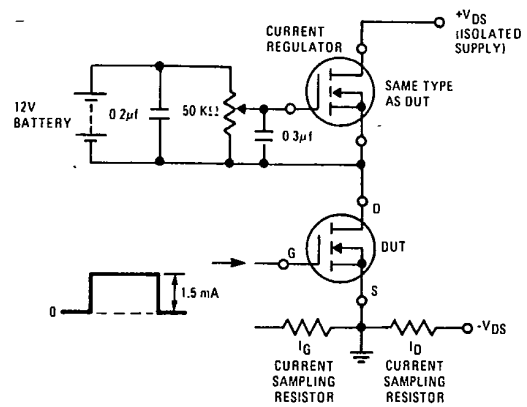


Fig. 18 - Gate Charge Test Circuit