

3875081 G E SOLID STATE
Standard Power MOSFETs

01E 18309 DT-39-13

IRF350, IRF351, IRF352, IRF353
Power MOS Field-Effect Transistors
File Number **1826**
N-Channel Enhancement-Mode
Power Field-Effect Transistors

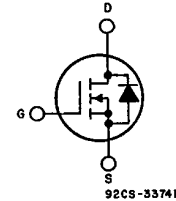
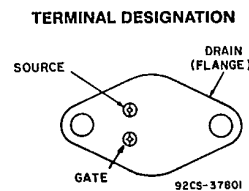
13 A and 15 A, 350 V - 400 V
 $r_{DS(on)} = 0.3 \Omega$ and 0.4Ω

Features:

- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance
- Majority carrier device

The IRF350, IRF351, IRF352 and IRF353 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA metal package.

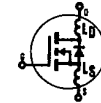
N-CHANNEL ENHANCEMENT MODE**TERMINAL DIAGRAM****JEDEC TO-204AA****Absolute Maximum Ratings**

Parameter	IRF350	IRF351	IRF352	IRF353	Units
V_{DS} Drain - Source Voltage ①	400	350	400	350	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 20 \text{ k}\Omega$) ①	400	350	400	350	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	15	15	13	13	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_{DM} Pulsed Drain Current ③	60	60	52	52	A
V_{GS} Gate - Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	150 (See Fig. 14)				W
Linear Derating Factor	1.2 (See Fig. 14)				W/K
I_{LM} Inductive Current, Clamped	(See Fig. 15 and 16) $L = 100 \mu\text{H}$				A
	60	60	52	52	
T_J Operating Junction and T_{stg} Storage Temperature Range	-55 to 150				$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

IRF350, IRF351, IRF352, IRF353

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS} Drain-Source Breakdown Voltage	IRF350 IRF352	400	—	—	V	V _{GS} = 0V I _D = 250μA
	IRF351 IRF353	350	—	—	V	
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{GSS} Gate-Source Leakage Forward	ALL	—	—	100	nA	V _{GS} = 20V
I _{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100	nA	V _{GS} = -20V
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C
I _{D(on)} On-State Drain Current ②	IRF350 IRF351	15	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V
	IRF352 IRF353	13	—	—	A	
R _{DS(on)} Static Drain-Source On-State Resistance ②	IRF350 IRF351	—	0.25	0.3	Ω	V _{GS} = 10V, I _D = 8.0A
	IRF352 IRF353	—	0.3	0.4	Ω	
g _{fs} Forward Transconductance ②	ALL	8.0	10	—	S (Ω)	V _{DS} > I _{D(on)} × R _{DS(on)} max., I _D = 8.0A
C _{iss} Input Capacitance	ALL	—	2000	3000	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 10
C _{oss} Output Capacitance	ALL	—	400	600	pF	
C _{rss} Reverse Transfer Capacitance	ALL	—	100	200	pF	V _{DD} = 180V, I _D = 8.0A, Z _o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t _{d(on)} Turn-On Delay Time	ALL	—	—	35	ns	
t _r Rise Time	ALL	—	—	65	ns	
t _{d(off)} Turn-Off Delay Time	ALL	—	—	150	ns	
t _f Fall Time	ALL	—	—	75	ns	V _{GS} = 10V, I _D = 18A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	79	120	nC	
Q _{gs} Gate-Source Charge	ALL	—	38	—	nC	
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	41	—	nC	
L _D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L _S Internal Source Inductance	ALL	—	12.5	—	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.



Thermal Resistance

R _{thJC} Junction-to-Case	ALL	—	—	0.83	K/W	
R _{thCS} Case-to-Sink	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	—	—	30	K/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I _S Continuous Source Current (Body Diode)	IRF350 IRF351	—	—	15	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
	IRF352 IRF353	—	—	13	A	
I _{SM} Pulse Source Current (Body Diode) ③	IRF350 IRF351	—	—	60	A	T _C = 25°C, I _S = 15A, V _{GS} = 0V
	IRF352 IRF353	—	—	52	A	
V _{SD} Diode Forward Voltage ②	IRF350 IRF351	—	—	1.6	V	T _C = 25°C, I _S = 13A, V _{GS} = 0V
	IRF352 IRF353	—	—	1.5	V	T _C = 25°C, I _S = 13A, V _{GS} = 0V
t _{rr} Reverse Recovery Time	ALL	—	1000	—	ns	T _J = 150°C, I _F = 15A, dI _F /dt = 100A/μs
Q _{RR} Reverse Recovered Charge	ALL	—	6.6	—	μC	T _J = 150°C, I _F = 15A, dI _F /dt = 100A/μs
t _{on} Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

① T_J = 25°C to 150°C.

② Pulse Test: Pulse width < 300μs, Duty Cycle < 2%.

③ Repetitive Rating: Pulse width limited by max. junction temperature.
See Transient Thermal Impedance Curve (Fig. 5).

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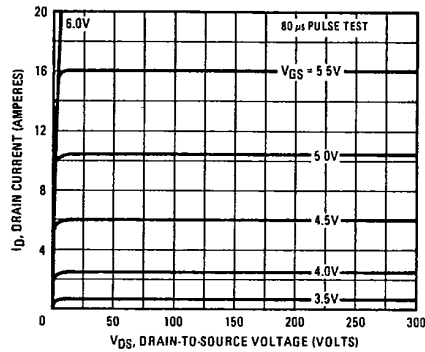


Fig. 1 - Typical Output Characteristics

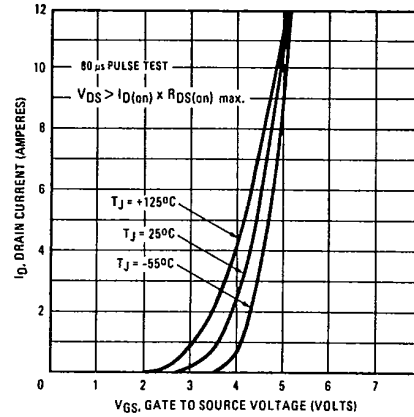


Fig. 2 - Typical Transfer Characteristics

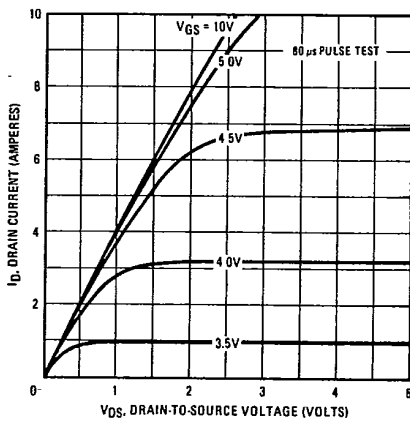


Fig. 3 - Typical Saturation Characteristics

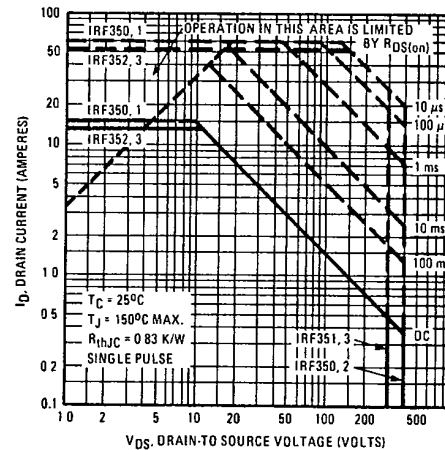


Fig. 4 - Maximum Safe Operating Area

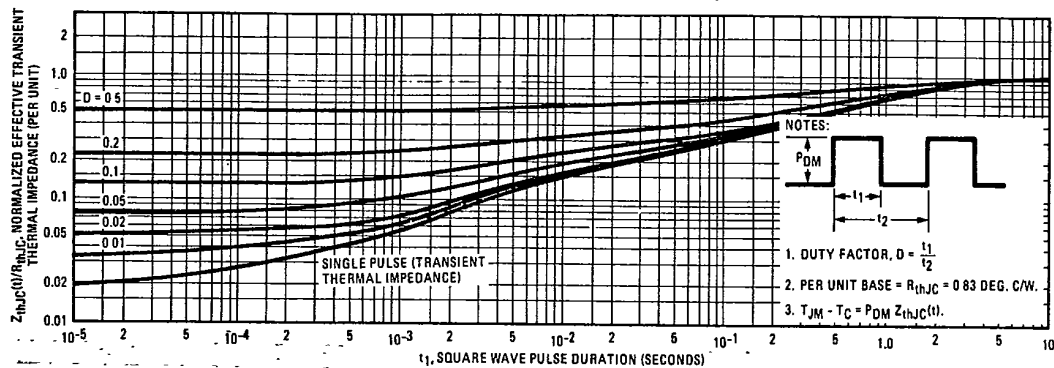


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF350, IRF351, IRF352, IRF353

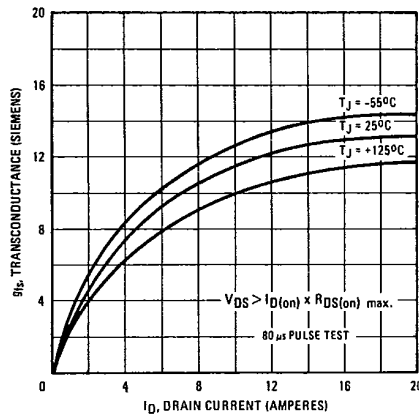


Fig. 6 - Typical Transconductance Vs. Drain Current

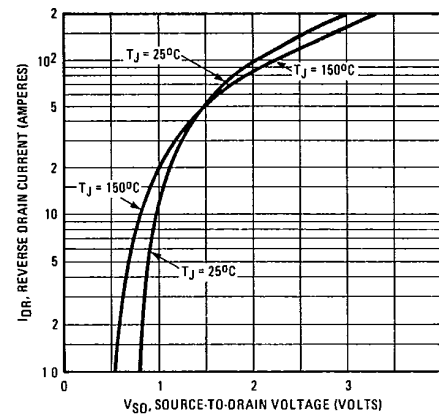


Fig. 7 - Typical Source-Drain Diode Forward Voltage

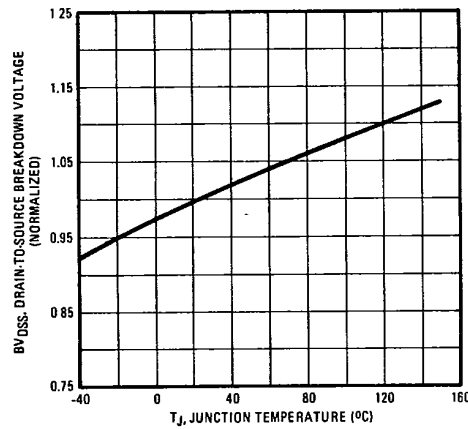


Fig. 8 - Breakdown Voltage Vs. Temperature

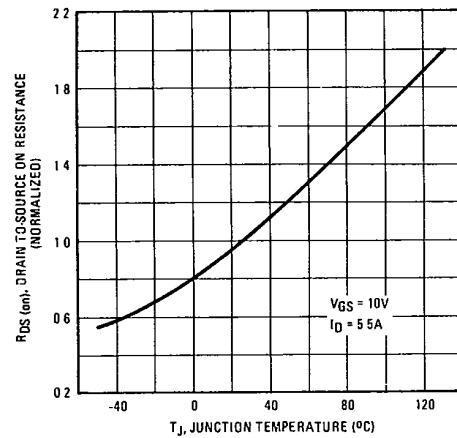


Fig. 9 - Normalized On-Resistance Vs. Temperature

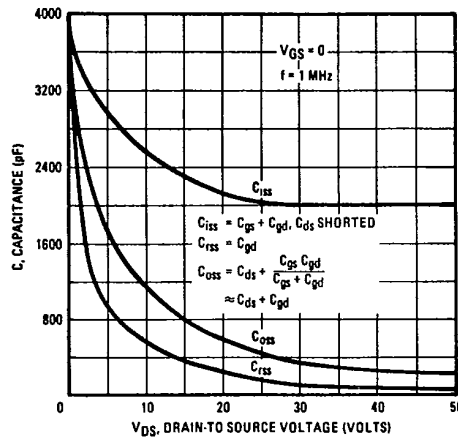


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

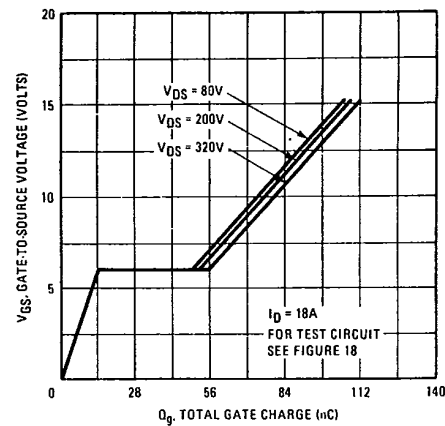


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

IRF350, IRF351, IRF352, IRF353

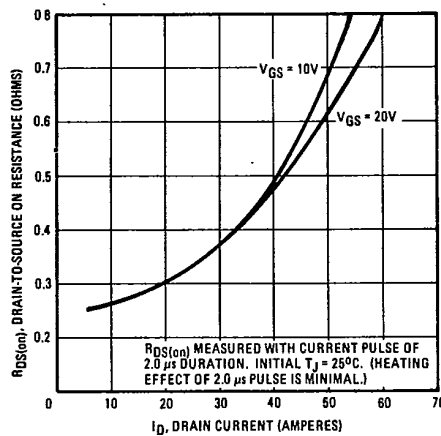


Fig. 12 - Typical On-Resistance Vs. Drain Current

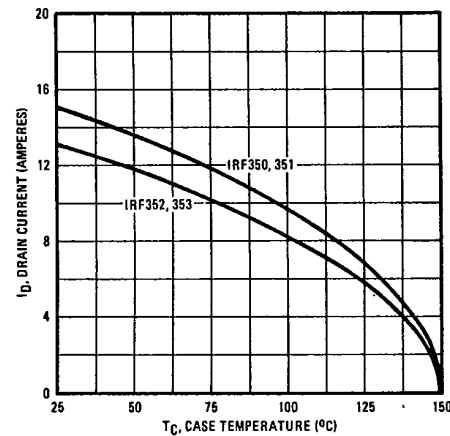


Fig. 13 - Maximum Drain Current Vs. Case Temperature

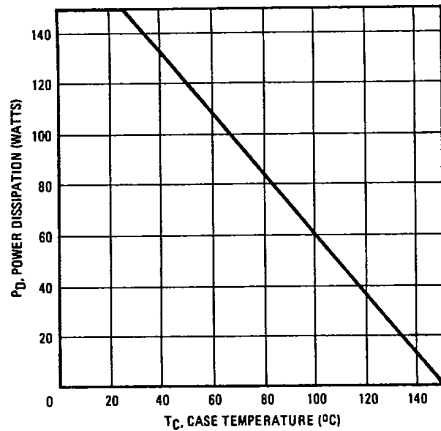


Fig. 14 - Power Vs. Temperature Derating Curve

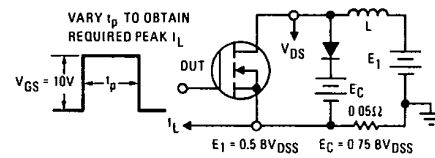


Fig. 15 - Clamped Inductive Test Circuit

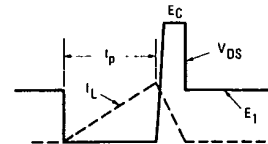


Fig. 16 - Clamped Inductive Waveforms

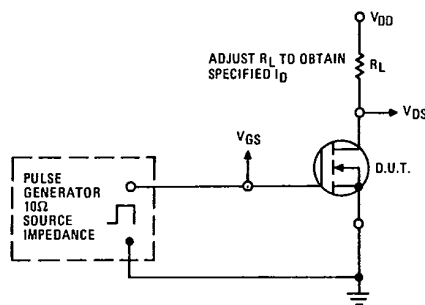


Fig. 17 - Switching Time Test Circuit

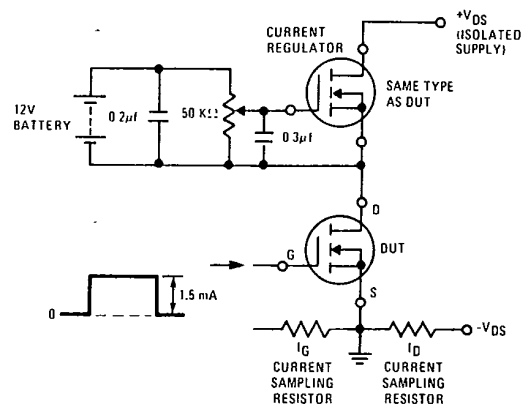


Fig. 18 - Gate Charge Test Circuit