

IRF620, IRF621, IRF622, IRF623

File Number 1577

Power MOS Field-Effect Transistors

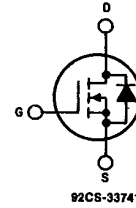
N-Channel Enhancement-Mode Power Field-Effect Transistors

4.0A and 5.0A, 150V-200V
 $r_{DS(on)} = 0.8 \Omega$ and 1.2Ω

Features:

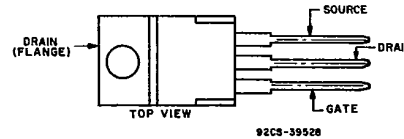
- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance
- Majority carrier device

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-220AB

The IRF620, IRF621, IRF622 and IRF623 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

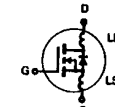
The IRF-types are supplied in the JEDEC TO-220AB plastic package.

Absolute Maximum Ratings

Parameter	IRF620	IRF621	IRF622	IRF623	Units
V_{DS} Drain - Source Voltage (1)	200	150	200	150	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 20 \text{ k}\Omega$) (1)	200	150	200	150	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	5.0	5.0	4.0	4.0	A
$I_D @ T_C = 100^\circ\text{C}$ Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM} Pulsed Drain Current (2)	20	20	16	16	A
V_{GS} Gate - Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	40 (See Fig 14)				W
Linear Derating Factor	0.32 (See Fig 14)				W/ $^\circ\text{C}$
I_{LM} Inductive Current, Clamped	20	20	16	16	A
T_J Operating Junction and Storage Temperature Range	-55 to 150				$^\circ\text{C}$
T_{Ltg} Lead Temperature	300 (0.063 in (1.6mm) from case for 10s)				$^\circ\text{C}$

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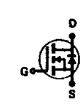
Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS} Drain-Source Breakdown Voltage	IRF620 IRF622	200	-	-	V	V _{GS} = 0V
	IRF621 IRF623	150	-	-	V	I _D = 250μA
	ALL	-	-	-	-	-
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	-	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{GSS} Gate-Source Leakage Forward	ALL	-	-	500	nA	V _{GS} = 20V
I _{GSS} Gate-Source Leakage Reverse	ALL	-	-	-500	nA	V _{GS} = -20V
I _{DSS} Zero Gate Voltage Drain Current	ALL	-	-	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V
	ALL	-	-	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C
I _{D(on)} On State Drain Current ②	IRF620 IRF621	5.0	-	-	A	V _{DS} > I _{D(on)} × R _{DS(on) max.} , V _{GS} = 10V
	IRF622 IRF623	4.0	-	-	A	
	ALL	-	-	-	-	
R _{DS(on)} Static Drain-Source On-State Resistance ②	IRF620 IRF621	-	0.5	0.8	Ω	V _{GS} = 10V, I _D = 2.5A
	IRF622 IRF623	-	0.8	1.2	Ω	
	ALL	-	-	-	-	
g _{fs} Forward Transconductance ②	ALL	1.3	2.5	-	S (Ω)	V _{DS} > I _{D(on)} × R _{DS(on) max.} , I _D = 2.5A
C _{iss} Input Capacitance	ALL	-	450	600	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz
C _{oss} Output Capacitance	ALL	-	150	300	pF	See Fig. 10
C _{rss} Reverse Transfer Capacitance	ALL	-	40	80	pF	See Fig. 10
t _{d(on)} Turn-On Delay Time	ALL	-	20	40	ns	V _{DD} = 2.5 BV _{DSS} , I _D = 2.5A, Z _o = 50Ω See Fig. 17
t _r Rise Time	ALL	-	30	60	ns	
t _{d(off)} Turn-Off Delay Time	ALL	-	60	100	ns	
t _f Fall Time*	ALL	-	30	60	ns	
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	-	11	15	nC	V _{GS} = 50V, I _D = 6.0A, V _{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q _{gs} Gate-Source Charge	ALL	-	6.0	-	nC	
Q _{gd} Gate-Drain ("Miller") Charge	ALL	-	6.0	-	nC	
L _D Internal Drain Inductance	ALL	-	3.5	-	nH	Measured from the contact screw on tab to center of die. Modified MOSFET symbol showing the internal device inductances. 
	ALL	-	4.5	-	nH	
L _S Internal Source Inductance	ALL	-	7.5	-	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad

Thermal Resistance

R _{thJC} Junction to Case	ALL	-	-	3 12	°C/W	
R _{thCS} Case to Sink	ALL	-	1.0	-	°C/W	Mounting surface flat, smooth, and greased.
R _{thJA} Junction-to-Ambient	ALL	-	-	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I _S Continuous Source Current (Body Diode)	IRF620 IRF621	-	-	5.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
	IRF622 IRF623	-	-	4.0	A	
I _{SM} Pulse Source Current (Body Diode) ③	IRF620 IRF621	-	-	20	A	
	IRF622 IRF623	-	-	16	A	
V _{SD} Diode Forward Voltage ②	IRF620 IRF621	-	-	1.8	V	T _C = 25°C, I _S = 5.0A, V _{GS} = 0V
	IRF622 IRF623	-	-	1.4	V	T _C = 25°C, I _S = 4.0A, V _{GS} = 0V
t _{rr} Reverse Recovery Time	ALL	-	350	-	ns	T _J = 150°C, I _F = 5.0A, di _F /dt = 100 A/μs
Q _{RR} Reverse Recovered Charge	ALL	-	2.3	-	μC	T _J = 150°C, I _F = 5.0A, di _F /dt = 100 A/μs
t _{on} Forward Turn-on Time	ALL	Intrinsic turn on time is negligible. Turn on speed is substantially controlled by L _S + L _D				

① T_J = 25°C to 150°C ② Pulse Test: Pulse width < 300μs, Duty Cycle < 2%. ③ Repetitive Rating Pulse width limited by max. junction temperature
See Transient Thermal Impedance Curve (Fig. 5)

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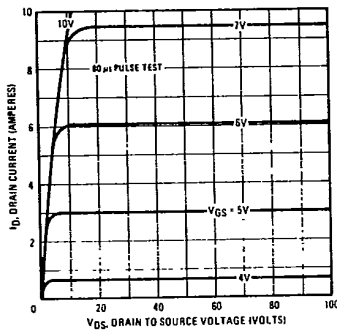


Fig. 1 - Typical Output Characteristics

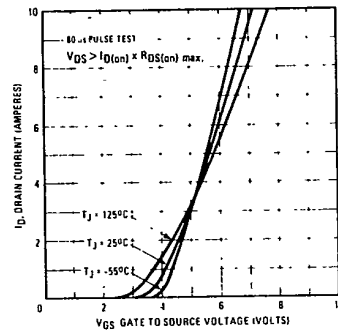


Fig. 2 - Typical Transfer Characteristics

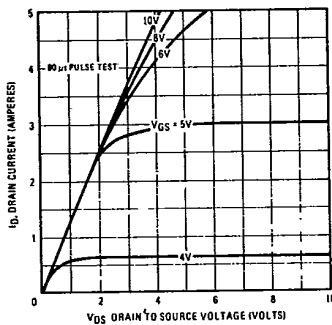


Fig. 3 - Typical Saturation Characteristics

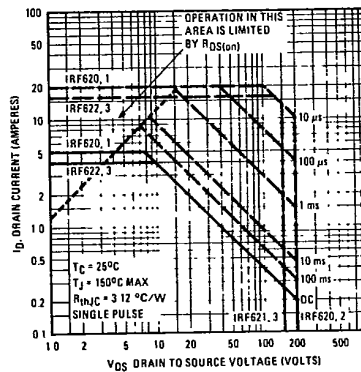


Fig. 4 - Maximum Safe Operating Area

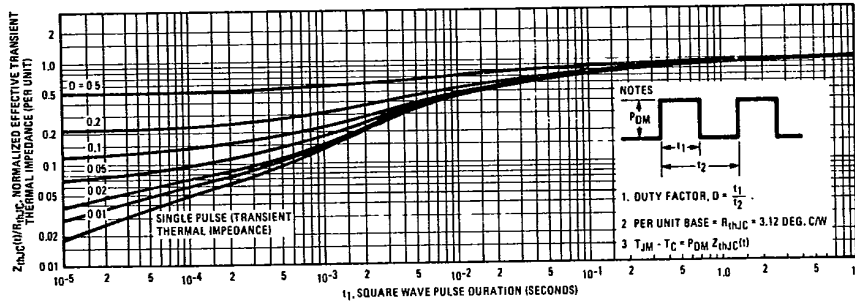


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

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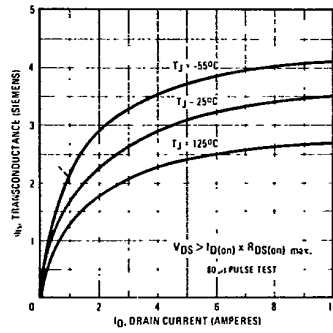


Fig. 6 - Typical Transconductance Vs. Drain Current

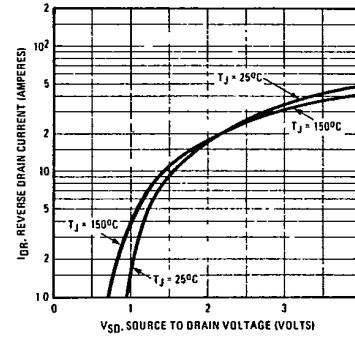


Fig. 7 - Typical Source-Drain Diode Forward Voltage

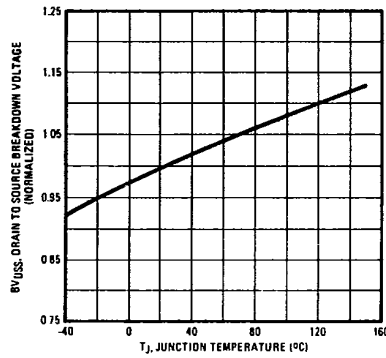


Fig. 8 - Breakdown Voltage Vs. Temperature

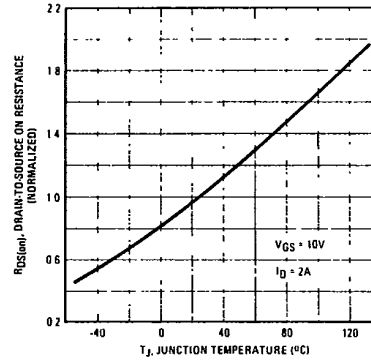


Fig. 9 - Normalized On-Resistance Vs. Temperature

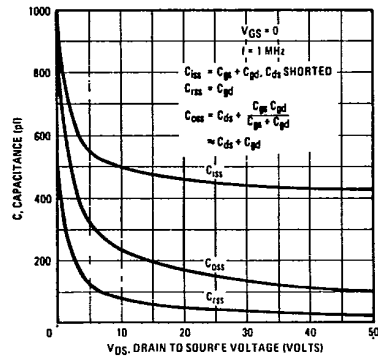


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

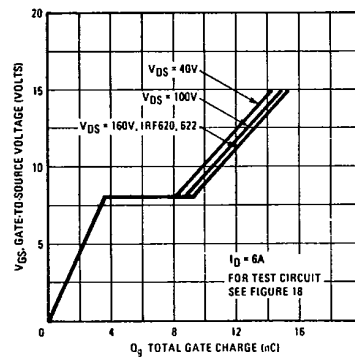


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

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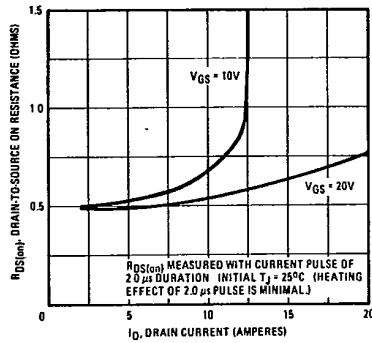


Fig. 12 - Typical On-Resistance Vs. Drain Current

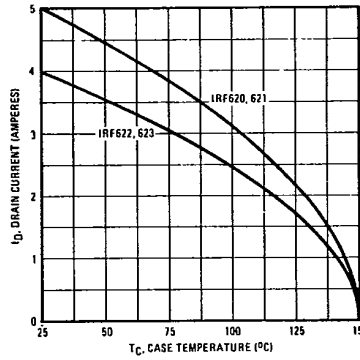


Fig. 13 - Maximum Drain Current Vs. Case Temperature

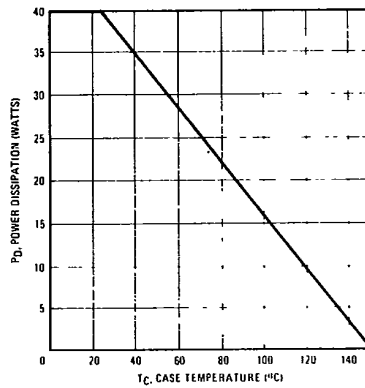


Fig. 14 - Power Vs. Temperature Derating Curve

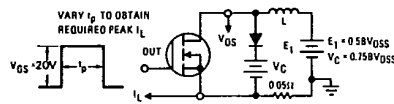


Fig. 15 - Clamped Inductive Test Circuit

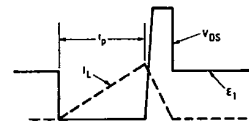


Fig. 16 - Clamped Inductive Waveforms

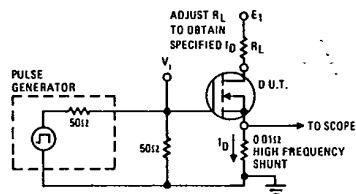


Fig. 17 - Switching Time Test Circuit

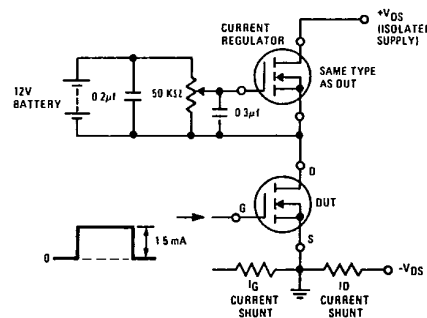


Fig. 18 - Gate Charge Test Circuit