Description

The GM71C4256B/BL is the new generation dynamic RAM organized 262,144 x 4 bit. GM71C4256B/BL has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71C4256B/BL offers Fast Page Mode as a high speed access mode. Multiplexed address inputs permit the GM71C4256B/BL to be packaged in a standard 20 pin DIP, SOJ and ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

Features

- 262,144 Words x 4 Bit Organization
- Fast Page Mode Capability
- Single Power Supply (5V ± 10%)
- Fast Access Time & Cycle Time

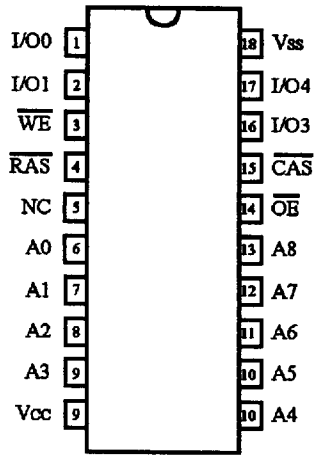
(Unit: ns)

	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
GM71C4256B/BL-60	60	20	120	45
GM71C4256B/BL-70	70	20	130	50
GM71C4256B/BL-80	80	25	160	55

- Low Power
  Active : 495/440/385mW (MAX)
  Standby : 5.5mW (CMOS level : MAX)
  1.1mW (L-series)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 512 Refresh Cycles/8ms
- 512 Refresh Cycles/64ms (L-series)
- Battery Back Up Operation (L-series)

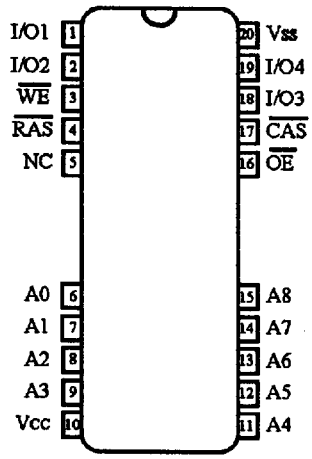
Pin Configuration

20 DIP



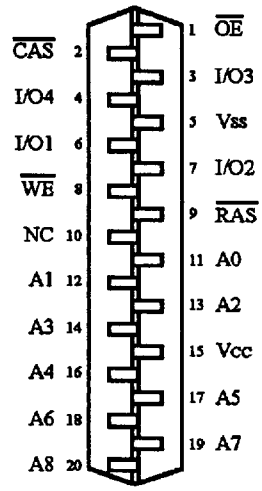
(Top View)

20 (26) SOJ



(Top View)

20 ZIP



(Bottom View)

Pin Description

Pin	Function	Pin	Function
A0-A8	Address Inputs	I/O1-I/O4	Data Input/Output
$\overline{RAS}$	Row Address Strobe	Vcc	Power (+5V)
$\overline{CAS}$	Column Address Strobe	Vss	Ground
$\overline{WE}$	Read/Write Enable	NC	No Connection
$\overline{OE}$	Output Enable		

Ordering Information

Type No.	Access Time	Package
GM71C4256B/BL-60 GM71C4256B/BL-70 GM71C4256B/BL-80	60ns 70ns 80ns	300 Mil 20 Pin Plastic DIP
GM71C4256BJ/BLJ-60 GM71C4256BJ/BLJ-70 GM71C4256BJ/BLJ-80	60ns 70ns 80ns	300 Mil 20 (26) Pin Plastic SOJ
GM71C4256BZ/BLZ-60 GM71C4256BZ/BLZ-70 GM71C4256BZ/BLZ-80	60ns 70ns 80ns	400 Mil 20 Pin Plastic ZIP

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	℃
T_{STG}	Storage Temperature (Plastic)	-55 ~ 125	℃
V_{IN}/V_{OUT}	Voltage on any Pin Relative to Vss	-1.0 ~ 7.0	V
V_{CC}	Voltage on Vcc Relative to Vss	-1.0 ~ 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.0	W

*Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended DC Operating Conditions (T_A = 0 ~ 70℃)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	6.5	V
V_{IL}	Input Low Voltage (I/O Pin)	-1.0	-	0.8	V
V_{IL}	Input Low Voltage (Others)	-2.0	-	0.8	V

DC Electrical Characteristics ($V_{CC} = 5V \pm 10\%$, $T_A = 0 \sim 70℃$)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = -5mA)		2.4	Vcc	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	60ns	-	90	mA	1, 2
		70ns	-	80		
		80ns	-	70		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$= V_{IH}, D_{OUT} = High-Z)		-	2	mA	
I_{CC3}	$\overline{RAS}$-Only Refresh Current Average Power Supply Current $\overline{RAS}$-Only Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	60ns	-	90	mA	2
		70ns	-	80		
		80ns	-	70		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	60ns	-	80	mA	1, 3
		70ns	-	70		
		80ns	-	60		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = Vcc - 0.2V)		-	1	mA	
			-	200	μA	5
I_{CC6}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	60ns	-	80	mA	
		70ns	-	70		
		80ns	-	70		
I_{CC7}	Battery Back Up Current (Standby with CBR Refresh) (t_{RC}=125us, $t_{RAS} \leq$ 1us, $\overline{WE}$=V_{IH}, $\overline{CAS}$=V_{IL}, $\overline{OE}$, Address and D_{IN}=V_{IH} orV_{IL}, D_{OUT}=High-Z)		-	300	μA	4, 5
I_{CC8}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		-	5	mA	1
$I_{I(L)}$	Input Leakage Current Any Input ($0V \leq V_{IN} \leq 7V$)		-10	10	μA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, $0V \leq V_{OUT} \leq 7V$)		-10	10	μA	

Note: 1. Icc depends on output load condition when the device is selected. Icc(max) is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. L Series.
5. t_{RAS}(max) = 1μs is applied to refresh of battery back up.

Capacitance ($V_{CC} = 5V \pm 10\%$, $T_A = 25℃$)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address, D_{IN})	-	5	pF	1
C_{I2}	Input Capacitance (Clocks)	-	7	pF	1
C_O	Output Capacitance (Data-In/Out)	-	10	pF	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

AC Characteristics($V_{CC} = 5V \pm 10\%$, $T_A = 0 \sim 70℃$, Notes 1, 14)

Test Conditions
Input rise and fall times: 5ns
Input timing reference levels: 0.8V, 2.4V
Output load : 2 TTL gate + C_L (100pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71C4256 B/BL-60		GM71C4256 B/BL-70		GM71C4256 B/BL-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	120	-	130	-	160	-	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	-	50	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{ASR}	Row Address Set-up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	12	-	ns	
t_{ASC}	Column Address Set-up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	20	-	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	22	55	ns	8
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	17	40	ns	9
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	80	-	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	20	-	20	-	20	-	ns	
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	0	-	0	-	0	-	ns	
t_{DZC}	$\overline{CAS}$ Dealy Time from D_{IN}	0	-	0	-	0	-	ns	
t_T	TransitionTime (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
	Refresh Period (L-Series)	-	64	-	64	-	64	ms	

Read Cycle

Symbol	Parameter	GM71C4256 B/BL-60		GM71C4256 B/BL-70		GM71C4256 B/BL-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	2, 3
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	-	25	ns	3, 4
t_{AA}	Access Time from Address	-	30	-	35	-	40	ns	3, 5
t_{OAC}	Access Time from $\overline{OE}$	-	20	-	20	-	25	ns	
t_{RCS}	Read Command Setup Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	-	0	-	0	-	ns	
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	10	-	10	-	10	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	40	-	ns	
t_{OFF1}	Output Buffer Turn-off Time	0	20	0	20	0	20	ns	6
t_{OFF2}	Output Buffer Turn-off Time from $\overline{OE}$	0	20	0	20	0	20	ns	6
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	-	20	-	20	-	ns	

Write Cycle

Symbol	Parameter	GM71C4256 B/BL-60		GM71C4256 B/BL-70		GM71C4256 B/BL-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Setup Time	0	-	0	-	0	-	ns	10
t_{WCH}	Write Command Hold Time	15	-	15	-	20	-	ns	
t_{WP}	Write Command Pulse Width	10	-	10	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{DS}	Data-in Setup Time	0	-	0	-	0	-	ns	11
t_{DH}	Data-in Hold Time	15	-	15	-	20	-	ns	11

Read-Modify-Write Cycle

Symbol	Parameter	GM71C4256 B/BL-60		GM71C4256 B/BL-70		GM71C4256 B/BL-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RWC}	Read-Write Cycle Time	170	-	180	-	220	-	ns	
t_{RWD}	RAS to WE Delay Time	85	-	95	-	110	-	ns	10
t_{CWD}	CAS to WE Delay Time	45	-	45	-	55	-	ns	10
t_{AWD}	Column Address to WE Delay Time	55	-	60	-	70	-	ns	10
t_{OEH}	OE Hold Time from WE	20	-	20	-	25	-	ns	

Refresh Cycle

Symbol	Parameter	GM71C4256 B/BL-60		GM71C4256 B/BL-70		GM71C4256 B/BL-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	15	-	15	-	20	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	-	10	-	10	-	ns	

Fast Page Mode Cycle

Symbol	Parameter	GM71C4256 B/BL-60		GM71C4256 B/BL-70		GM71C4256 B/BL-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	-	50	-	55	-	ns	
t_{CP}	Fast Page Mode $\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{RASC}	Fast Page Mode $\overline{RAS}$ Pulse Width	-	100,000	-	100,000	-	100,000	ns	12
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	-	40	-	45	-	50	ns	13
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	-	45	-	50	-	ns	

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	GM71C4256 B/BL-60		GM71C4256 B/BL-70		GM71C4256 B/BL-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	95	-	100	-	110	-	ns	

Notes:

1. AC Measurements assume $t_T = 5$ns.
2. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
5. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
6. $t_{OFF}(max)$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the $t_{RCD}(max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RCD}(max)$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(max)$ limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RAD}(max)$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only if $t_{WCS} \geq t_{WCS}(min)$ the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(min)$, $t_{CWD} \geq t_{CWD}(min)$, $t_{AWD} \geq t_{AWD}(min)$ and $t_{CPW} \geq t_{CPW}(min)$, the cycle is a read modify write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or Read-Modify-Write cycles.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If the internal refresh counter is used, a minimum of eitht $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

Timing Waveforms

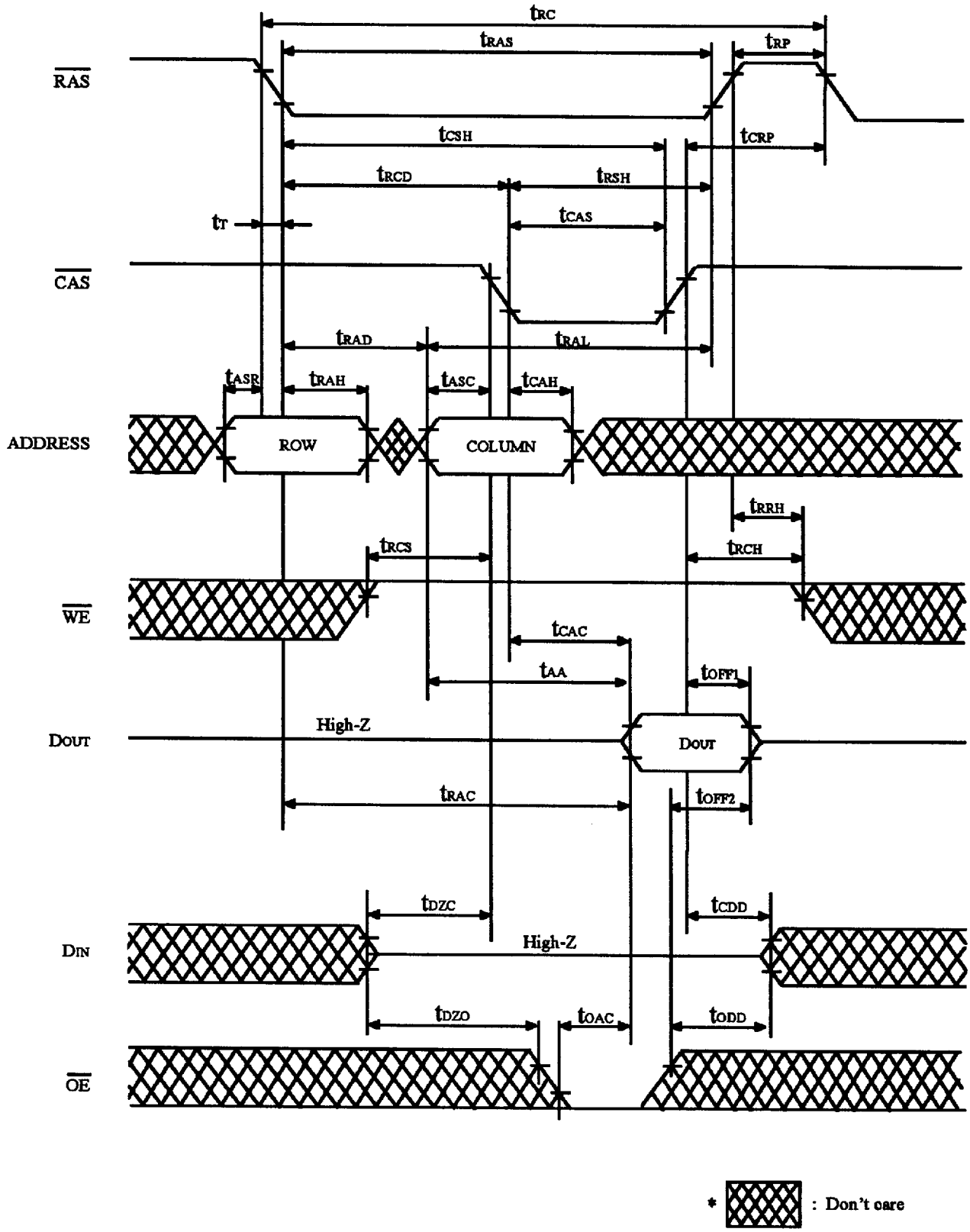


FIGURE 1. READ CYCLE

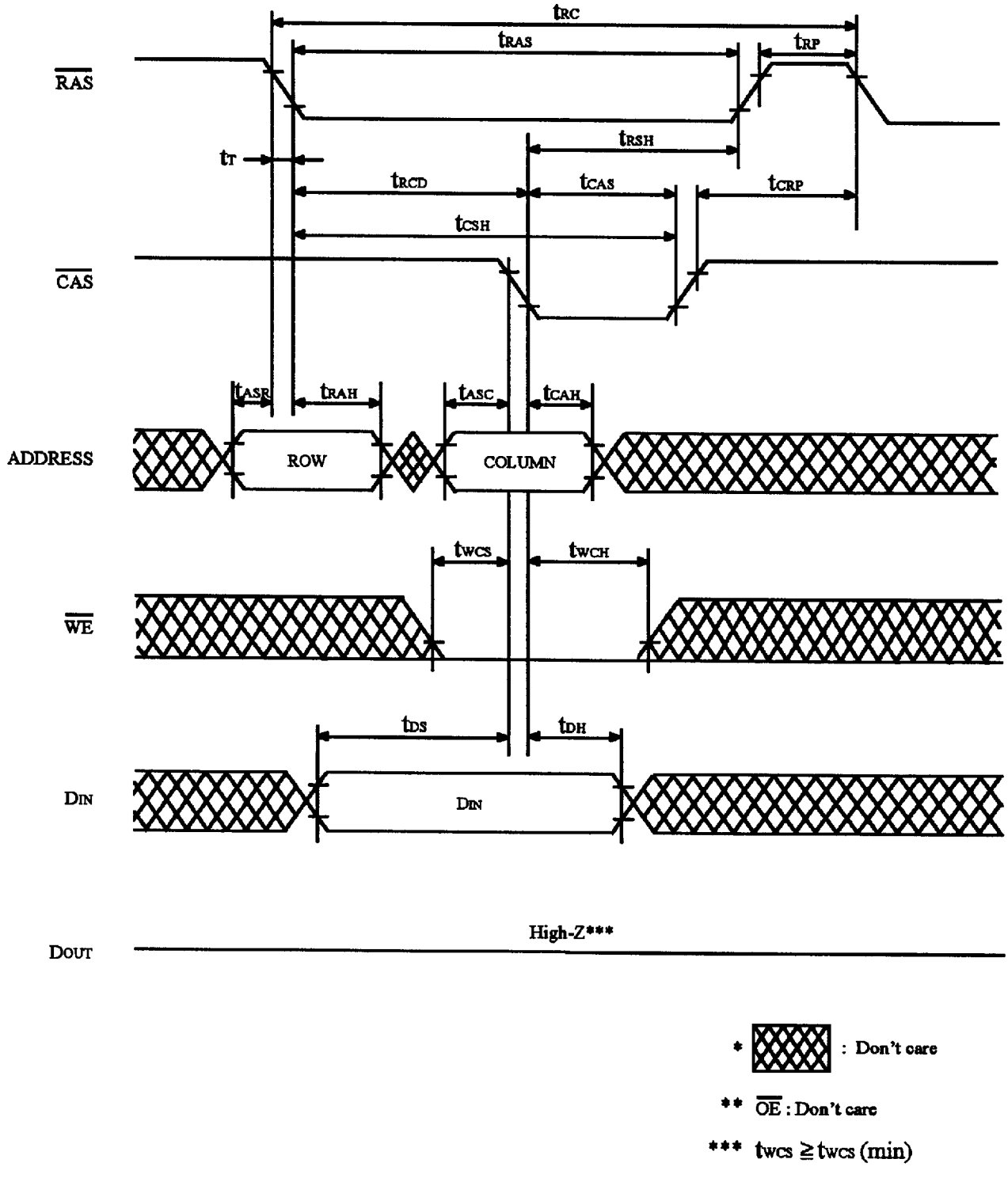


FIGURE 2. EARLY WRITE CYCLE

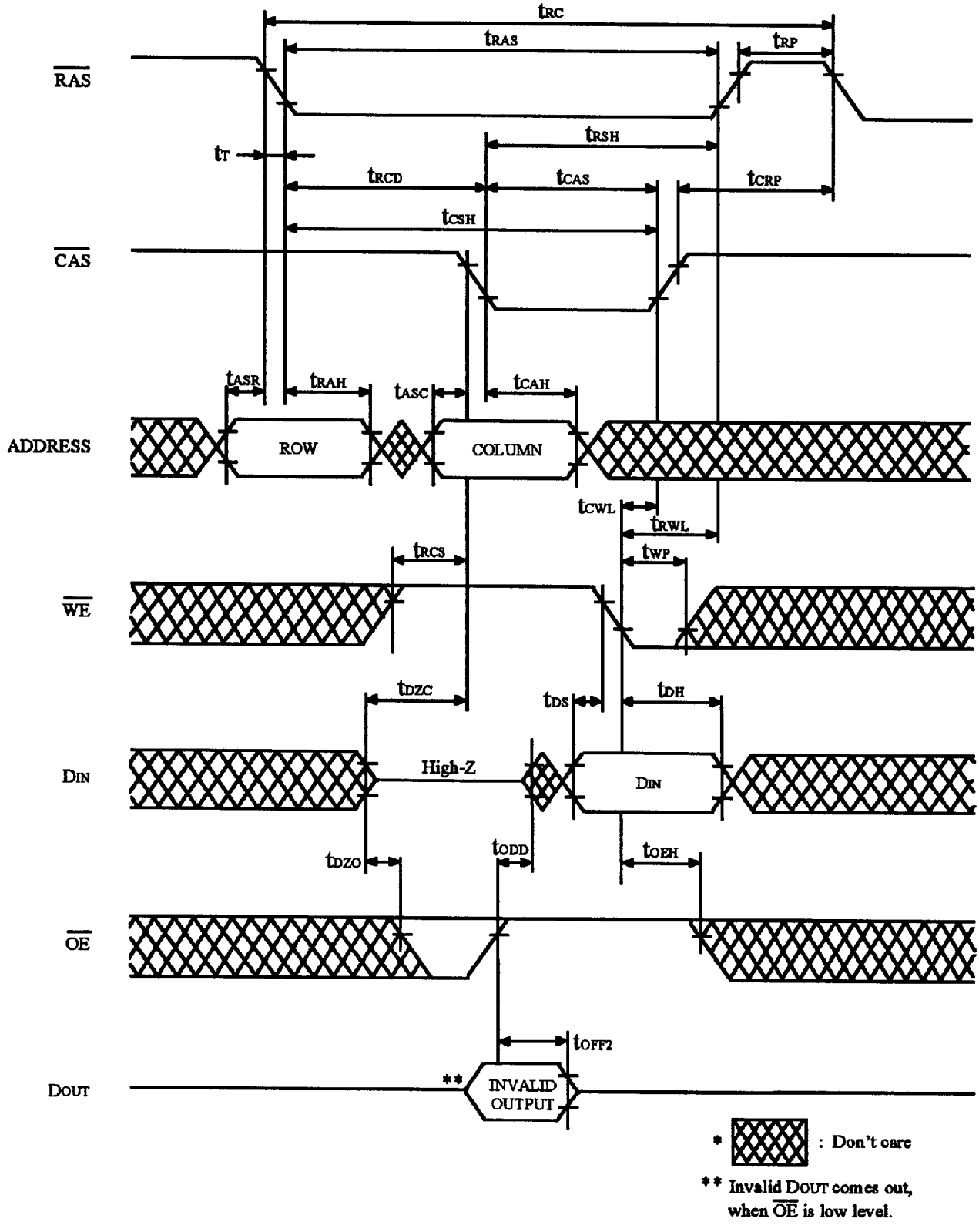


FIGURE 3. DELAYED WRITE CYCLE*18

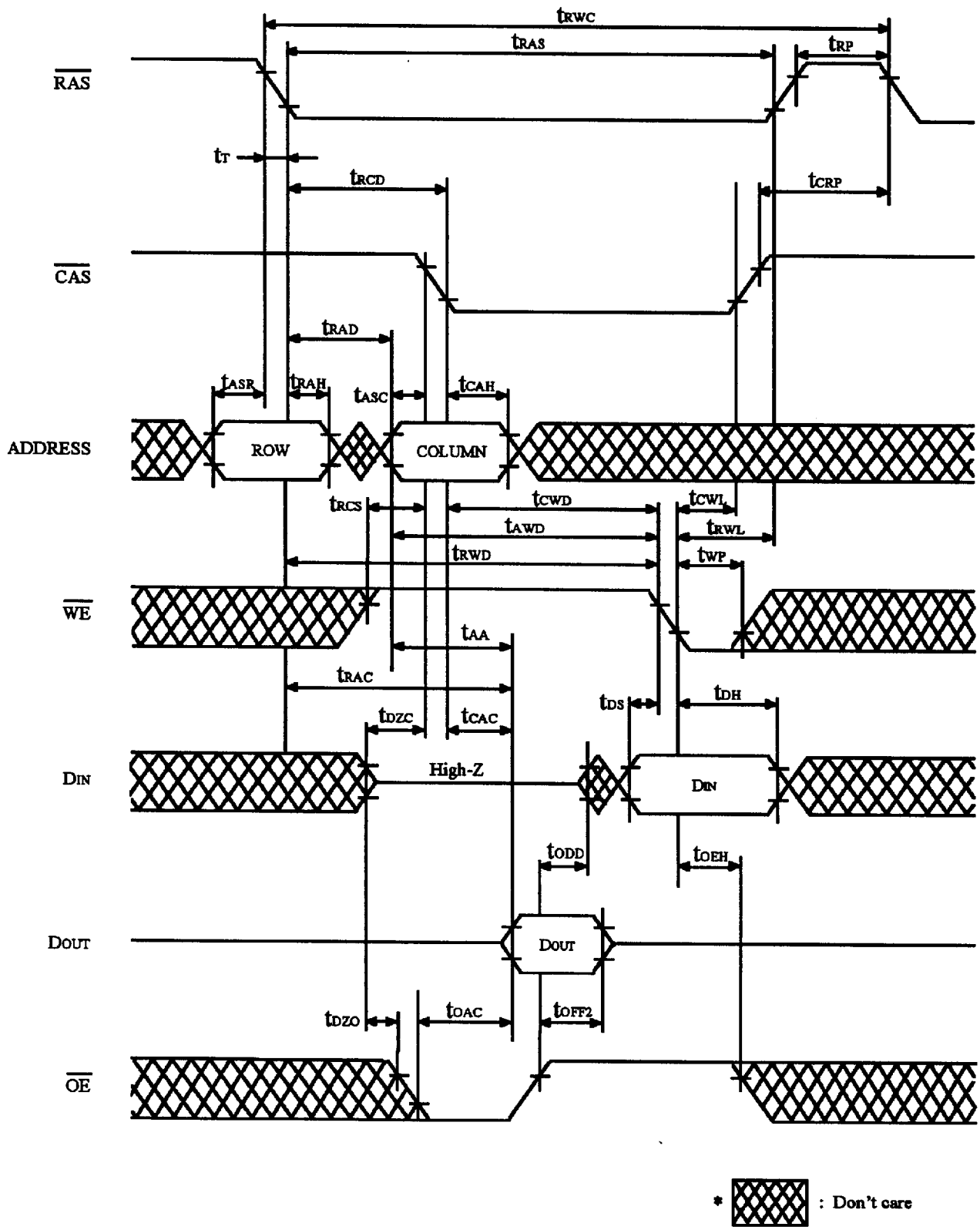
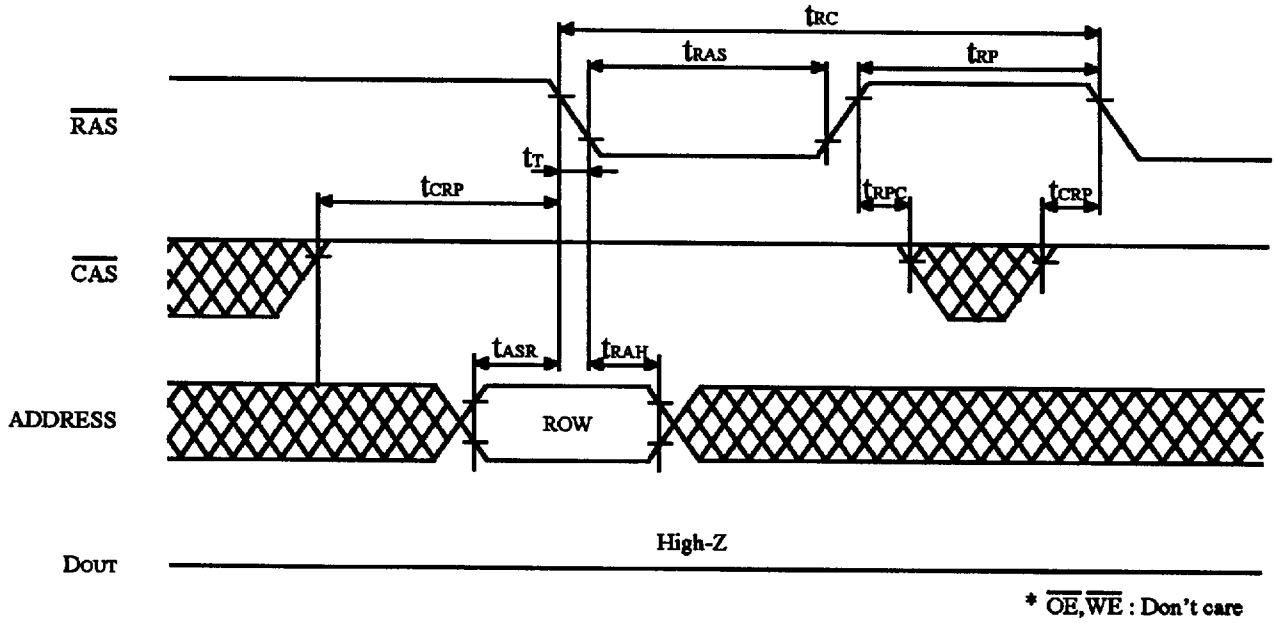


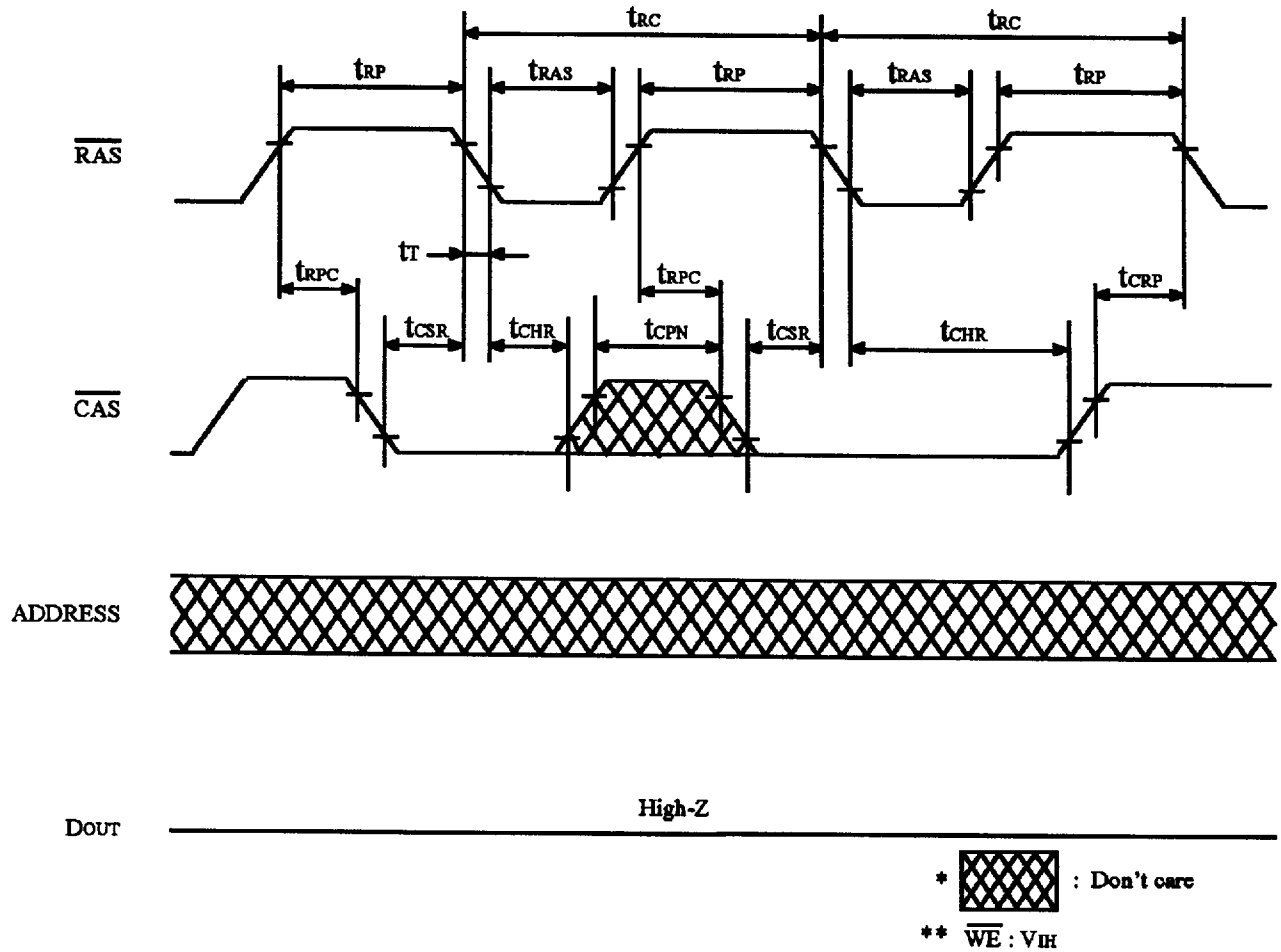
FIGURE 4. READ MODIFY WRITE CYCLE



* $\overline{OE}$,$\overline{WE}$: Don't care

FIGURE 5. $\overline{RAS}$ ONLY REFRESH CYCLE

** Rrfresh address : A0~A9



* : Don't care

** $\overline{WE}$: V_{IH}

FIGURE 6. $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

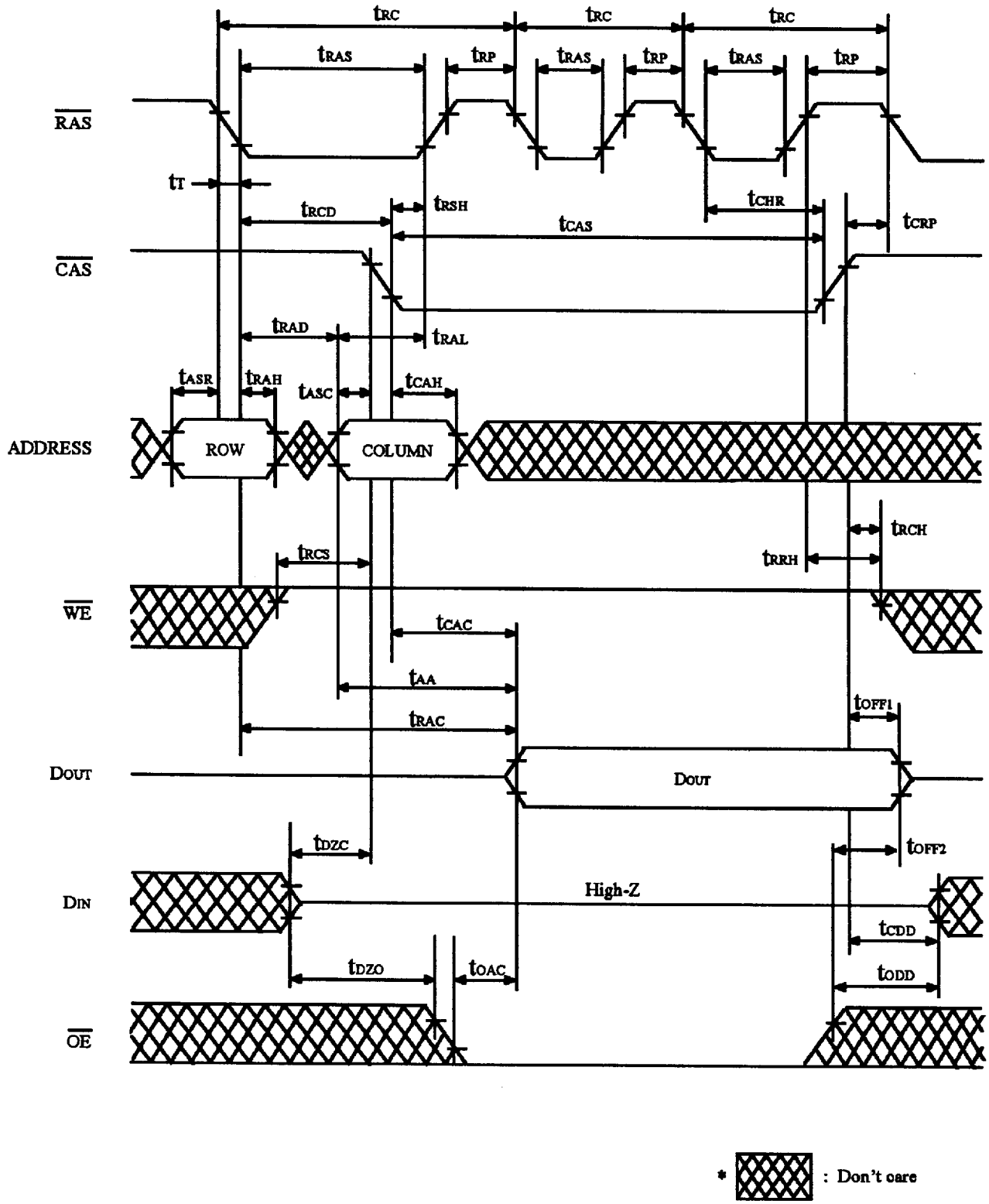


FIGURE 7. HIDDEN REFRESH CYCLE

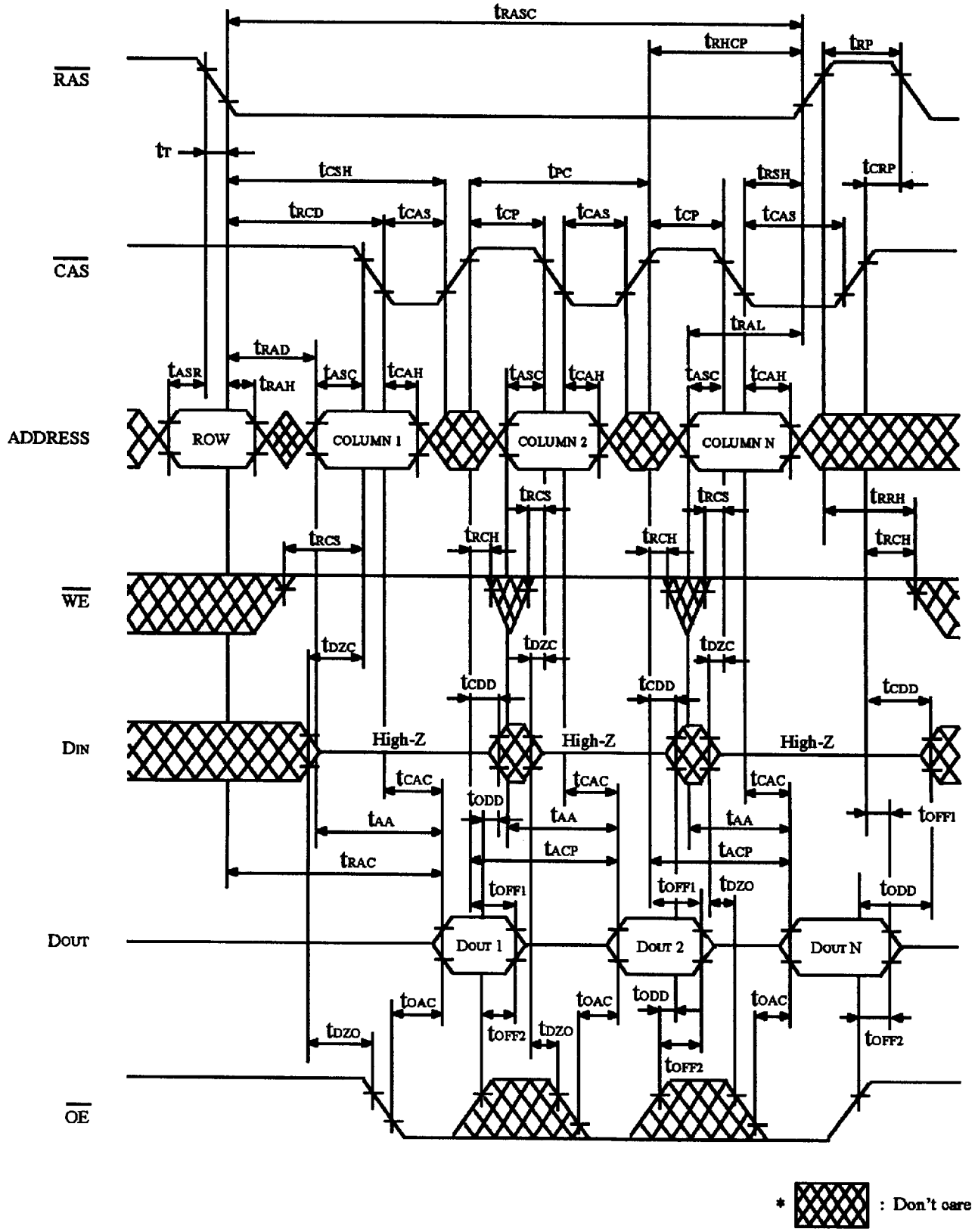


FIGURE 8. FAST PAGE MODE READ CYCLE

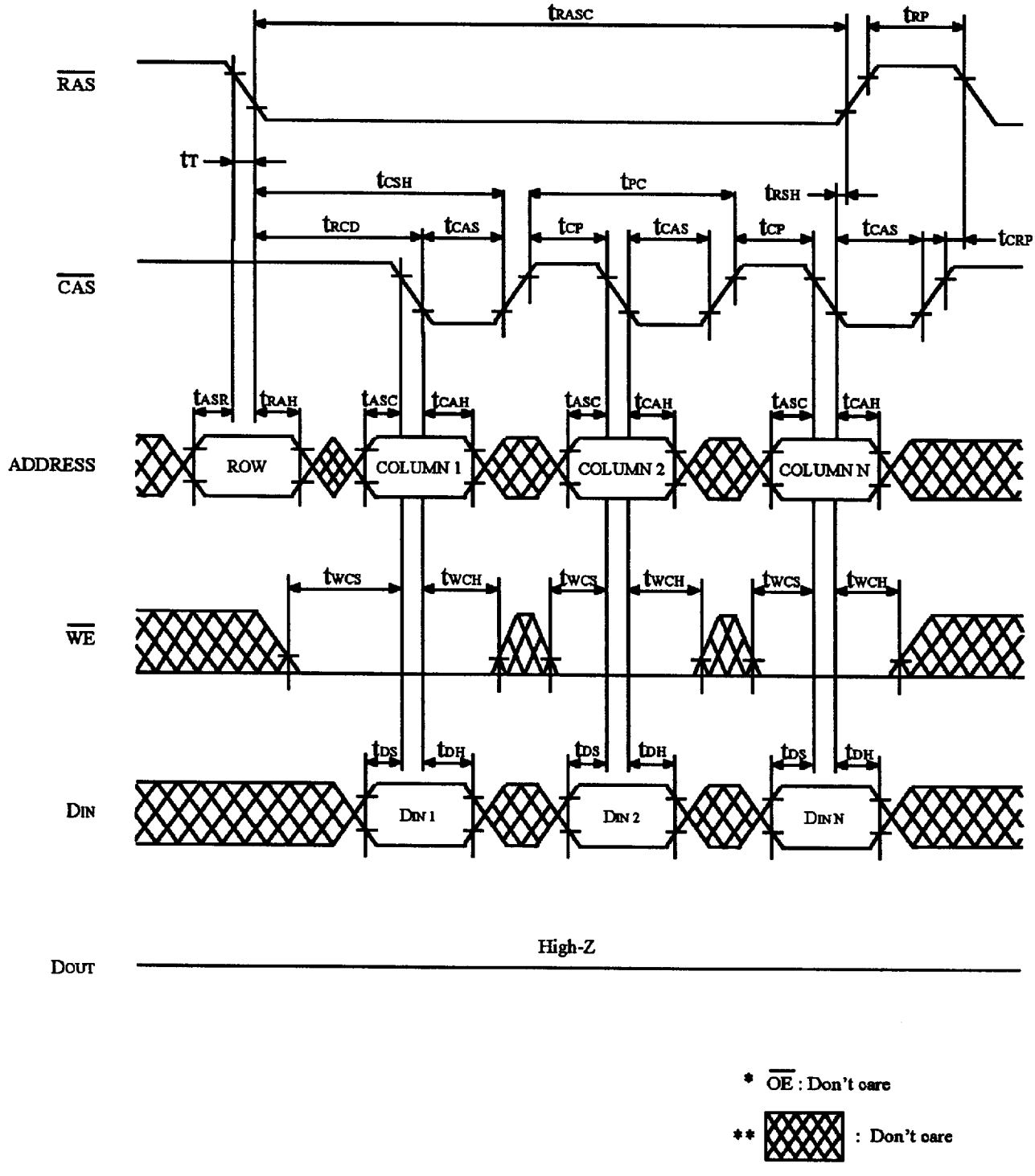


FIGURE 9. FAST PAGE MODE EARLY WRITE CYCLE

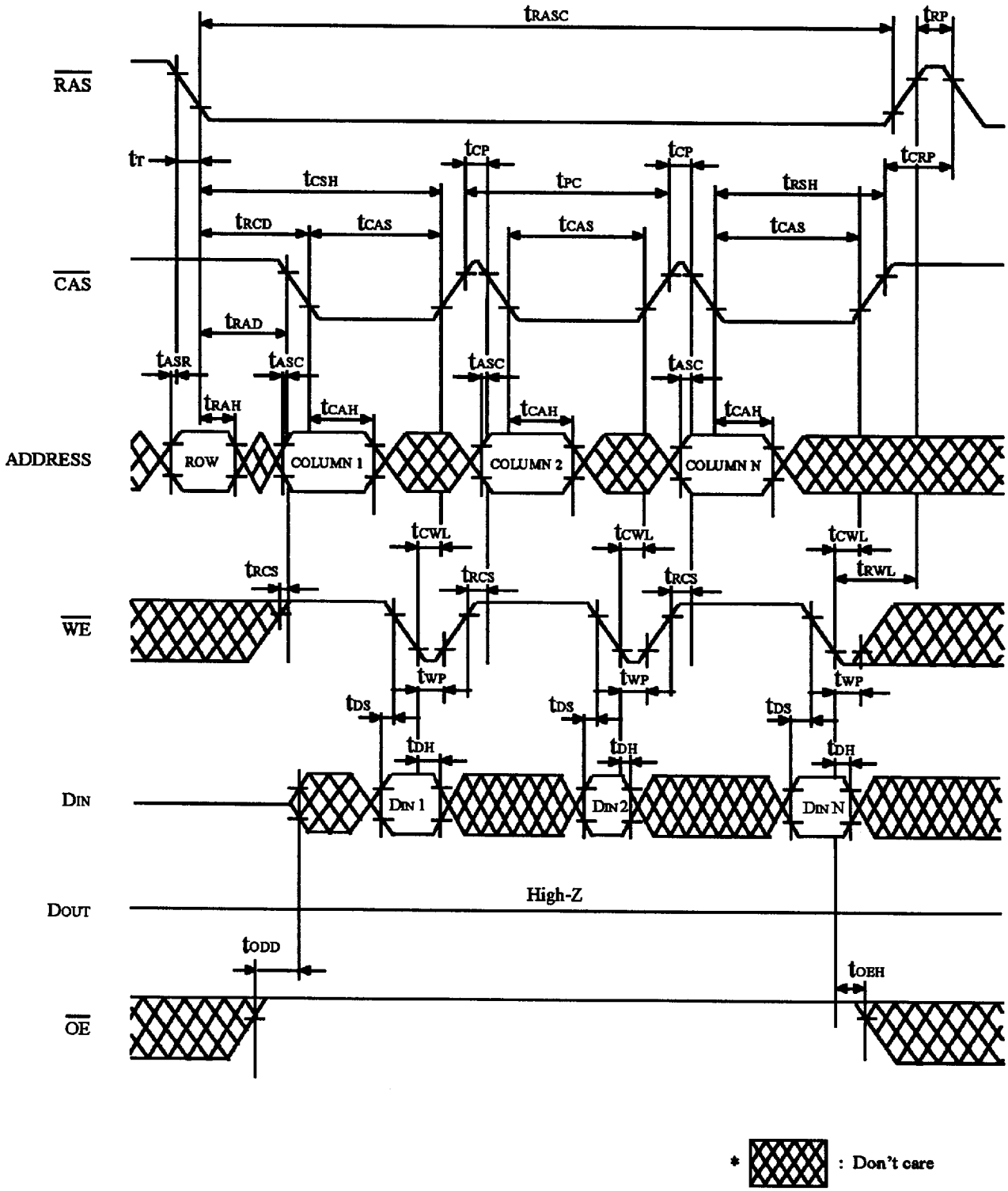


FIGURE 10. FAST PAGE MODE DELAYED WRITE CYCLE

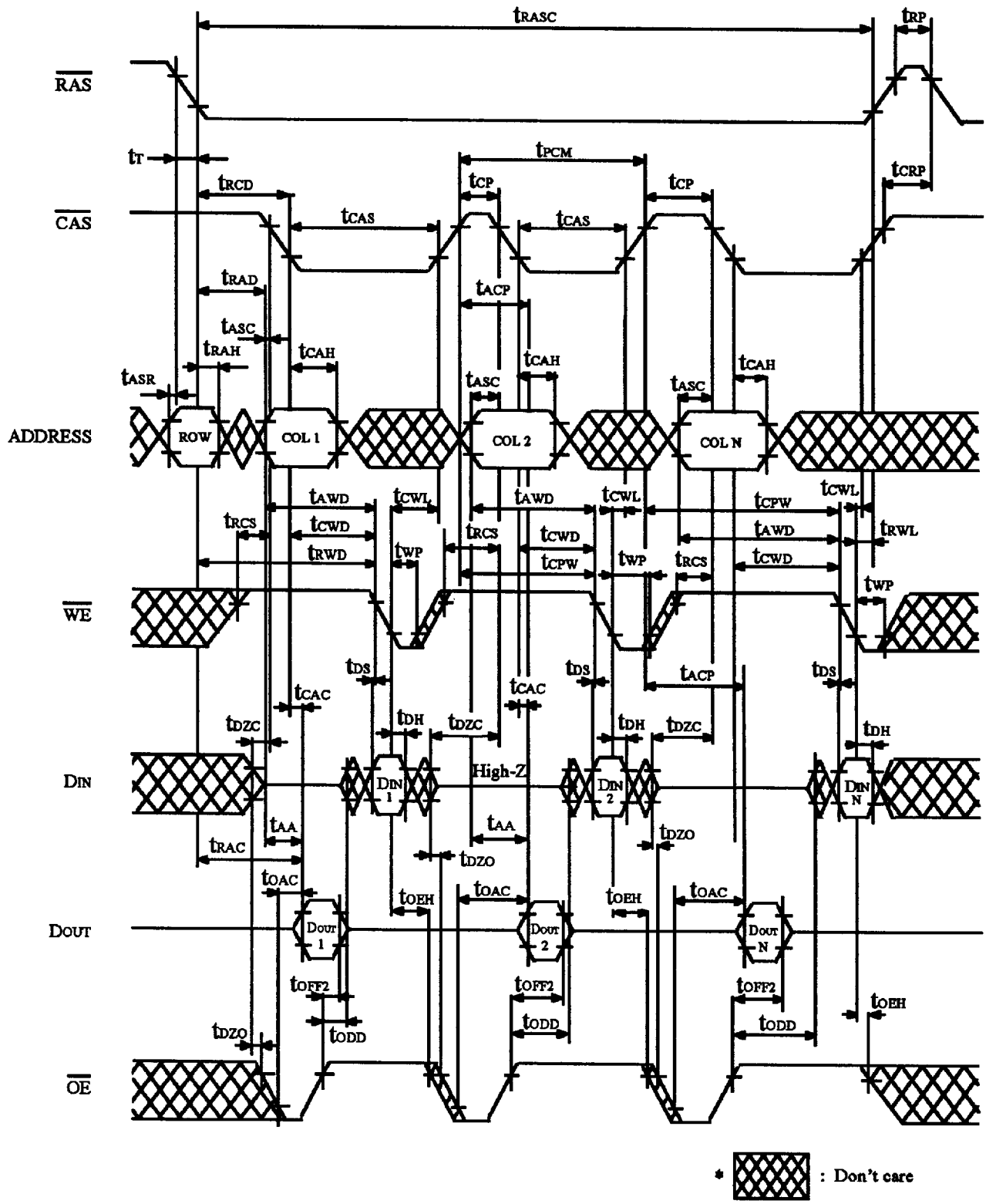
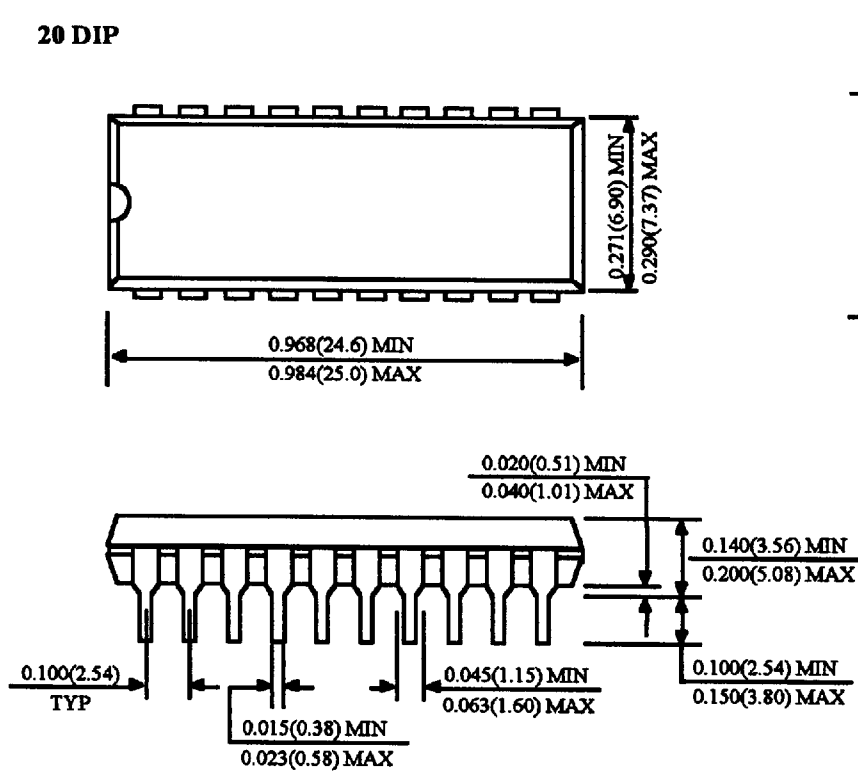


FIGURE 11. FAST PAGE MODE READ MODIFY WRITE CYCLE

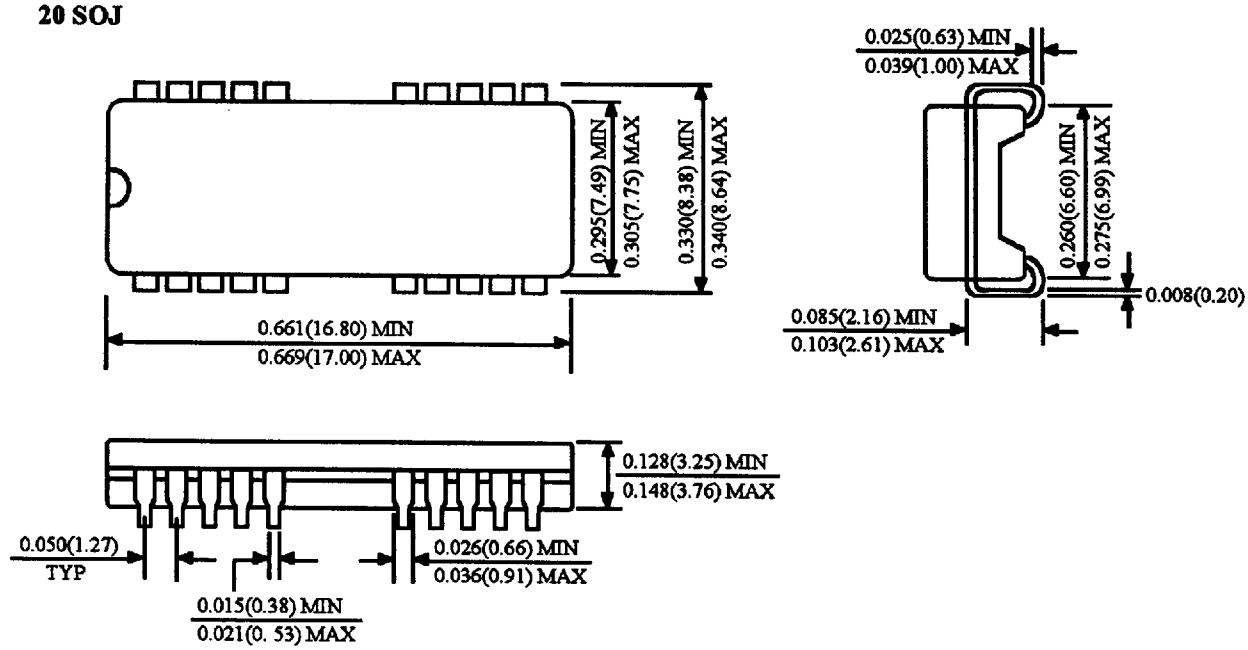
Package Dimension

Unit: Inches (mm)

20 DIP



20 SOJ



Package Dimension

Unit: Inches (mm)

20 ZIP