



8K × 8 CMOS STATIC RAM

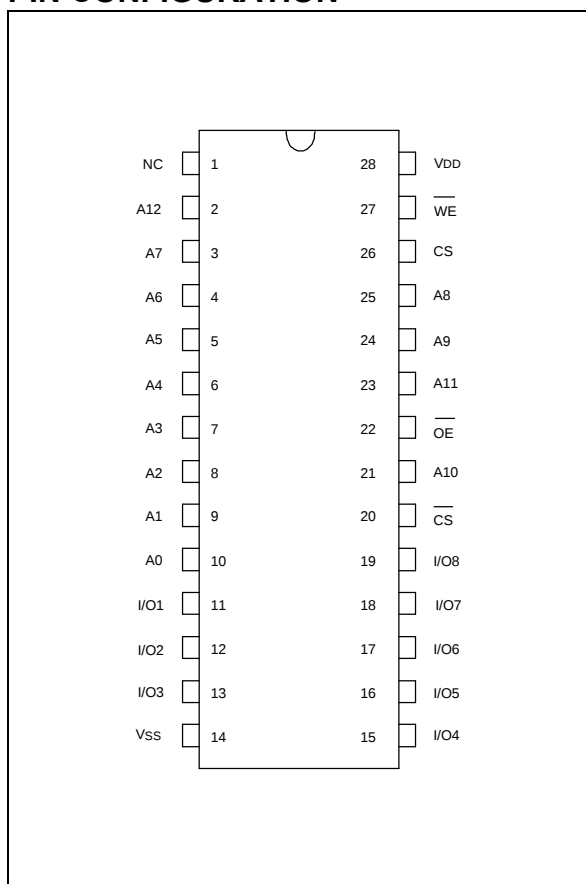
GENERAL DESCRIPTION

The W2465 is a slow-speed, low-power CMOS static RAM organized as 8192 × 8 bits that operates on a single 5-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

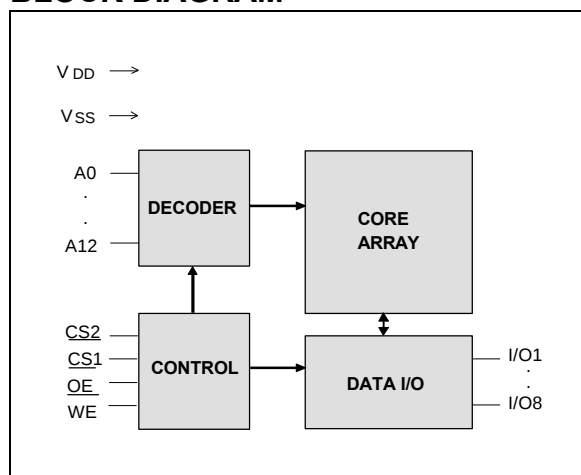
FEATURES

- Low power consumption:
 - Active: 250 mW (max.)
 - Standby: 100 μW (max.)(LL-version)
250 μW (max.)(L-version)
- Access time: 70/100 nS (max.)
- Single +5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 2V (min.)
- Available packages: 28-pin 600 mil DIP, 330 mil SOP and 300 mil skinny DIP

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A12	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
CS1, CS2	Chip Select Inputs
WE	Write Enable Input
OE	Output Enable Input
VDD	Power Supply
VSS	Ground
NC	No Connection

TRUTH TABLE

CS1	CS2	OE	WE	MODE	I/O1-I/O8	V _{DD} CURRENT
H	X	X	X	Not Selected	High Z	I _{SB} , I _{SB1}
X	L	X	X	Not Selected	High Z	I _{SB} , I _{SB1}
L	H	H	H	Output Disable	High Z	I _{DD}
L	H	L	H	Read	Data Out	I _{DD}
L	H	X	L	Write	Data In	I _{DD}

DC CHARACTERISTICS**Absolute Maximum Ratings**

PARAMETER	RATING	UNIT
Supply Voltage to V _{SS} Potential	-0.5 to +7.0	V
Input/Output to V _{SS} Potential	-0.5 to V _{DD} +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V _{IL}	-		-0.5	-	+0.8	V
Input High Voltage	V _{IH}	-		+2.2	-	V _{DD} +0.5	V
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{DD}		-2	-	+2	μA
Output Leakage Current	I _{LO}	V _{I/O} = V _{SS} to V _{DD} CS1 = V _{IH} (min.) or CS2 = V _{IL} (max.) or OE = V _{IH} (min.) or WE = V _{IL} (max.)		-2	-	+2	μA
Output Low Voltage	V _{OL}	I _{OL} = +4.0 mA		-	-	0.4	V
Output High Voltage	V _{OH}	I _{OH} = -1.0 mA		2.4	-	-	V
Operating Power Supply Current	I _{DD}	CS1 = V _{IL} (max.), CS2 = V _{IH} (min.)	70	-	-	70	mA
		I/O = 0 mA, Cycle = min. Duty = 100%	100	-	-	60	mA
Standby Power Supply Current	I _{SB}	CS1 = V _{IH} (min.) or CS2 = V _{IL} (max.), Cycle = min. Duty = 100%		-	-	3	mA
		I _{SB1}	CS1 ≥ V _{DD} -0.2V or CS2 ≤ 0.2V	LL	-	-	20
				L	-	-	50

Note: Typical characteristics are at V_{DD} = 5 V, T_A = 25° C.



CAPACITANCE

($V_{DD} = 5V$, $T_A = 25^\circ C$, $f = 1\text{ MHz}$)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	$V_{IN} = 0V$	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{OUT} = 0V$	8	pF

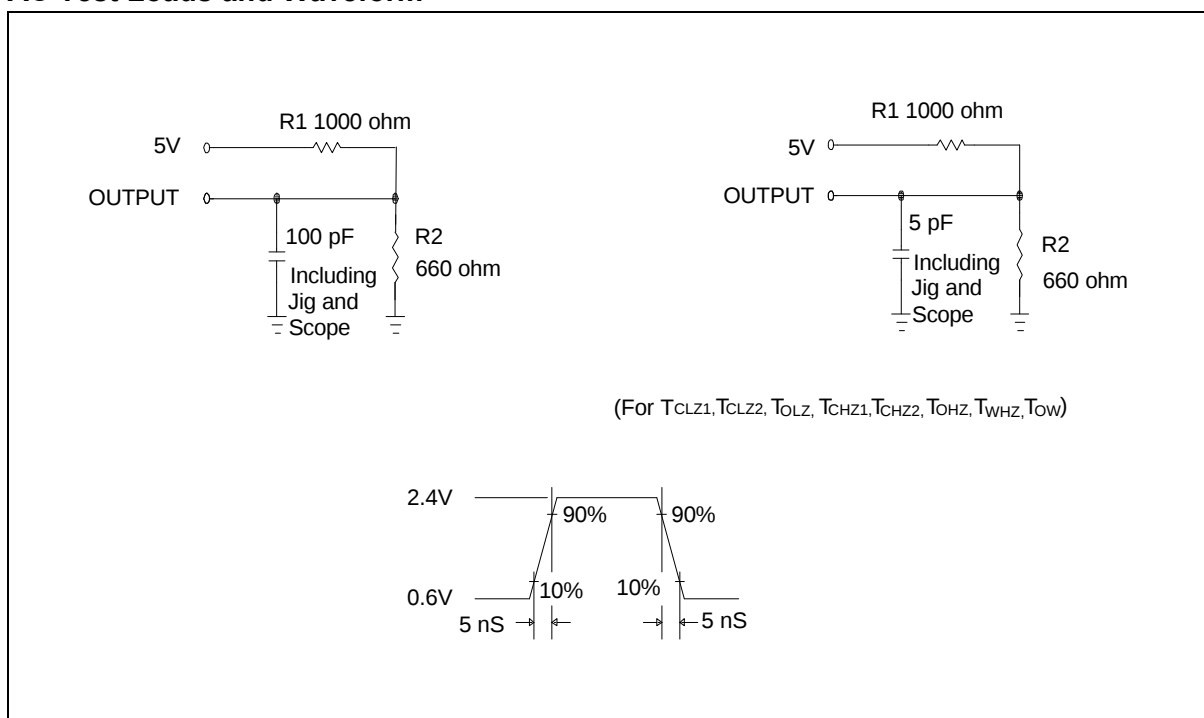
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	$C_L = 100\text{ pF}$, $I_{OH}/I_{OL} = -1\text{ mA}/4\text{ mA}$

AC Test Loads and Waveform





AC Characteristics, continued

(V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)**Read Cycle**

PARAMETER		SYM.	W2465-70		W2465-10		UNIT
			MIN.	MAX.	MIN.	MAX.	
Read Cycle Time		TRC	70	-	100	-	nS
Address Access Time		TAA	-	70	-	100	nS
Chip Select Access Time	$\overline{\text{CS1}}$	TACS1	-	70	-	100	nS
	CS2	TACS2	-	70	-	100	nS
Output Enable to Output Valid		TAOE	-	35	-	50	nS
Chip Selection to Output in Low Z	$\overline{\text{CS1}}$	TCLZ1*	5	-	10	-	nS
	CS2	TCLZ2*	5	-	10	-	nS
Output Enable to Output in Low Z		TOLZ*	5	-	5	-	nS
Chip Deselection to Output in High Z	$\overline{\text{CS1}}$	TCHZ1*	-	30	-	35	nS
	CS2	TCHZ2*	-	30	-	35	nS
Output Disable to Output in High Z		TOHZ*	-	30	-	35	nS
Output Hold from Address Change		TOH	10	-	10	-	nS

* These parameters are sampled but not 100% tested.

Write Cycle

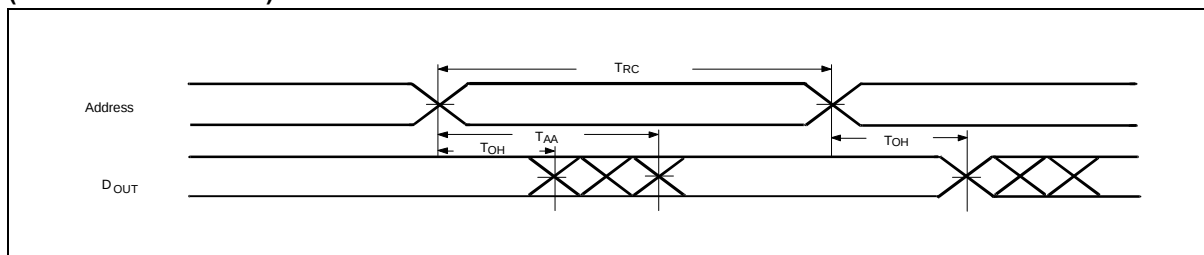
PARAMETER		SYM.	W2465-70		W2465-10		UNIT
			MIN.	MAX.	MIN.	MAX.	
Write Cycle Time		TWC	70	-	100	-	nS
Chip Selection to End of Write	$\overline{\text{CS1}}$	TCW1	60	-	80	-	nS
	CS2	TCW2	60	-	80	-	nS
Address Valid to End of Write		TAW	60	-	80	-	nS
Address Setup Time		TAS	0	-	0	-	nS
Write Pulse Width		TWP	45	-	60	-	nS
Write Recovery Time	$\overline{\text{CS1}}, \overline{\text{WE}}$	TWR1	0	-	0	-	nS
	CS2	TWR2	0	-	0	-	nS
Data Valid to End of Write		TDW	30	-	40	-	nS
Data Hold from End of Write		TDH	0	-	0	-	nS
Write to Output in High Z		TWHZ*	-	30	-	30	nS
Output Disable to Output in High Z		TOHZ*	-	30	-	30	nS
Output Active from End of Write		TOW	0	-	0	-	nS

* These parameters are sampled but not 100% tested.

TIMING WAVEFORMS

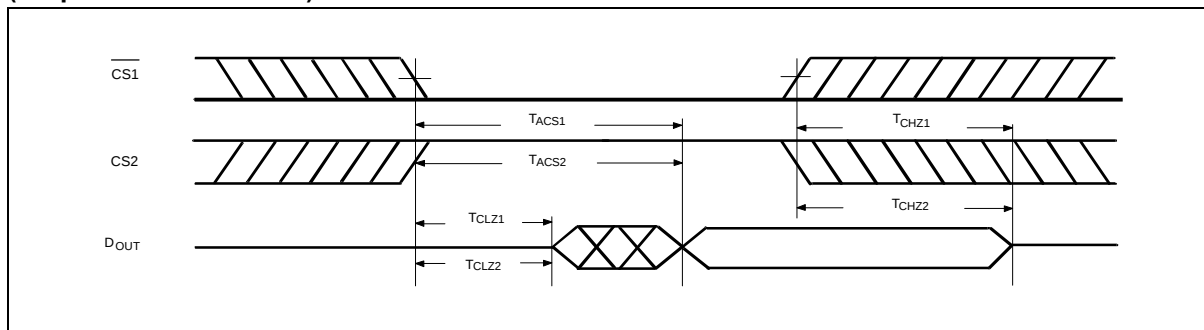
Read Cycle 1

(Address Controlled)



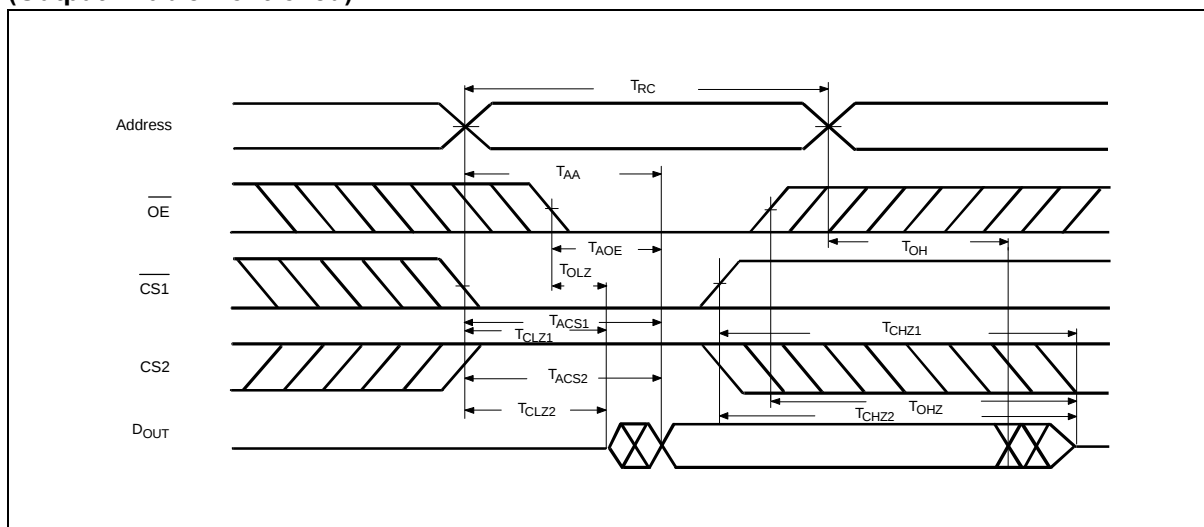
Read Cycle 2

(Chip Select Controlled)



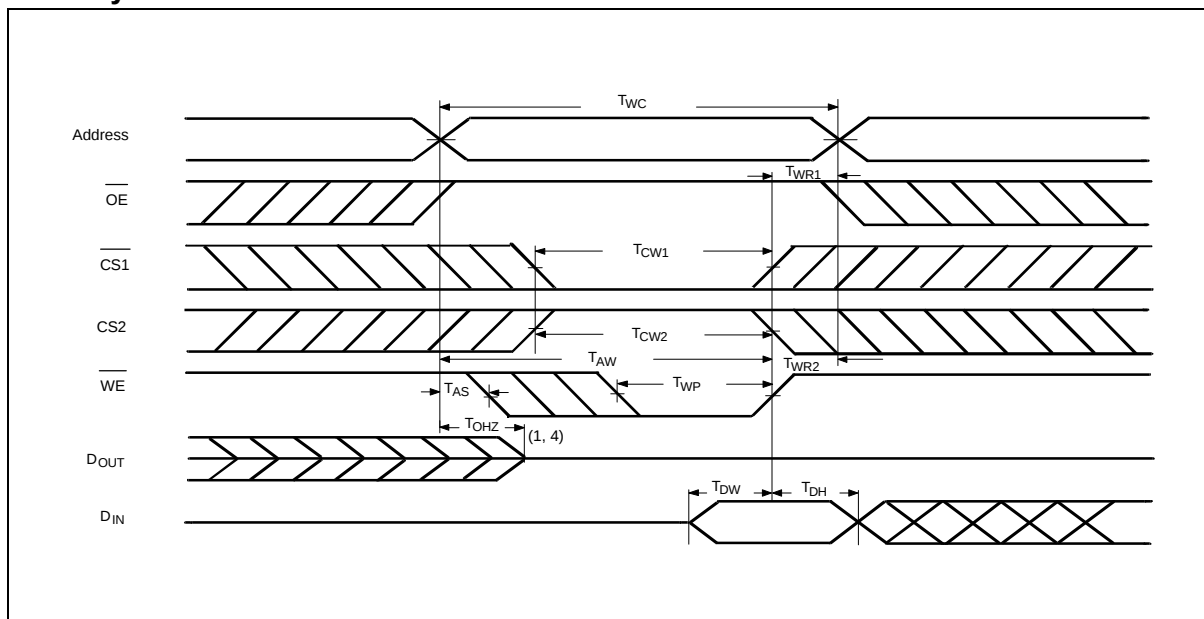
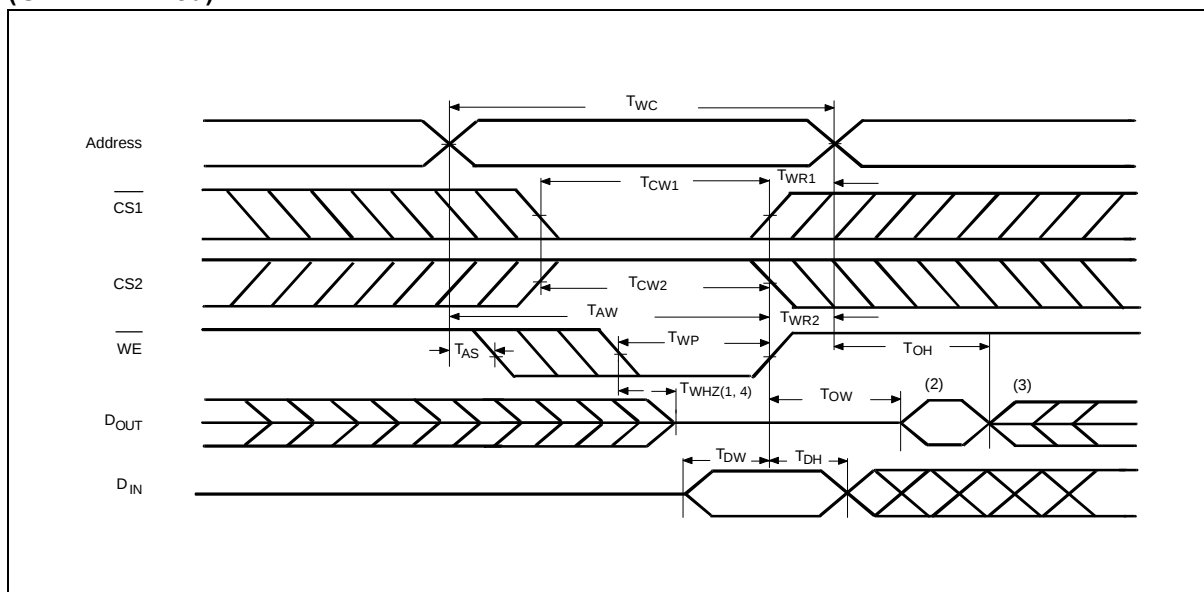
Read Cycle 3

(Output Enable Controlled)





Timing Waveforms, continued

Write Cycle 1**Write Cycle 2****(OE = V_{IL} Fixed)**

Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from D_{OUT} are the same as the data written to D_{IN} during the write cycle.
3. D_{OUT} provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with $C_L = 5$ pF. This parameter is guaranteed but not 100% tested.

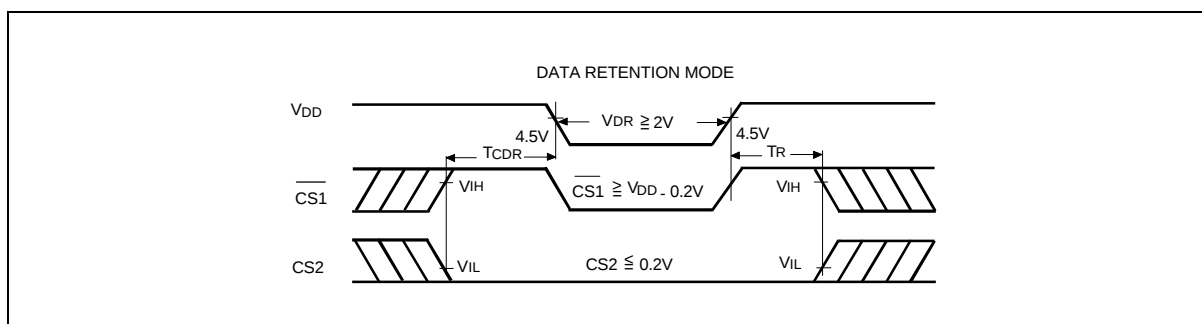
DATA RETENTION CHARACTERISTICS

(TA = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{DD} for Data Retention	V _{DR}	$\overline{CS1} \geq V_{DD} - 0.2V$, or $CS2 \leq 0.2V$	2.0	-	-	V
Data Retention Current	I _{DDDR}	$\overline{CS1} \geq V_{DD} - 0.2V$, or $CS2 \leq 0.2V$ $V_{DD} = 3V$	LL	-	-	10 μA
			L	-	-	20 μA
Chip Deselect to Data Retention Time	T _{CDR}	See data retention waveforms	0	-	-	nS
Operation Recovery Time	T _R		T _{RC} *	-	-	nS

T_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORMS



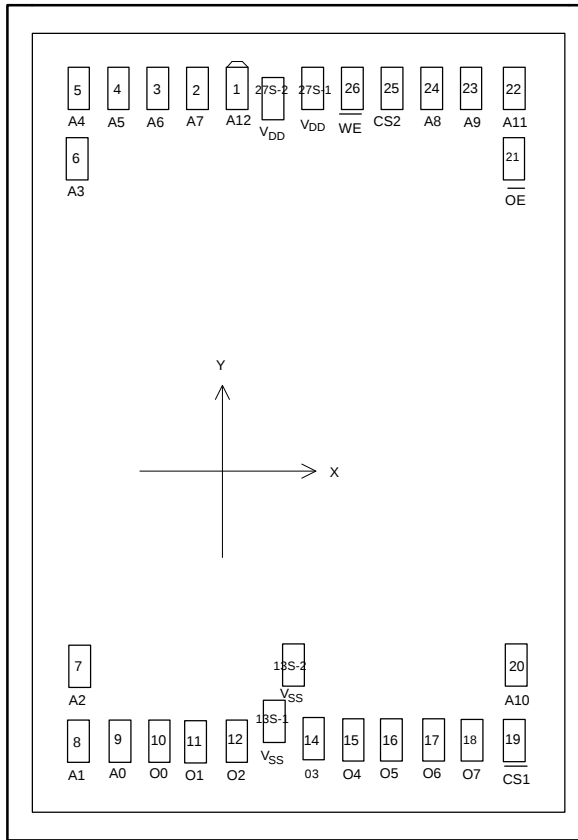
ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (μA)	PACKAGE
W2465-70LL	70	70	20	600 mil DIP
W2465-10L	100	60	50	600 mil DIP
W2465S-70LL	70	70	20	330 mil SOP
W2465S-10L	100	60	50	330 mil SOP
W2465K-70LL	70	70	20	300 mil Skinny
W2465K-10L	100	60	50	300 mil Skinny

Notes:

- Winbond reserves the right to make changes to its products without prior notice.
- Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

BONDING PAD DIAGRAM

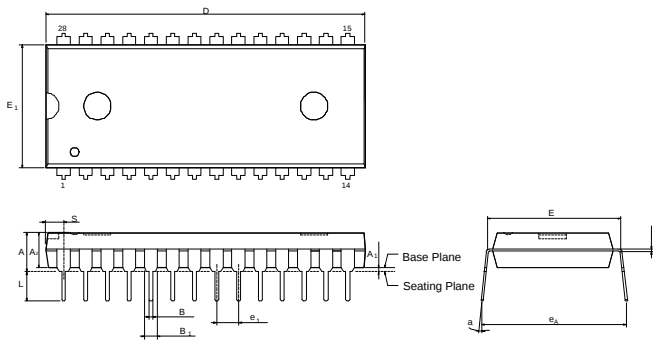


PAD NO.	X	Y
1	-226.95	1526.15
2	-350.95	1526.15
3	-484.10	1526.15
4	-608.10	1526.15
5	-739.75	1526.15
6	-741.75	1315.10
7	-741.75	-1231.85
8	-741.75	-1456.30
9	-610.60	-1456.30
10	-481.50	-1466.30
11	-343.80	-1466.30
12	-206.10	-1466.30
13S-1	-73.00	-1401.10
13S-2	-8.35	-1212.80
14	60.10	-1466.30
15	193.30	-1466.30
16	332.40	-1466.30
17	465.60	-1466.30
18	603.30	-1466.30
19	738.15	-1456.30
20	740.15	-1221.45
21	740.15	1310.80
22	738.15	1526.15
23	606.50	1526.15
24	482.50	1526.15
25	349.35	1526.15
26	225.35	1526.15
27S-1	94.20	1526.15
27S-2	-50.40	1456.10

Note: For bare chip form (C.O.B.) applications, the substrate must be connected to VDD or left floating in the PCB layout.

PACKAGE DIMENSIONS

28-pin P-DIP

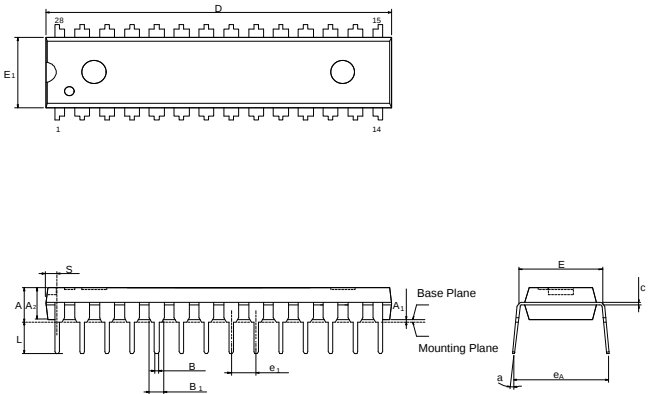


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A ₁	0.010	—	—	0.25	—	—
A ₂	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B ₁	0.058	0.060	0.064	1.47	1.52	1.63
C	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.460	1.470	—	37.08	37.34
E	0.590	0.600	0.610	14.99	15.24	15.49
E ₁	0.540	0.545	0.550	13.72	13.84	13.97
e ₁	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e _A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.090	—	—	2.29

Notes:

1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

28-pin P-DIP Skinny



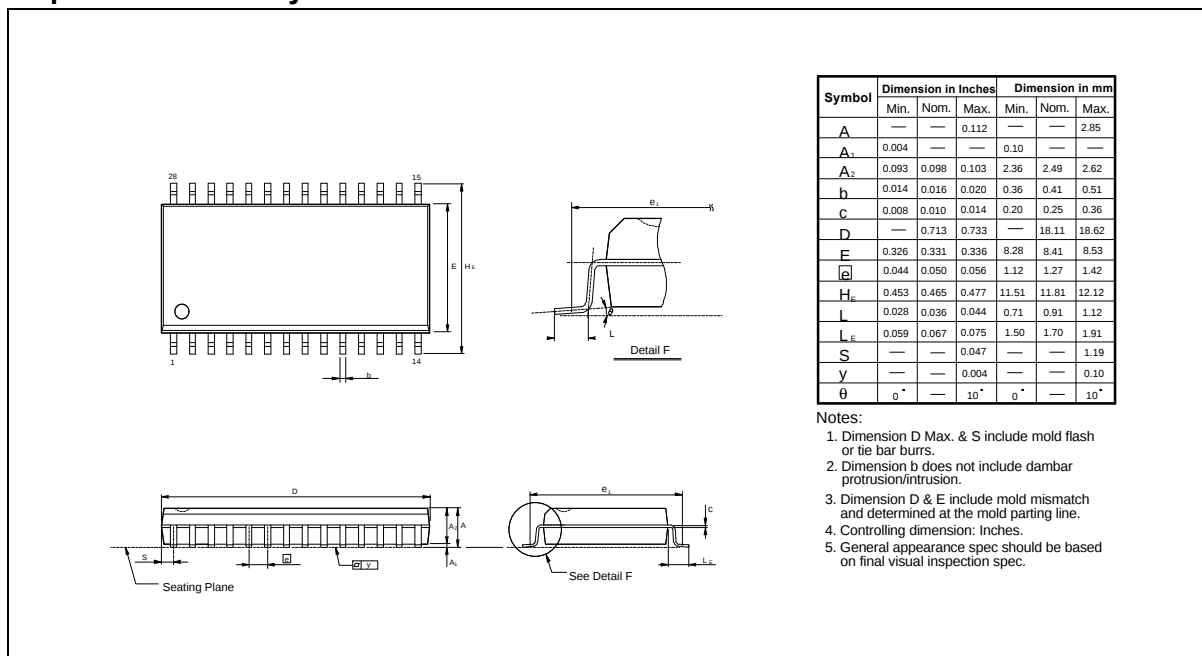
Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.175	—	—	4.45
A ₁	0.010	—	—	0.25	—	—
A ₂	0.125	0.130	0.135	3.18	3.30	3.43
B	0.016	0.018	0.022	0.41	0.46	0.56
B ₁	0.058	0.060	0.064	1.47	1.52	1.63
C	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.388	1.400	—	35.26	35.56
E	0.300	0.310	0.320	7.62	7.87	8.13
E ₁	0.283	0.288	0.293	7.19	7.32	7.44
e ₁	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0°	—	15°	0°	—	15°
e _A	0.330	0.350	0.370	8.38	8.89	9.40
S	—	—	0.055	—	—	1.40

Notes:

1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.



Package Dimensions, continued

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Note: All data and specifications are subject to change without notice.