

W27E010



128K × 8 ELECTRICALLY ERASABLE EPROM

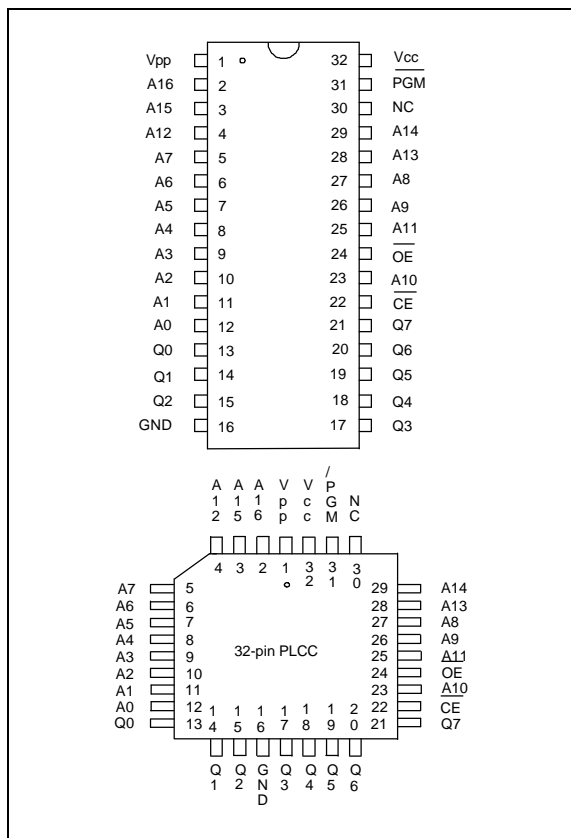
GENERAL DESCRIPTION

The W27E010 is a high speed, low power Electrically Erasable and Programmable Read Only Memory organized as 131072 × 8 bits that operates on a single 5 volt power supply. The W27E010 provides an electrical chip erase function.

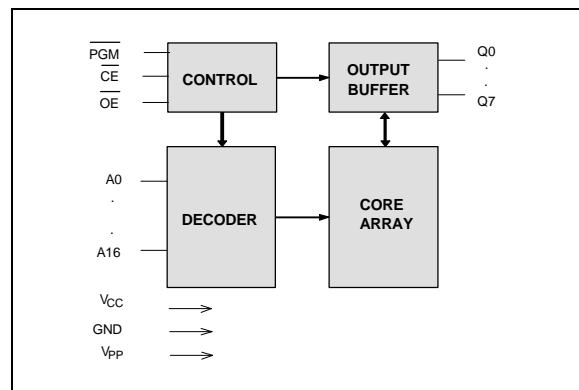
FEATURES

- High speed access time: 45/55/70/90/120 nS (max.)
- Read operating current: 30 mA (typ.)
- Erase/Programming operating current: 1 mA (typ.)
- Standby current: 5 μA (typ.)
- Single 5V power supply
- +14V erase/+12V programming voltage
- Fully static operation
- All inputs and outputs directly TTL/CMOS compatible
- Three-state outputs
- Available packages: 32-pin 600 mil DIP, 450 mil SOP and PLCC

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A16	Address Inputs
Q0–Q7	Data Inputs/Outputs
CE	Chip Enable
OE	Output Enable
PGM	Program Enable
VPP	Program/Erase Supply Voltage
VCC	Power Supply
GND	Ground
NC	No Connection



FUNCTIONAL DESCRIPTION

Read Mode

Like conventional UVEPROMs, the W27E010 has two control functions, both of which produce data at the outputs.

\overline{CE} is for power control and chip select. \overline{OE} controls the output buffer to gate data to the output pins. When addresses are stable, the address access time (T_{ACC}) is equal to the delay from \overline{CE} to output (T_{CE}), and data are available at the outputs T_{OE} after the falling edge of \overline{OE} , if T_{ACC} and T_{CE} timings are met.

Erase Mode

The erase operation is the only way to change data from "0" to "1." Unlike conventional UVEPROMs, which use ultraviolet light to erase the contents of the entire chip (a procedure that requires up to half an hour), the W27E010 uses electrical erasure. Generally, the chip can be erased within 100 mS by using an EPROM writer with a special erase algorithm.

Erase mode is entered when V_{PP} is raised to V_{PE} (14V), $V_{CC} = V_{CE}$ (5V), $\overline{CE} = V_{IL}$ (0.8V or below but higher than GND), $\overline{OE} = V_{IH}$ (2V or above but lower than V_{CC}), $A_9 = V_{HH}$ (14V), $A_0 = V_{IL}$, and all other address pins equal V_{IL} and data input pins equal V_{IH} . Pulsing \overline{PGM} low starts the erase operation.

Erase Verify Mode

After an erase operation, all of the bytes in the chip must be verified to check whether they have been successfully erased to "1" or not. The erase verify mode automatically ensures a substantial erase margin. This mode will be entered after the erase operation if $V_{PP} = V_{PE}$ (14V), $\overline{CE} = V_{IL}$, and $\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$.

Program Mode

Programming is performed exactly as it is in conventional UVEPROMs, and programming is the only way to change cell data from "1" to "0." The program mode is entered when V_{PP} is raised to V_{PP} (12V), $V_{CC} = V_{CP}$ (5V), $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, the address pins equal the desired addresses, and the input pins equal the desired inputs. Pulsing \overline{PGM} low starts the programming operation.

Program Verify Mode

All of the bytes in the chip must be verified to check whether they have been successfully programmed with the desired data or not. Hence, after each byte is programmed, a program verify operation should be performed. The program verify mode automatically ensures a substantial program margin. This mode will be entered after the program operation if $V_{PP} = V_{PP}$ (12V), $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$, and $\overline{PGM} = V_{IH}$.

Erase/Program Inhibit

Erase or program inhibit mode allows parallel erasing or programming of multiple chips with different data. When $\overline{CE} = V_{IH}$, erasing or programming of non-target chips is inhibited, so that except for the \overline{CE} , the W27E010 may have common inputs.



Standby Mode

The standby mode significantly reduces VCC current. This mode is entered when $\overline{CE} = V_{IH}$. In standby mode, all outputs are in a high impedance state, independent of \overline{OE} and PGM.

Two-line Output Control

Since EPROMs are often used in large memory arrays, the W27E010 provides two control inputs for multiple memory connections. Two-line control provides for lowest possible memory power dissipation and ensures that data bus contention will not occur.

System Considerations

EPROM power switching characteristics require careful device decoupling. System designers are concerned with three supply current issues: standby current levels (ISB), active current levels (ICC), and transient current peaks produced by the falling and rising edges of \overline{CE} . Transient current magnitudes depend on the device output's capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μ F ceramic capacitor connected between its VCC and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every eight devices, a 4.7 μ F electrolytic capacitor should be placed at the array's power supply connection between VCC and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

TABLE OF OPERATING MODES

$V_{PP} = 12V$, $V_{PE} = 14V$, $V_{HH} = 12V$, $V_{CP} = 5V$, $X = V_{IH}$ or V_{IL}

MODE	PINS							
	\overline{CE}	\overline{OE}	\overline{PGM}	A0	A9	VCC	VPP	OUTPUTS
Read	VIL	VIL	X	X	X	VCC	VCC	DOUT
Output Disable	VIL	V _{IH}	X	X	X	VCC	VCC	High Z
Standby (TTL)	V _{IH}	X	X	X	X	VCC	VCC	High Z
Standby (CMOS)	$V_{CC} \pm 0.3V$	X	X	X	X	VCC	VCC	High Z
Program	VIL	V _{IH}	V _{IL}	X	X	V _{CP}	V _{PP}	DIN
Program Verify	VIL	V _{IL}	V _{IH}	X	X	V _{CP}	V _{PP}	DOUT
Program Inhibit	V _{IH}	X	X	X	X	V _{CP}	V _{PP}	High Z
Erase	VIL	V _{IH}	V _{IL}	V _{IL}	V _{PE}	VCC	V _{PE}	FF (Hex)
Erase Verify	VIL	V _{IL}	V _{IH}	X	X	VCC	V _{PE}	DOUT
Erase Inhibit	V _{IH}	X	X	X	X	V _{CP}	V _{PE}	High Z
Product Identifier- Manufacturer	VIL	V _{IL}	X	V _{IL}	V _{HH}	VCC	VCC	DA (Hex)
Product Identifier-Device	VIL	V _{IL}	X	V _{IH}	V _{HH}	VCC	VCC	01 (Hex)



DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Ambient Temperature with Power Applied	-55 to +125	°C
Storage Temperature	-65 to +125	°C
Voltage on all Pins with Respect to Ground Except VCC, VPP and A9 Pins	-0.5 to VCC +0.5	V
Voltage on VCC Pin with Respect to Ground	-0.5 to +7	V
Voltage on VPP Pin with Respect to Ground	-0.5 to +14.5	V
Voltage on A9 Pin with Respect to Ground	-0.5 to +14.5	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC Erase Characteristics

($T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$, $V_{HH} = 14\text{V}$)

PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Input Load Current	ILI	$V_{IN} = V_{IL}$ or V_{IH}	-10	-	10	μA
VCC Erase Current	ICP	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, $\overline{PGM} = V_{IL}$, A9 = VHH	-	-	30	mA
VPP Erase Current	IPP	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, $\overline{PGM} = V_{IL}$, A9 = VHH	-	-	30	mA
Input Low Voltage	VIL	-	-0.3	-	0.8	V
Input High Voltage	VIH	-	2.4	-	5.5	V
Output Low Voltage (Verify)	VOL	$I_{OL} = 2.1\text{ mA}$	-	-	0.45	V
Output High Voltage (Verify)	VOH	$I_{OH} = -0.4\text{ mA}$	2.4	-	-	V
A9 Erase Voltage	VID	-	13.75	14.0	14.25	V
VPP Erase Voltage	VPE	-	13.75	14.0	14.25	V
VCC Supply Voltage (Erase)	VCE	-	4.5	5.0	5.5	V

Note: VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP.



CAPACITANCE

($V_{CC} = 5V$, $T_A = 25^\circ C$, $f = 1\text{ MHz}$)

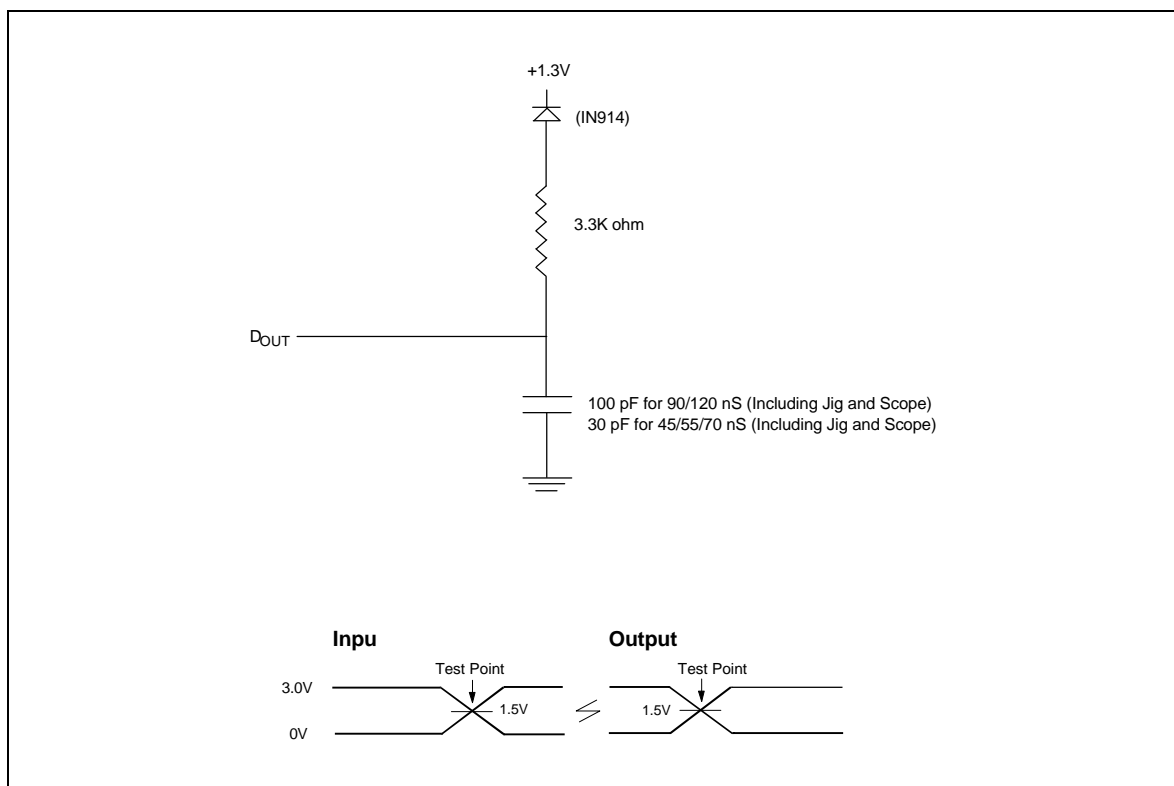
PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
Input Capacitance	CIN	$V_{IN} = 0V$	6	pF
Output Capacitance	COUT	$V_{OUT} = 0V$	12	pF

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0 to 3.0V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V/1.5V
Output Load	$C_L = 30\text{ pF}$, $I_{OH}/I_{OL} = -0.4\text{ mA}/2.1\text{ mA}$

AC Test Load and Waveforms





READ OPERATION DC CHARACTERISTICS

(V_{CC} = 5.0V ±10%)

PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Input Load Current	I _{LI}	V _{IN} = 0V to V _{CC}	-5	-	5	μA
Output Leakage Current	I _{LO}	V _{OUT} = 0V to V _{CC}	-10	-	10	μA
Standby V _{CC} Current (TTL input)	I _{SB}	$\overline{CE} = V_{IH}$	-	-	1.0	mA
Standby V _{CC} Current (CMOS input)	I _{SB1}	$\overline{CE} = V_{CC} \pm 0.2V$	-	5	100	μA
V _{CC} Operating Current	I _{CC}	$\overline{CE} = V_{IL}$ I _{OUT} = 0 mA f = 5 MHz	-	-	30	mA
V _{PP} Operating Current	I _{PP}	V _{PP} = V _{CC}	-	-	10	μA
Input Low Voltage	V _{IL}	-	-0.3	-	0.8	V
Input High Voltage	V _{IH}	-	2.0	-	V _{CC} + 0.5	V
Output Low Voltage	V _{OL}	I _{OL} = 2.1 mA	-	-	0.45	V
Output High Voltage	V _{OH}	I _{OH} = -0.4 mA	2.4	-	-	V
V _{PP} Operating Voltage	V _{PP}	-	V _{CC} - 0.7	-	V _{CC}	V

READ OPERATION AC CHARACTERISTICS

(V_{CC} = 5.0V ±10%, for 70, 90 and 120 nS; V_{CC} = 5.0V ±5% for 45, 55 nS, T_A = 0 to 70° C)

PARAMETER	SYM.	W27E010-45		W27E010-55		W27E010-70		W27E010-90		W27E010-12		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T _{RC}	45	-	55	-	70	-	90	-	120	-	nS
Chip Enable Access Time	T _{CE}	-	45	-	55	-	70	-	90	-	120	nS
Address Access Time	T _{ACC}	-	45	-	55	-	70	-	90	-	120	nS
Output Enable Access Time	T _{OE}	-	20	-	25	-	30	-	40	-	55	nS
\overline{OE} High to High-Z Output	T _{DF}	-	20	-	20	-	25	-	25	-	30	nS
Output Hold from Address Change	T _{OH}	0	-	0	-	0	-	0	-	0	-	nS

Note: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.



DC PROGRAMMING CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 25° C ±5° C)

PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Input Load Current	I _{LI}	V _{IN} = V _{IL} or V _{IH}	-	-	10	μA
V _{CC} Program Current	I _{CP}	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH},$ $\overline{PGM} = V_{IL}$	-	-	30	mA
V _{PP} Program Current	I _{PP}	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH},$ $\overline{PGM} = V_{IL}$	-	-	30	mA
Input Low Voltage	V _{IL}	-	-0.3	-	0.8	V
Input High Voltage	V _{IH}	-	2.4	-	5.5	V
Output Low Voltage (Verify)	V _{OL}	I _{OL} = 2.1 mA	-	-	0.45	V
Output High Voltage (Verify)	V _{OH}	I _{OH} = -0.4 mA	2.4	-	-	V
A9 Silicon I.D. Voltage	V _{ID}	-	11.5	12.0	12.5	V
V _{PP} Program Voltage	V _{PP}	-	11.75	12.0	12.25	V
V _{CC} Supply Voltage (Program)	V _{CP}	-	4.5	5.0	5.5	V

AC PROGRAMMING/ERASE CHARACTERISTICS

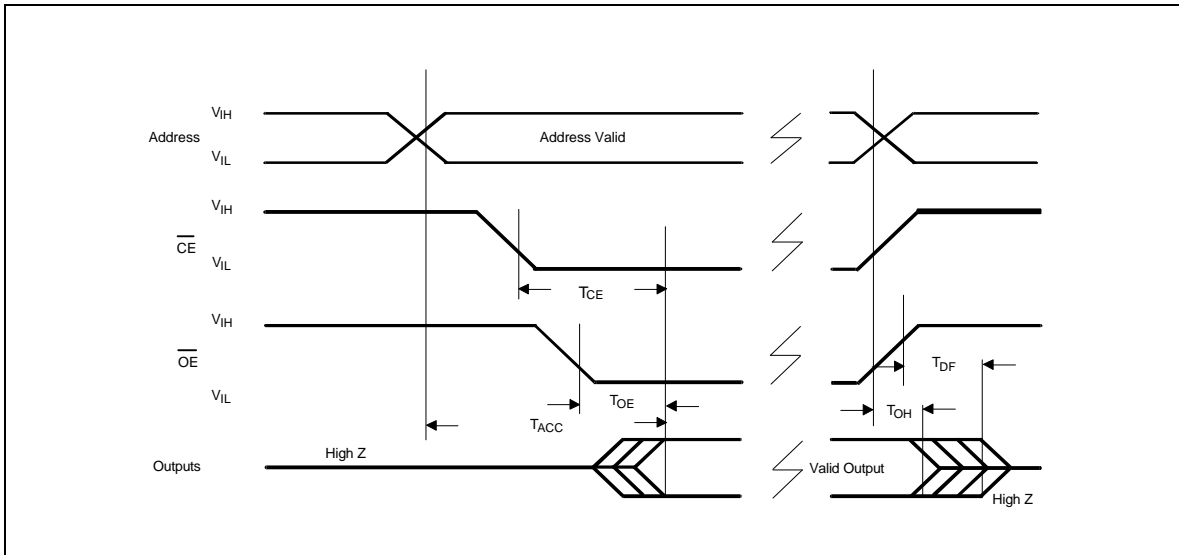
(V_{CC} = 5.0V ±10%, T_A = 25° C ±5° C)

PARAMETER	SYM.	LIMITS			UNIT
		MIN.	TYP.	MAX.	
V _{PP} Setup Time	T _{VPS}	2.0	-	-	μS
Address Setup Time	T _{AS}	2.0	-	-	μS
Data Setup Time	T _{DS}	2.0	-	-	μS
\overline{PGM} Program Pulse Width	T _{PWP}	95	100	105	μS
\overline{PGM} Erase Pulse Width	T _{PWE}	95	100	105	mS
Data Hold Time	T _{DH}	2.0	-	-	μS
\overline{OE} Setup Time	T _{OES}	2.0	-	-	μS
Data Valid from \overline{OE}	T _{OEV}	-	-	150	nS
\overline{OE} High to Output High Z	T _{DFP}	0	-	130	nS
Address Hold Time after \overline{PGM} High	T _{AH}	0	-	-	μS
Address Hold Time (Erase)	T _{AHE}	2.0	-	-	μS
\overline{CE} Setup Time	T _{CES}	2.0	-	-	μS

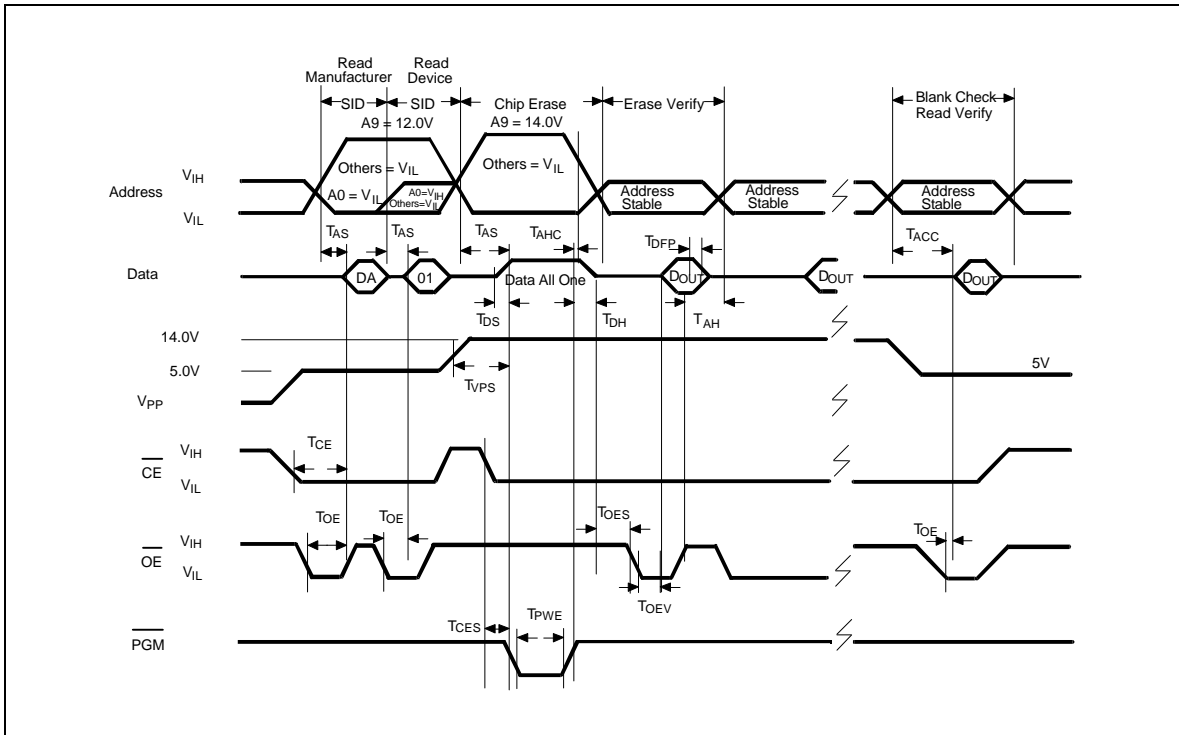
Note: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

TIMING WAVEFORMS

AC Read Waveform



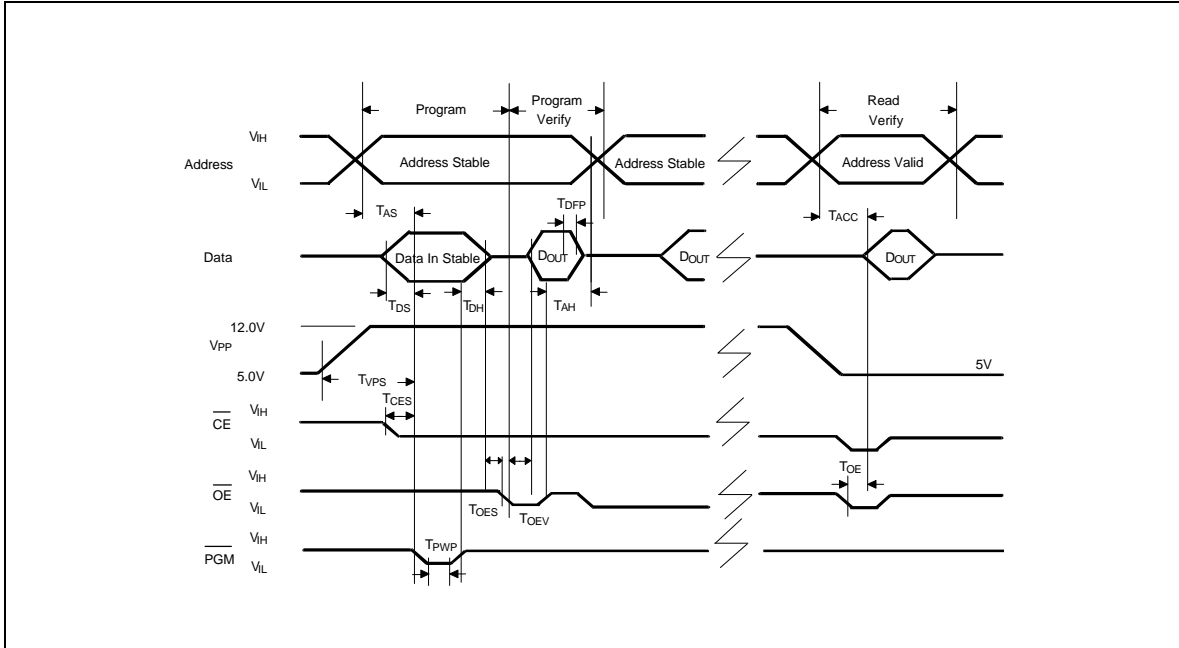
Erase Waveform



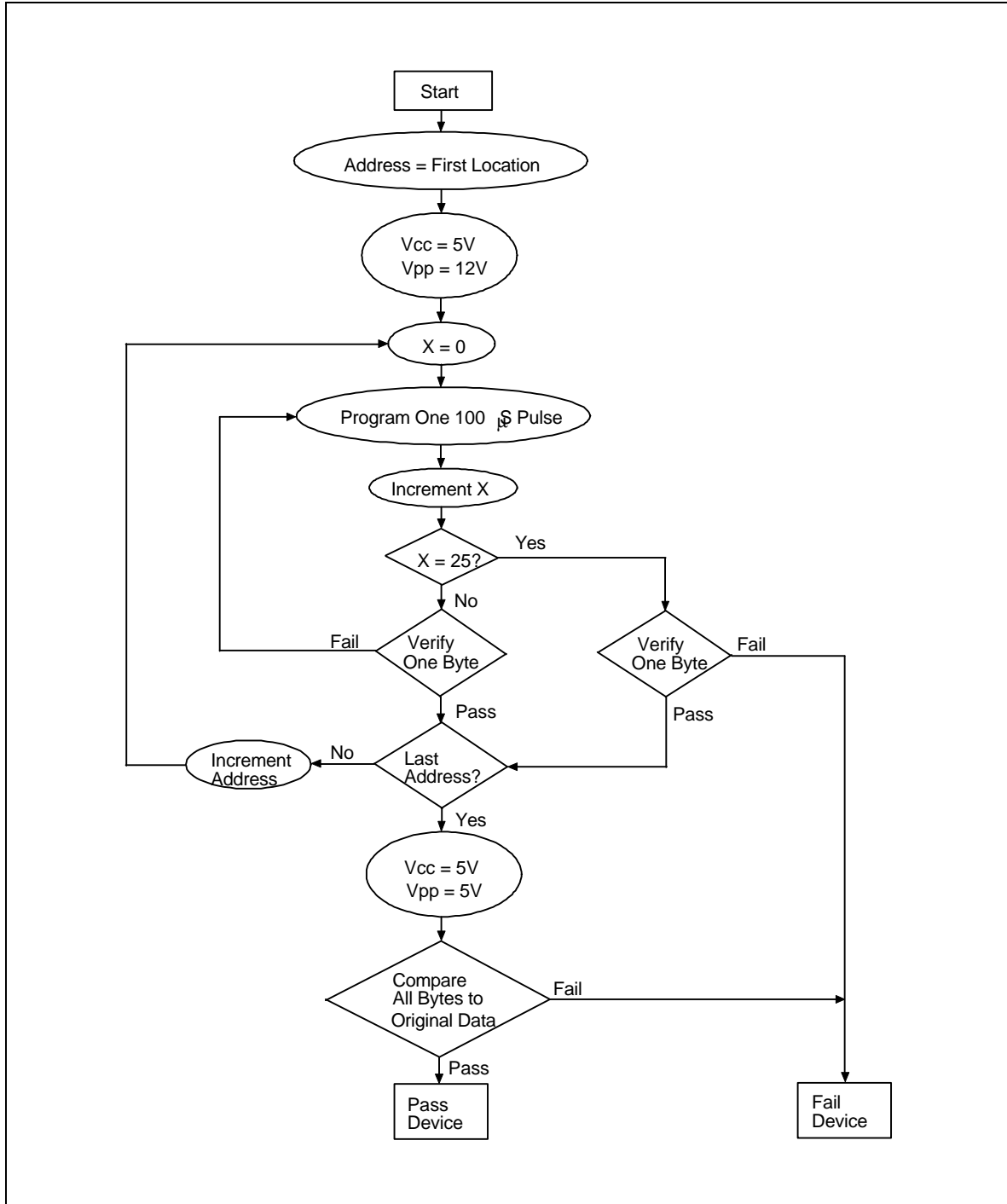


Timing Waveforms, Continued

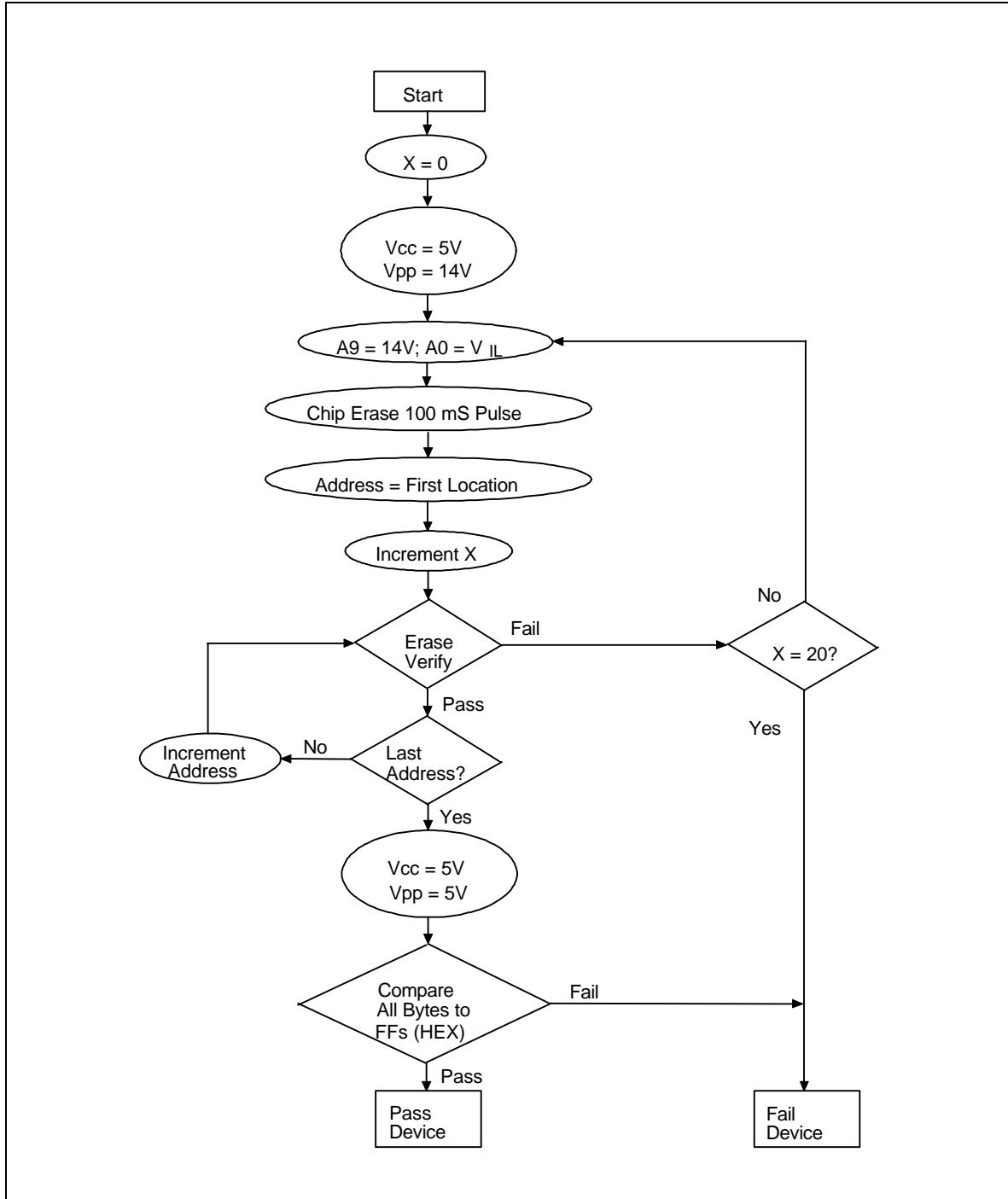
Programming Waveform



SMART PROGRAMMING ALGORITHM



SMART ERASE ALGORITHM



W27E010



ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	STANDBY V _{cc} CURRENT MAX. (mA)	PACKAGE
W27E010-45	45	30	100	600 mil DIP
W27E010-55	55	30	100	600 mil DIP
W27E010-70	70	30	100	600 mil DIP
W27E010-90	90	30	100	600 mil DIP
W27E010-12	120	30	100	600 mil DIP
W27E010S-45	45	30	100	450 mil SOP
W27E010S-55	55	30	100	450 mil SOP
W27E010S-70	70	30	100	450 mil SOP
W27E010S-90	90	30	100	450 mil SOP
W27E010S-12	120	30	100	450 mil SOP
W27E010P-45	45	30	100	32-pin PLCC
W27E010P-55	55	30	100	32-pin PLCC
W27E010P-70	70	30	100	32-pin PLCC
W27E010P-90	90	30	100	32-pin PLCC
W27E010P-12	120	30	100	32-pin PLCC

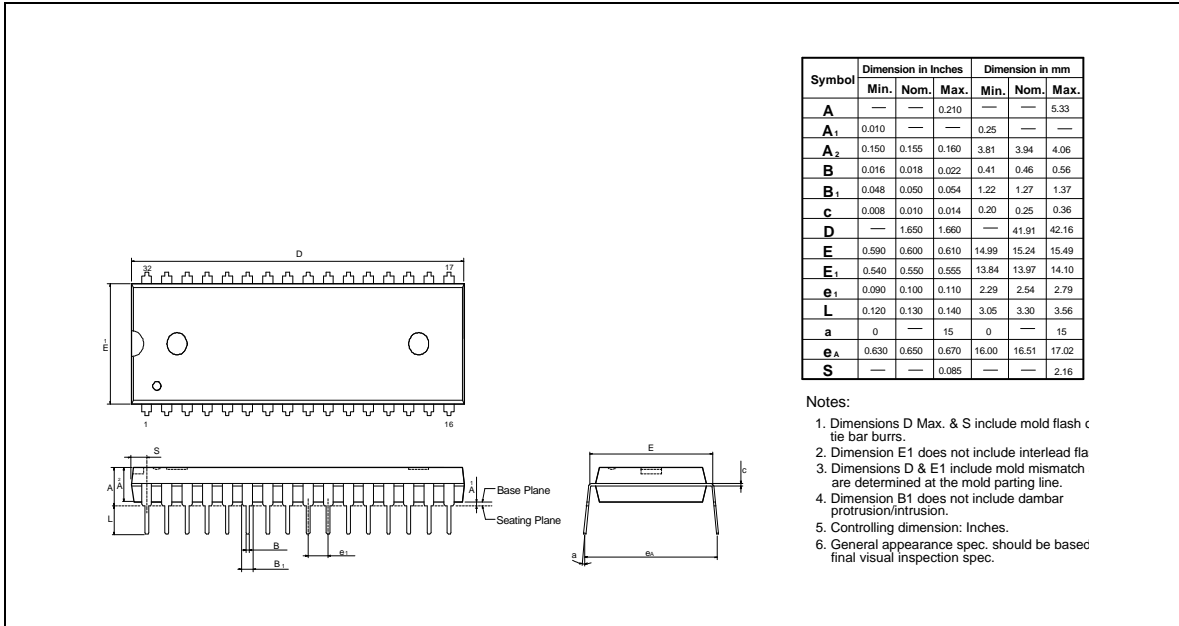
Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

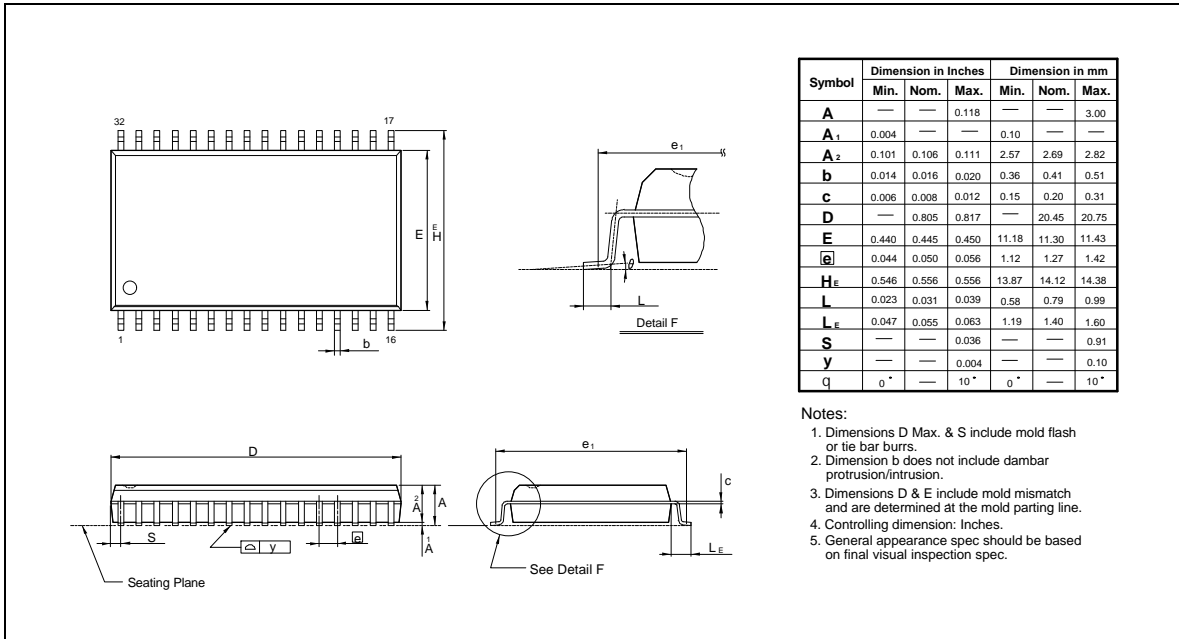


PACKAGE DIMENSIONS

32-pin P-DIP



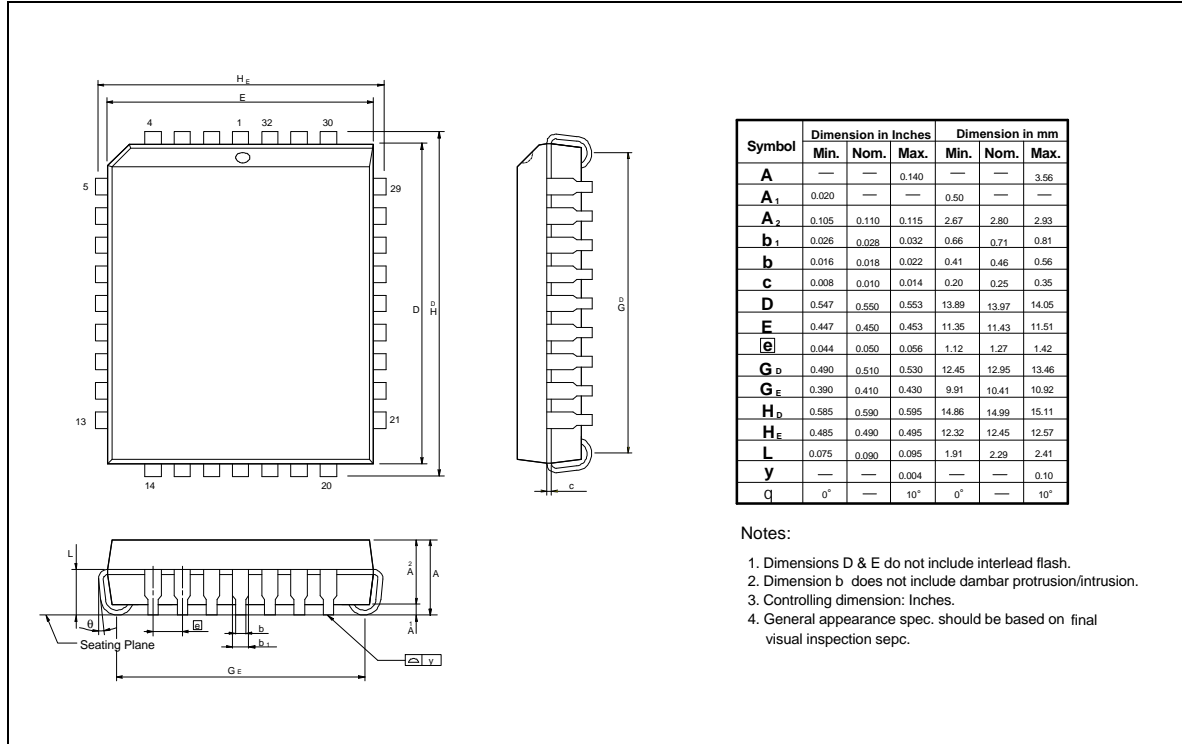
32-pin SO Wide Body





Package Dimensions, Continued

32-Lead PLCC



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.140	—	—	3.56
A₁	0.020	—	—	0.50	—	—
A₂	0.105	0.110	0.115	2.67	2.80	2.93
b₁	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.35
D	0.547	0.550	0.553	13.89	13.97	14.05
E	0.447	0.450	0.453	11.35	11.43	11.51
ⓐ	0.044	0.050	0.056	1.12	1.27	1.42
G_D	0.490	0.510	0.530	12.45	12.95	13.46
G_E	0.390	0.410	0.430	9.91	10.41	10.92
H_D	0.585	0.590	0.595	14.86	14.99	15.11
H_E	0.485	0.490	0.495	12.32	12.45	12.57
L	0.075	0.090	0.095	1.91	2.29	2.41
y	—	—	0.004	—	—	0.10
Q	0°	—	10°	0°	—	10°

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches.
4. General appearance spec. should be based on final visual inspection sepc.



VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A6	Jun. 2000	5	Modify Input Pulse Levels in AC Test Conditions



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Note: All data and specifications are subject to change without notice.