# MP7542

5 V CMOS
4-Bit Input, 12-Bit
Digital-to-Analog Converter

## FEATURES

- **12-Bit DAC with a 4-Bit Parallel Address for 4 & 8-Bit Microprocessor or Microcontroller Interface**
- **Nonlinearity ±1/2 LSB Tmin to Tmax**
- **Latch-Up Free**
- **Low Sensitivity to Output Amplifier $V_{OS}$**
- **Low Output Capacitance**
- **+5 V Supply Operation**
- **Low Power Consumption: 40mW Max.**
- **Low Cost**
- **Serial Version: MP7543**

## GENERAL DESCRIPTION

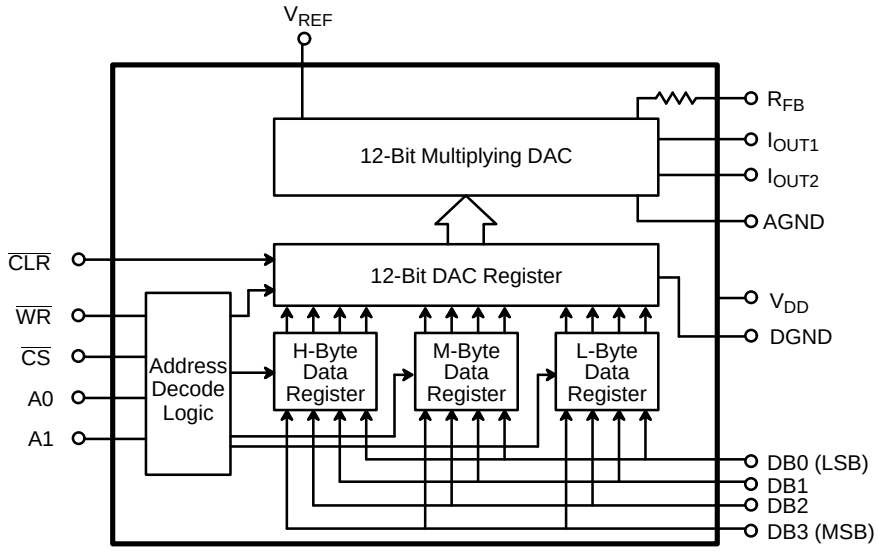
The MP7542 is a precision, 12-bit CMOS 4-quadrant multiplying Digital-to-Analog Converter designed for direct interface to 4 and 8-bit microprocessors.

The MP7542 consists of three 4-bit registers, a 12-bit DAC register, address decoding logic, and a 12-bit CMOS multiplying DAC. Data is loaded into the data registers in three 4-bit nibbles and subsequently transferred to the 12-bit DAC register. All data loading or data transfer operations are identical to the WRITE cycle of a static RAM. A CLEAR input allows the 12-bit DAC register to be reset to all zeros.

The MP7542 is manufactured using advanced thin-film on monolithic double metal CMOS fabrication process. A unique decoding technique is utilized yielding excellent accuracy and stability.

The MP7542 reduces the additional linearity errors due to output amplifier offset to only 330µV per millivolt of offset versus 670 µV for the standard R-2R ladder CMOS DACs.

## SIMPLIFIED BLOCK DIAGRAM



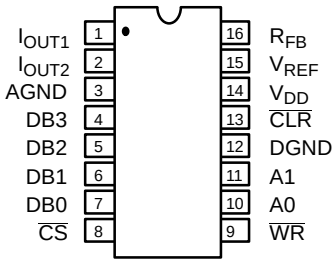
## ORDERING INFORMATION

| Package Type | Temperature Range | Part No. | INL (LSB) | DNL (LSB) | Gain Error (LSB) |
|---|---|---|---|---|---|
| Plastic Dip | –40 to +85°C | MP7542JN | ±1 | ±2 | ±14.5 |
| Plastic Dip | –40 to +85°C | MP7542KN | ±1/2 | ±1 | ±14.5 |
| SOIC | –40 to +85°C | MP7542JS | ±1 | ±2 | ±14.5 |
| SOIC | –40 to +85°C | MP7542KS | ±1/2 | ±1 | ±14.5 |
| Ceramic Dip | –40 to +85°C | MP7542AD | ±1 | ±2 | ±14.5 |
| Ceramic Dip | –40 to +85°C | MP7542BD | ±1/2 | ±1 | ±14.5 |
| Ceramic Dip | –55 to +125°C | MP7542SD* | ±1 | ±2 | ±14.5 |
| Ceramic Dip | –55 to +125°C | MP7542TD* | ±1/2 | ±1 | ±14.5 |

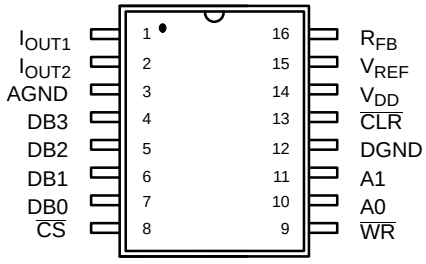
*Contact factory for non-compliant military processing

## PIN CONFIGURATIONS

*See Packaging Section for Package Dimensions*




**16 Pin CDIP, PDIP (0.300")**
**D16, N16**




**16 Pin SOIC (Jedec, 0.300")**
**S16**

## PIN OUT DEFINITIONS

| PIN NO. | NAME | DESCRIPTION |
|---|---|---|
| 1 | $I_{OUT1}$ | DAC current output. Normally terminated at op amp. |
| 2 | $I_{OUT2}$ | DAC current output. Normally terminated at ground. |
| 3 | AGND | Analog Ground |
| 4 | DB3 | Data Input Bit 3 (MSB) |
| 5 | DB2 | Data Input Bit 2 |
| 6 | DB1 | Data Input Bit 1 |
| 7 | DB0 | Data Input Bit 0 (LSB) |

| PIN NO. | NAME | DESCRIPTION |
|---|---|---|
| 8 | $\overline{CS}$ | Chip Select Input |
| 9 | $\overline{WR}$ | Write Input |
| 10 | A0 | Address Bus Input |
| 11 | A1 | Address Bus Input |
| 12 | DGND | Digital Ground |
| 13 | $\overline{CLR}$ | Clear Input |
| 14 | $V_{DD}$ | +5 V Supply Input |
| 15 | $V_{REF}$ | Reference Input |
| 16 | $R_{FB}$ | DAC Feedback Resistor |

## ELECTRICAL CHARACTERISTICS

**($V_{DD}$ = + 5 V, $V_{REF}$ = +10 V unless otherwise noted)**

| Parameter | Symbol | 25°C Min | 25°C Typ | 25°C Max | Tmin to Tmax Min | Tmin to Tmax Max | Units | Test Conditions/Comments |
|---|---|---|---|---|---|---|---|---|
| **STATIC PERFORMANCE[1]** | | | | | | | | |
| Resolution (All Grades) | N | 12 | | | 12 | | Bits | |
| Integral Non-Linearity (Relative Accuracy) | INL | | | | | | LSB | Best Fit Straight Line Spec. (Max INL – Min INL) / 2 |
| J, A, S | | | | ±1 | | ±1 | | |
| K, B, T | | | | ±1/2 | | ±1/2 | | |
| Differential Non-Linearity | DNL | | | | | | LSB | Monotonicity |
| J, A, S | | | | ±2 | | ±2 | | 11 Bits Guaranteed |
| K, B, T | | | | ±1 | | ±1 | | 12 Bits Guaranteed |
| Gain Error | | | | | | | | |
| J, A, S, K, B, T | GE | | | ±12.3 | | ±14.5 | LSB | Using Internal $R_{FB}$ |
| Gain Temperature Coefficient[2] | $TC_{GE}$ | | | | | ±2 | ppm/°C | ΔGain/ΔTemperature |
| Power Supply Rejection Ratio | PSRR | | | ±50 | | ±100 | ppm/% | $\lvert\Delta Gain/\Delta V_{DD}\rvert$ $\Delta V_{DD}$ = ± 5% |
| Output Leakage Current | $I_{OUT}$ | | | ±10 | | ±200 | nA | |
| **DYNAMIC PERFORMANCE** | | | | | | | | $R_L$=100Ω, $C_L$=13pF |
| Current Settling Time[2] | $t_S$ | | | 2.0 | | 2.0 | µs | Full Scale Change to 1/2 LSB |
| AC Feedthrough at $I_{OUT1}$[2] | $F_T$ | | | 2.5 | | 2.5 | mV p-p | $V_{REF}$ = 10kHz, 20 Vp-p, sinewave |
| **REFERENCE INPUT** | | | | | | | | |
| Input Resistance | $R_{IN}$ | 5 | 10 | 20 | 5 | 20 | kΩ | |
| **DIGITAL INPUTS[3]** | | | | | | | | |
| Logical "1" Voltage | $V_{IH}$ | 3.0 | | | 3.0 | | V | |
| Logical "0" Voltage | $V_{IL}$ | | | 0.8 | | 0.8 | V | |
| Input Leakage Current | $I_{LKG}$ | | | ±1 | | ±1 | µA | |
| Input Capacitance[2] | $C_{IN}$ | | | 8 | | 8 | pF | |
| **ANALOG OUTPUTS** | | | | | | | | |
| Output Capacitance[2] | | | | | | | | |
| | $C_{OUT1}$ | | | 260 | | 260 | pF | DAC Inputs all 1's |
| | $C_{OUT1}$ | | | 100 | | 100 | pF | DAC Inputs all 0's |
| | $C_{OUT2}$ | | | 50 | | 50 | pF | DAC Inputs all 1's |
| | $C_{OUT2}$ | | | 210 | | 210 | pF | DAC Inputs all 0's |
| **POWER SUPPLY** | | | | | | | | |
| Supply Voltage[5] | $V_{DD}$ | +4.5 | | +5.5 | +4.5 | +5.5 | V | |
| Supply Current | $I_{DD}$ | | | 2.5 | | 2.5 | mA | All digital inputs = 0 V or all = 5 V |

## ELECTRICAL CHARACTERISTICS (CONT'D)

| Parameter | Symbol | 25°C Min | 25°C Typ | 25°C Max | Tmin to Tmax Min | Tmin to Tmax Max | Units | Test Conditions/Comments |
|---|---|---|---|---|---|---|---|---|
| **SWITCHING CHARACTERISTICS[2, 4]** | | | | | | | | |
| $\overline{WR}$ Pulse Width | $t_{WR}$ | 120 | | | 220 | | ns | |
| Address to $\overline{WR}$ Hold Time | $t_{AWH}$ | 50 | | | 65 | | ns | |
| $\overline{CS}$ to $\overline{WR}$ Hold Time | $t_{CWH}$ | 50 | | | 100 | | ns | |
| $\overline{CLR}$ Pulse Width | $t_{CLR}$ | 200 | | | 300 | | ns | |
| Byte Loading, $\overline{CS}$ to $\overline{WR}$ Setup | $t_{CWS1}$ | 60 | | | 130 | | ns | |
| Byte Loading, Address to $\overline{WR}$ Setup | $t_{AWS1}$ | 80 | | | 180 | | ns | |
| Byte Loading, $\overline{WR}$ to Data Setup | $t_{DS}$ | 50 | | | 65 | | ns | |
| Byte Loading, $\overline{WR}$ to Data Hold | $t_{DH}$ | 50 | | | 65 | | ns | |
| DAC Loading, $\overline{CS}$ to $\overline{WR}$ Setup | $t_{CWS2}$ | 60 | | | 150 | | ns | |
| DAC Loading, Address to $\overline{WR}$ Setup | $t_{AWS2}$ | 120 | | | 240 | | ns | |

**NOTES:**

1 Full Scale Range (FSR) is 10V for unipolar mode.
2 Guaranteed but not production tested.
3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
4 See timing diagram.
5 Specified values guarantee functionality. Refer to other parameters for accuracy.

**Specifications are subject to change without notice**

## ABSOLUTE MAXIMUM RATINGS ($T_A$ = +25°C unless otherwise noted)[1, 2, 3]

$V_{DD}$ to GND ..... +7 V
Digital Input Voltage to GND (2) . GND –0.5 to $V_{DD}$ +0.5 V
$I_{OUT1}$, $I_{OUT2}$ to GND ..... GND –0.5 to $V_{DD}$ +0.5 V
$V_{REF}$ to GND (2) ..... ±25 V
$V_{RFB}$ to GND (2) ..... ±25 V
AGND to DGND ..... ±1 V
(Functionality Guaranteed ±0.5 V)

Storage Temperature ..... –65°C to +150°C

Lead Temperature (Soldering, 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC ..... 700mW
Derates above 75°C ..... 10mW/°C

**NOTES:**

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.
3 GND refers to AGND and DGND.

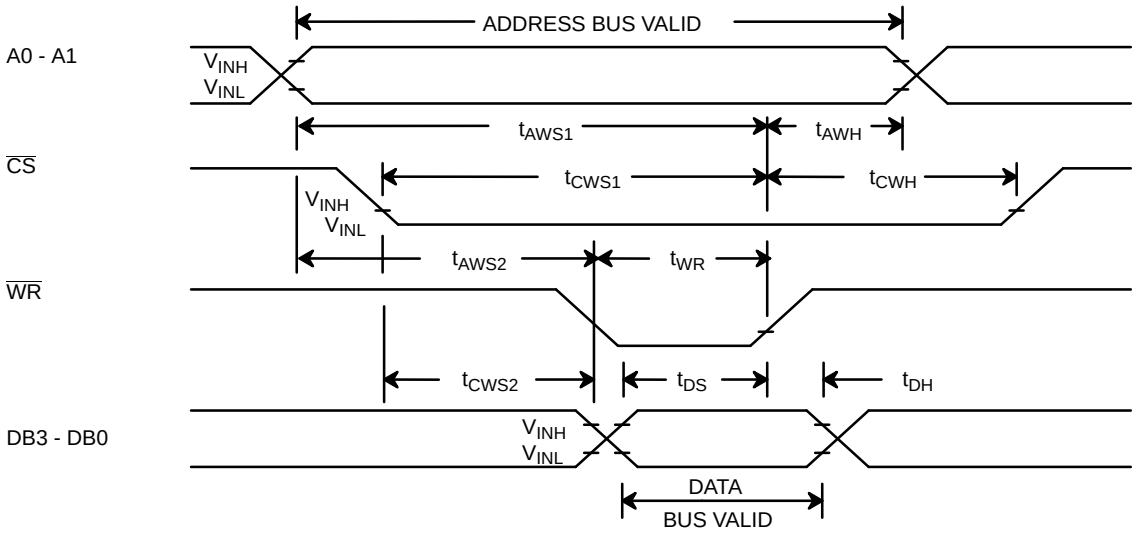



**Figure 1. Timing Diagram**

| MP7542 Control Inputs | | | | | MP7542 Operation | |
|---|---|---|---|---|---|---|
| $A_1$ | $A_0$ | $\overline{CS}$ | $\overline{WR}$ | $\overline{CLR}$ | | |
| X | X | X | X | 0 | Resets DAC 12-bit register to code 0000 0000 0000 | |
| X | X | 1 | 1 | 1 | No operation; device not selected | |
| 0 | 0 | ↗ | 0 | 1 | Load LOW byte data register on edges as shown | Load applicable data register with data at $D_0$ - $D_3$ |
| 0 | 0 | 0 | ↗ | 1 | | |
| 0 | 1 | ↗ | 0 | 1 | Load MIDDLE byte data register on edges as shown | |
| 0 | 1 | 0 | ↗ | 1 | | |
| 1 | 0 | ↗ | 0 | 1 | Load HIGH byte data register on edges as shown | |
| 1 | 0 | 0 | ↗ | 1 | | |
| 1 | 1 | 0 | 0 | 1 | Load 12-bit DAC register with data in LOW byte, MIDDLE byte, & HIGH byte data registers | |
| 1 | 1 | 0 | 0 | 1 | | |

NOTES
1. 1 indicates logic HIGH
2. 0 indicates logic LOW
3. X indicates don't care
4. ↗ indicates LOW to HIGH transition
5. MSB XXXX XXXX XXXX LSB
   high byte, middle byte, low byte
6. Although positive-going edge of either $\overline{CS}$ or $\overline{WR}$ will load data register, timing is optimized by using $\overline{WR}$ to latch data and using $\overline{CS}$ as a device enable.

**Table 1. Truth Table**

## APPLICATION NOTES
***Refer to Section 8 for Applications Information***

### Interface Logic Information

The MP7542 is designed to interface as a memory-mapped output device.

A typical system configuration is shown below. $\overline{CS}$ is the decoded device address, and is derived by decoding the 14 higher order address bits. A0 and A1 are the MP7542 operation address bits, and are decoded internally in the MP7542 to point to the desired loading operation (i.e. load high byte, middle byte, low byte or DAC register). *See Table 1.*

All data loading operations are identical to the write cycle of a RAM.

Additionally, the $\overline{CLR}$ input allows the MP7542 DAC register to be cleared asynchronously to 0000 0000 0000. When operating the MP7542 in a unipolar mode a CLEAR sets the DAC output to zero scale output. In the bipolar mode a CLEAR causes the DAC output to go to $-V_{REF}$.

In summary:

1. The MP7542 DAC register can be asynchronously cleared with the $\overline{CLR}$ input.
2. Each MP7542 requires only 4 bits of memory.
3. Any of the four basic loading operations (i.e. load low byte data register, middle byte data register, high byte data register or 12-bit DAC register) are accomplished by executing a memory WRITE operation to the applicable address location for the required DAC operation.

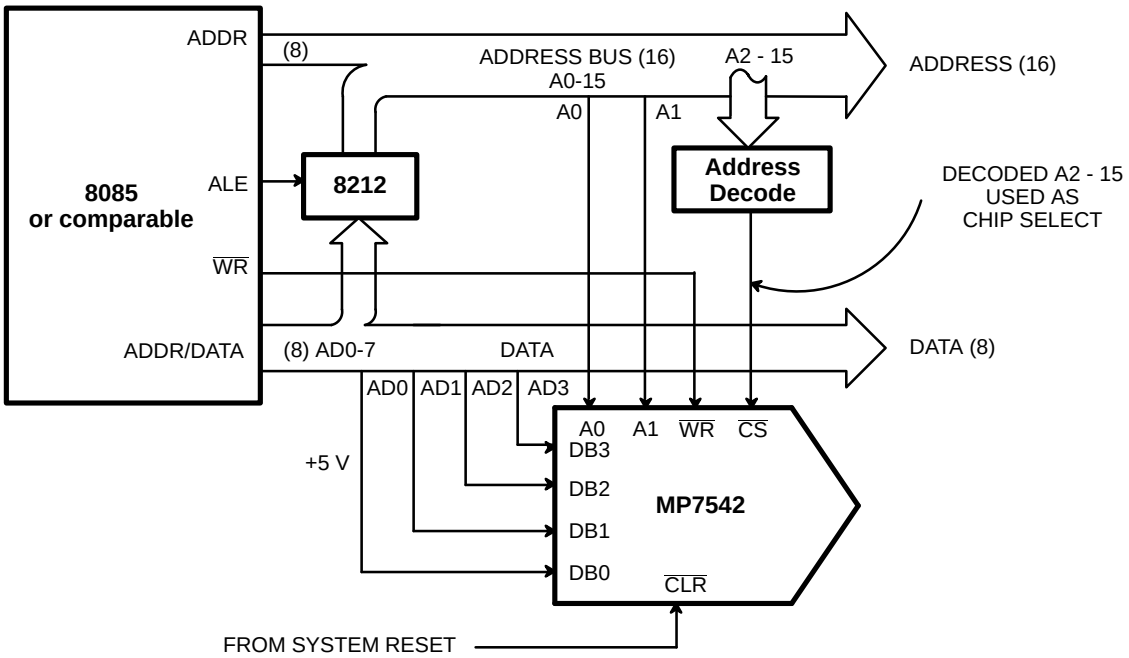
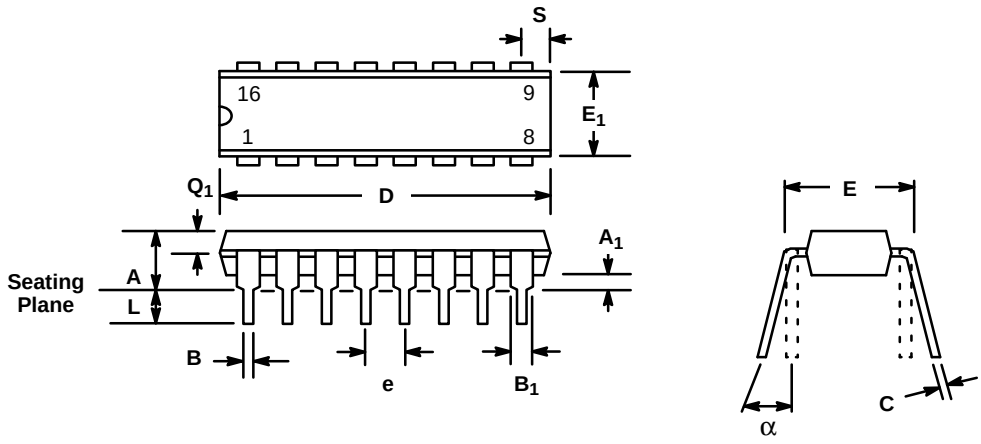



**Figure 2. 8085/MP7542 Interface (Memory Mapped Output)**

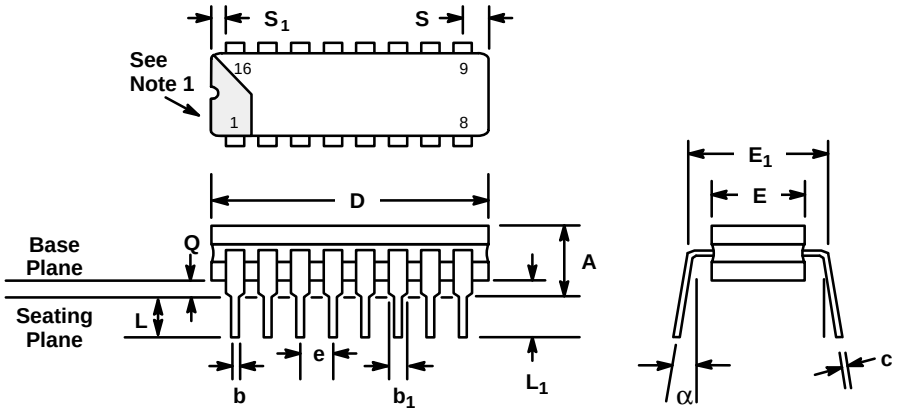
## 16 LEAD PLASTIC DUAL-IN-LINE
## (300 MIL PDIP)
## N16




| SYMBOL | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | — | 0.200 | — | 5.08 |
| $A_1$ | 0.015 | — | 0.38 | — |
| B | 0.014 | 0.023 | 0.356 | 0.584 |
| $B_1$ (1) | 0.038 | 0.065 | 0.965 | 1.65 |
| C | 0.008 | 0.015 | 0.203 | 0.381 |
| D | 0.745 | 0.785 | 18.92 | 19.94 |
| E | 0.295 | 0.325 | 7.49 | 8.26 |
| $E_1$ | 0.220 | 0.310 | 5.59 | 7.87 |
| e | 0.100 BSC | | 2.54 BSC | |
| L | 0.115 | 0.150 | 2.92 | 3.81 |
| α | 0° | 15° | 0° | 15° |
| $Q_1$ | 0.055 | 0.070 | 1.40 | 1.78 |
| S | 0.020 | 0.080 | 0.51 | 2.03 |

Note: (1) The minimum limit for dimensions B1 may be 0.023” (0.58 mm) for all four corner leads only.

## 16 LEAD CERAMIC DUAL-IN-LINE
## (300 MIL CDIP)
## D16

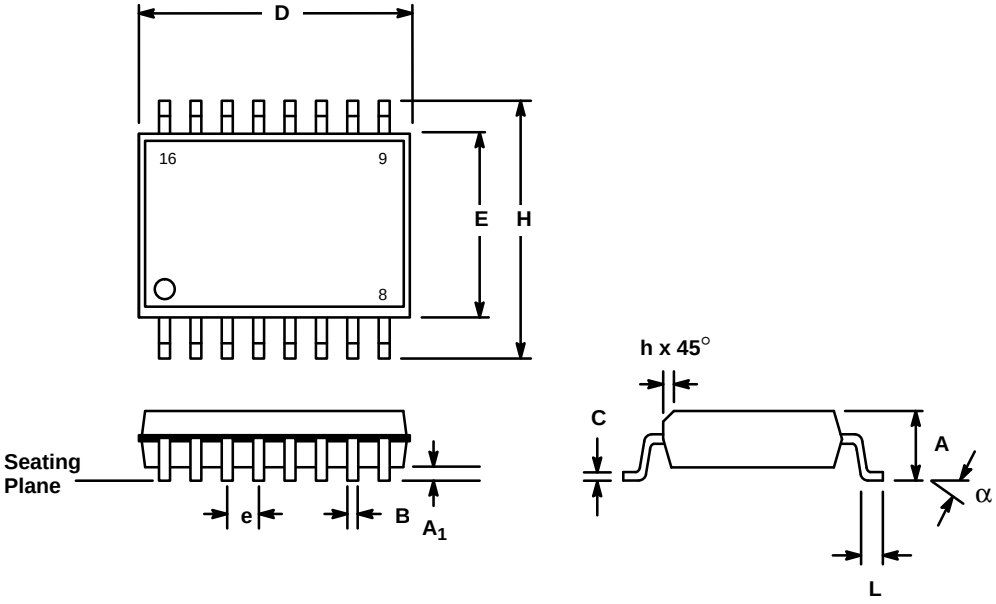



| SYMBOL | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX | NOTES |
|---|---|---|---|---|---|
| A | — | 0.200 | — | 5.08 | — |
| b | 0.014 | 0.023 | 0.356 | 0.584 | — |
| $b_1$ | 0.038 | 0.065 | 0.965 | 1.65 | 2 |
| c | 0.008 | 0.015 | 0.203 | 0.381 | — |
| D | — | 0.840 | — | 21.34 | 4 |
| E | 0.220 | 0.310 | 5.59 | 7.87 | 4 |
| $E_1$ | 0.290 | 0.320 | 7.37 | 8.13 | 7 |
| e | 0.100 BSC | | 2.54 BSC | | 5 |
| L | 0.125 | 0.200 | 3.18 | 5.08 | — |
| $L_1$ | 0.150 | — | 3.81 | — | — |
| Q | 0.015 | 0.060 | 0.381 | 1.52 | 3 |
| S | — | 0.080 | — | 2.03 | 6 |
| $S_1$ | 0.005 | — | 0.13 | — | 6 |
| α | 0° | 15° | 0° | 15° | — |

**NOTES**

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension $b_1$ may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
6. Applies to all four corners.
7. This is measured to outside of lead, not center.

## 16 LEAD SMALL OUTLINE
## (300 MIL JEDEC SOIC)
## S16




| SYMBOL | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.097 | 0.104 | 2.46 | 2.64 |
| $A_1$ | 0.0050 | 0.0115 | 0.127 | 0.292 |
| B | 0.014 | 0.019 | 0.356 | 0.482 |
| C | 0.0091 | 0.0125 | 0.231 | 0.318 |
| D | 0.402 | 0.412 | 10.21 | 10.46 |
| E | 0.292 | 0.299 | 7.42 | 7.59 |
| e | 0.050 BSC | | 1.27 BSC | |
| H | 0.400 | 0.410 | 10.16 | 10.41 |
| h | 0.010 | 0.016 | 0.254 | 0.406 |
| L | 0.016 | 0.035 | 0.406 | 0.889 |
| α | 0° | 8° | 0° | 8° |

# Notes

# Notes

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