

CD4015BC Dual 4-Bit Static Shift Register

General Description

The CD4015BC contains two identical, 4-stage, serial-input/parallel-output registers with independent "Data", "Clock," and "Reset" inputs. The logic level present at the input of each stage is transferred to the output of that stage at each positive-going clock transition. A logic high on the "Reset" input resets all four stages covered by that input. All inputs are protected from static discharge by a series resistor and diode clamps to V_{DD} and V_{SS} .

Features

- Wide supply voltage range: 3.0V to 18V
- High noise immunity: $0.45 V_{DD}$ (typ.)
- Low power TTL: Fan out of 2 driving 74L compatibility: or 1 driving 74LS
- Medium speed operation: 8 MHz (typ.) clock rate
- Fully static design: @ $V_{DD} - V_{SS} = 10V$

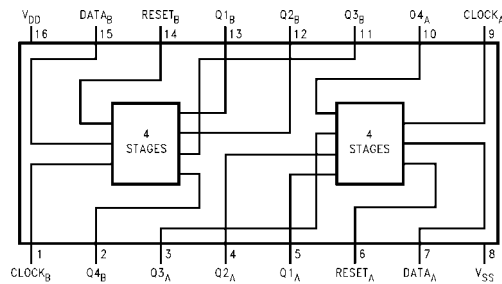
Applications

- Serial-input/parallel-output data queueing
- Serial to parallel data conversion
- General purpose register

Ordering Code:

Order Number	Package Number	Package Description
CD4015BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4015BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram



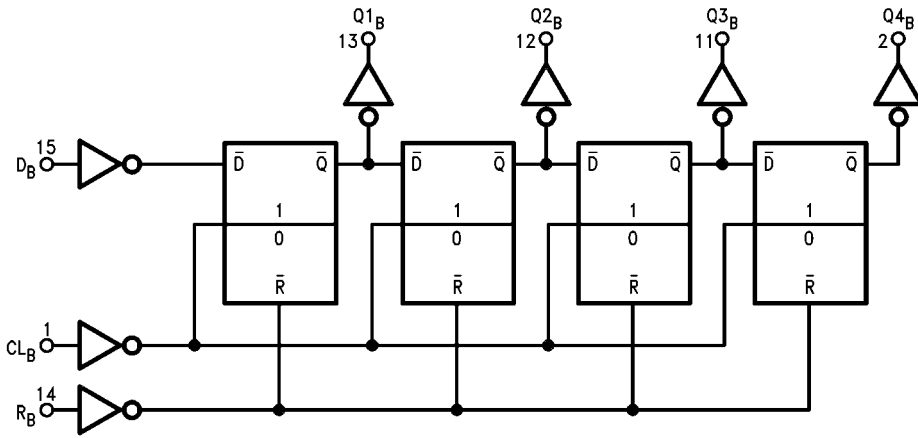
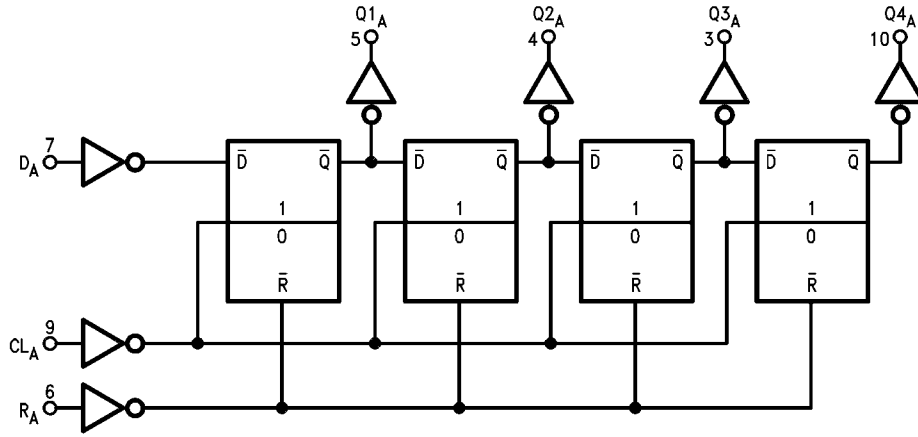
Truth Table

CL (Note 1)	D	R	Q ₁	Q _n	
↘	0	0	0	Q _{n-1}	(No change)
↗	1	0	1	Q _{n-1}	
↖	X	0	Q ₁	Q _n	
X	X	1	0	0	

X = Don't Care Case

Note 1: Level Change

Logic Diagrams



Terminal No. 16 = V_{DD}
Terminal No. 8 = GND

Absolute Maximum Ratings ^(Note 2)		Recommended Operating Conditions	
^(Note 3)			
DC Supply Voltage (V_{DD})	-0.5 to +18 V_{DC}	DC Supply Voltage (V_{DD})	+3 to +15 V_{DC}
Input Voltage (V_{IN})	-0.5 to $V_{DD} + 0.5 V_{DC}$	Input Voltage (V_{IN})	0 to $V_{DD} V_{DC}$
Storage Temperature Range (T_S)	-65°C to +150°C	Operating Temperature Range (T_A)	-55°C to +125°C
Power Dissipation (P_D)			
Dual-In-Line	700 mW		
Small Outline	500 mW		
Lead Temperature (T_L)			
(Soldering, 10 seconds)	260°C		

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 3: $V_{SS} = 0V$ unless otherwise specified.

DC Electrical Characteristics ^(Note 3)

Symbol	Parameter	Conditions	-55°C		+25°C			+125°C		Units	
			Min	Max	Min	Typ	Max	Min	Max		
I_{DD}	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or V_{SS}		5		0.005	5		150	μA	
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or V_{SS}		10		0.010	10		300		
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or V_{SS}		20		0.015	20		600		
V_{OL}	LOW Level Output Voltage	$V_{DD} = 5V$		0.05		0	0.05		0.05	V	
		$V_{DD} = 10V$	$ I_{OL} < 1 \mu A$		0.05		0	0.05			0.05
		$V_{DD} = 15V$			0.05		0	0.05			0.05
V_{OH}	HIGH Level Output Voltage	$V_{DD} = 5V$	4.95		4.95	5		4.95		V	
		$V_{DD} = 10V$	9.95		9.95	10		9.95			
		$V_{DD} = 15V$	14.95		14.95	15		14.95			
V_{IL}	LOW Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V	
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$		3.0		4.50	3.0		3.0		
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0		
V_{IH}	HIGH Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V	
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$	7.0		7.0	5.50		7.0			
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0			
I_{OL}	LOW Level Output Current (Note 4)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA	
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.9			
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8.8		2.4			
I_{OH}	HIGH Level Output Current (Note 4)	$V_{DD} = 5V, V_O = 4.6V$	-0.64		-0.51	-0.88		-0.36		mA	
		$V_{DD} = 10V, V_O = 9.5V$	-1.6		-1.3	-2.25		-0.9			
		$V_{DD} = 15V, V_O = 13.5V$	-4.2		-3.4	-8.8		-2.4			
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.1		-10^{-5}	-0.1		-1.0	μA	
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0		

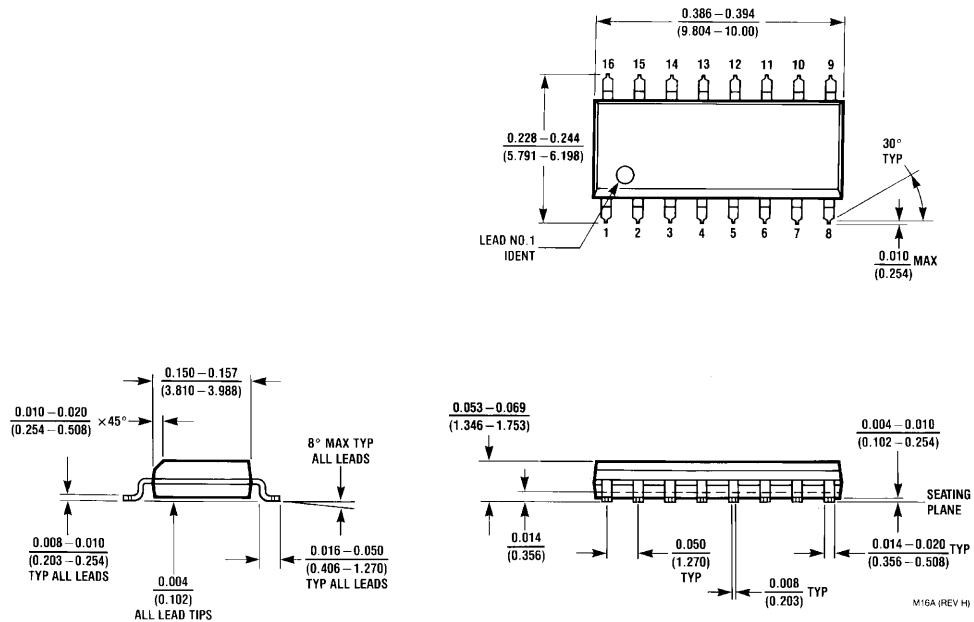
Note 4: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics (Note 5)T_A = 25°C, C_L = 50 pF, R_L = 200k, t_r = t_f = 20 ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CLOCK OPERATION						
t _{PHL} , t _{PLH}	Propagation Delay Time	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		230 80 60	350 160 120	ns
t _{THL} , t _{TLH}	Transition Time	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		100 50 40	200 100 80	ns
t _{WL} , t _{WM}	Minimum Clock Pulse-Width	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		160 60 50	250 110 85	ns
t _{rCL} , t _{fCL}	Clock Rise and Fall Time	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V			15 15 15	μs
t _{SU}	Minimum Data Set-Up Time	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		50 20 15	100 40 30	μs
f _{CL}	Maximum Clock Frequency	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V	2 4.5 6	3.5 8 11		MHz
C _{IN}	Input Capacitance	Clock Input Other Inputs		7.5 5	10 7.5	pF
RESET OPERATION						
t _{PHL(R)}	Propagation Delay Time	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		200 100 80	400 200 160	ns
t _{WH(R)}	Minimum Reset Pulse Width	V _{DD} = 5V V _{DD} = 10V V _{DD} = 15V		135 40 30	250 80 60	ns

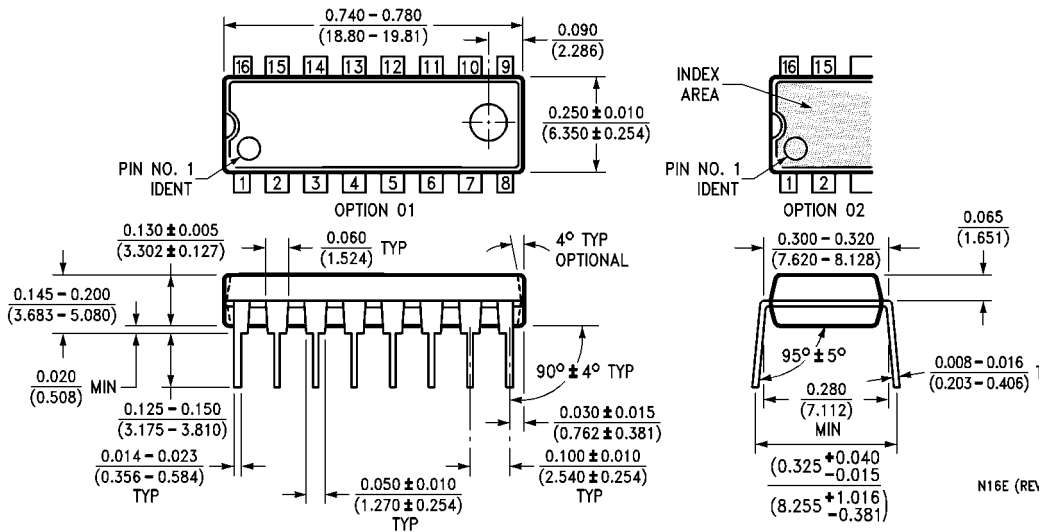
Note 5: AC Parameters are guaranteed by DC correlated testing.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com