

## CD4017BC • CD4022BC

### Decade Counter/Divider with 10 Decoded Outputs • Divide-by-8 Counter/Divider with 8 Decoded Outputs

#### General Description

The CD4017BC is a 5-stage divide-by-10 Johnson counter with 10 decoded outputs and a carry out bit.

The CD4022BC is a 4-stage divide-by-8 Johnson counter with 8 decoded outputs and a carry-out bit.

These counters are cleared to their zero count by a logical "1" on their reset line. These counters are advanced on the positive edge of the clock signal when the clock enable signal is in the logical "0" state.

The configuration of the CD4017BC and CD4022BC permits medium speed operation and assures a hazard free counting sequence. The 10/8 decoded outputs are normally in the logical "0" state and go to the logical "1" state only at their respective time slot. Each decoded output remains high for 1 full clock cycle. The carry-out signal completes a full cycle for every 10/8 clock input cycles and is used as a ripple carry signal to any succeeding stages.

#### Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45  $V_{DD}$  (typ.)
- Low power Fan out of 2 driving 74L TTL compatibility: or 1 driving 74LS
- Medium speed operation: 5.0 MHz (typ.) with 10V  $V_{DD}$
- Low power: 10  $\mu$ W (typ.)
- Fully static operation

#### Applications

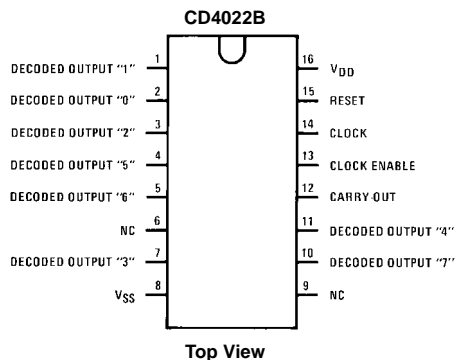
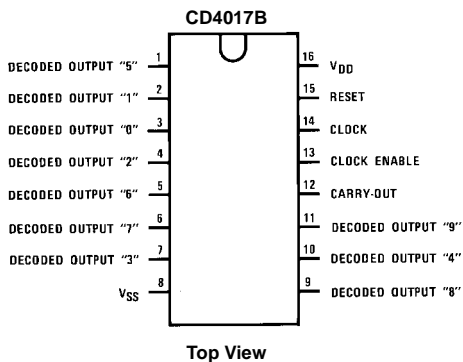
- Automotive
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering

#### Ordering Code:

Order Number	Package Number	Package Description
CD4017BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4017BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
CD4022BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4022BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

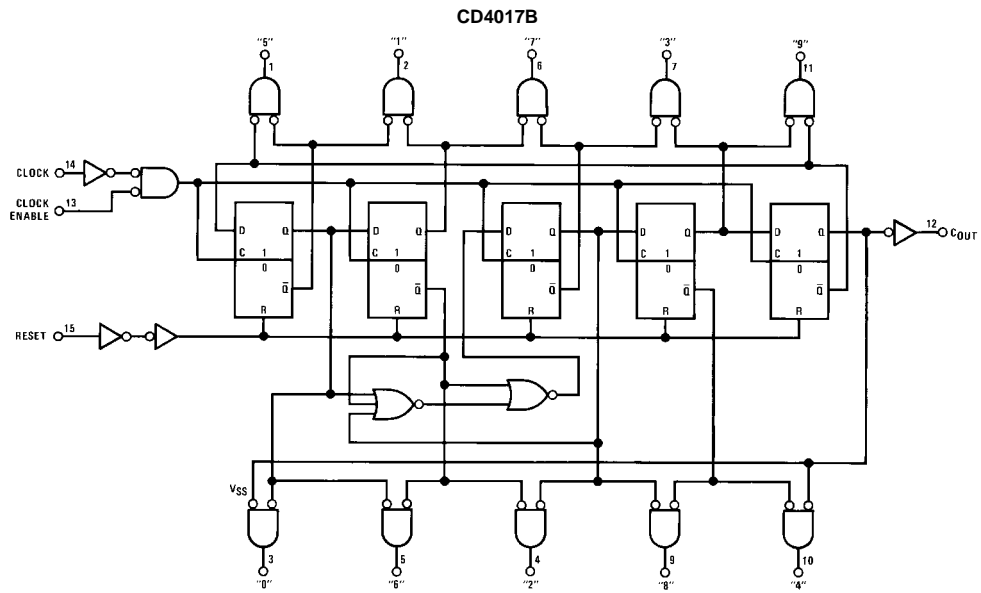
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Connection Diagrams

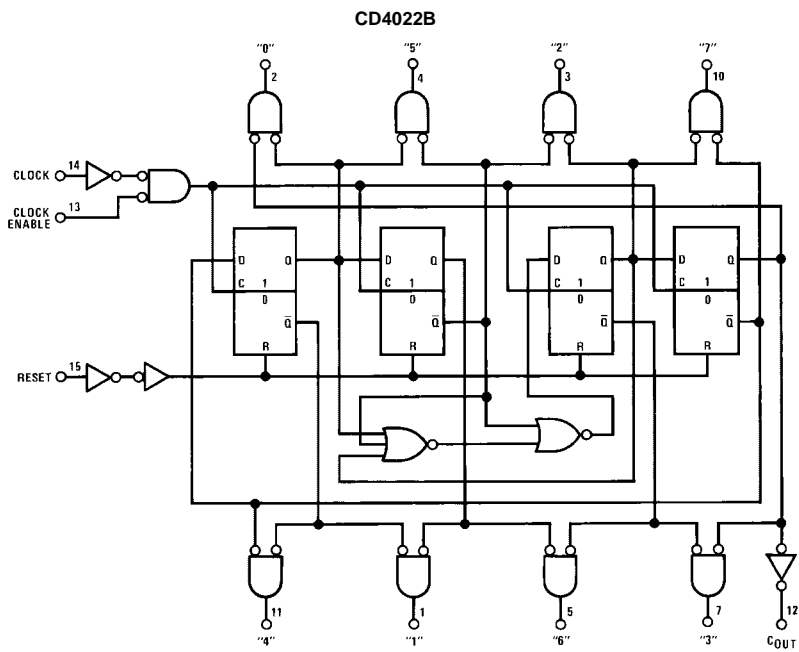


CD4017BC • CD4022BC Decade Counter/Divider with 10 Decoded Outputs • Divide-by-8 Counter/Divider with 8 Decoded Outputs

Logic Diagrams



Terminal No. 8 = GND  
Terminal No. 16 = V<sub>DD</sub>



Terminal No. 16 = V<sub>DD</sub>  
Terminal No. 8 = GND

Absolute Maximum Ratings (Note 1)		Recommended Operating Conditions (Note 2)	
DC Supply Voltage ( $V_{DD}$ )	-0.5 $V_{DC}$ to +18 $V_{DC}$	DC Supply Voltage ( $V_{DD}$ )	+3 $V_{DC}$ to +15 $V_{DC}$
Input Voltage ( $V_{IN}$ )	-0.5 $V_{DC}$ to $V_{DD}$ +0.5 $V_{DC}$	Input Voltage ( $V_{IN}$ )	0 to $V_{DD}$ $V_{DC}$
Storage Temperature ( $T_S$ )	-65°C to +150°C	Operating Temperature Range ( $T_A$ )	-55°C to +125°C
Power Dissipation ( $P_D$ )			
Dual-In-Line	700 mW		
Small Outline	500 mW		
Lead Temperature ( $T_L$ )			
(Soldering, 10 seconds)	260°C		

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:**  $V_{SS} = 0V$  unless otherwise specified.

### DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	-55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device Current	$V_{DD} = 5V$		5		0.3	5		150	$\mu A$
		$V_{DD} = 10V$		10		0.5	10		300	
		$V_{DD} = 15V$		20		1.0	20		600	
$V_{OL}$	LOW Level Output Voltage	$ I_{OL}  < 1.0 \mu A$								V
		$V_{DD} = 5V$		0.05		0	0.05		0.05	
		$V_{DD} = 10V$		0.05		0	0.05		0.05	
		$V_{DD} = 15V$		0.05		0	0.05		0.05	
$V_{OH}$	HIGH Level Output Voltage	$ I_{OL}  < 1.0 \mu A$								V
		$V_{DD} = 5V$	4.95		4.95	5		4.95		
		$V_{DD} = 10V$	9.95		9.95	10		9.95		
		$V_{DD} = 15V$	14.95		14.95	15		14.95		
$V_{IL}$	LOW Level Input Voltage	$ I_{OL}  < 1.0 \mu A$								V
		$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$		1.5			1.5		1.5	
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$		3.0			3.0		3.0	
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		4.0			4.0		4.0	
$V_{IH}$	HIGH Level Input Voltage	$ I_{OL}  < 1.0 \mu A$								V
		$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$	7.0		7.0			7.0		
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		
$I_{OL}$	LOW Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.9		
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8.8		2.4		
$I_{OH}$	HIGH Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	-0.25		-0.2	-0.36		-0.14		mA
		$V_{DD} = 10V, V_O = 9.5V$	-0.62		-0.5	-0.9		-0.35		
		$V_{DD} = 15V, V_O = 13.5V$	-1.8		-1.5	-3.5		-1.1		
$I_{IN}$	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.1		$-10^{-5}$	-0.1		-1.0	$\mu A$
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		$10^{-5}$	0.1		1.0	

**Note 3:**  $I_{OL}$  and  $I_{OH}$  are tested one output at a time.

### AC Electrical Characteristics (Note 4)

T<sub>A</sub> = 25°C, C<sub>L</sub> = 50 pF, R<sub>L</sub> = 200k, t<sub>rCL</sub> and t<sub>fCL</sub> = 20 ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>CLOCK OPERATION</b>						
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Time Carry Out Line	V <sub>DD</sub> = 5V		415	800	ns
		V <sub>DD</sub> = 10V		160	320	
		V <sub>DD</sub> = 15V		130	250	
	Carry Out Line	V <sub>DD</sub> = 5V	C <sub>L</sub> = 15 pF	240	480	ns
		V <sub>DD</sub> = 10V		85	170	
		V <sub>DD</sub> = 15V		70	140	
	Decode Out Lines	V <sub>DD</sub> = 5V		500	1000	ns
		V <sub>DD</sub> = 10V		200	400	
		V <sub>DD</sub> = 15V		160	320	
t <sub>TLH</sub> , t <sub>THL</sub>	Transition Time Carry Out and Decode Out Lines	V <sub>DD</sub> = 5V		200	360	ns
		V <sub>DD</sub> = 10V		100	180	
		V <sub>DD</sub> = 15V		80	130	
	t <sub>THL</sub>	V <sub>DD</sub> = 5V		100	200	ns
		V <sub>DD</sub> = 10V		50	100	
		V <sub>DD</sub> = 15V		40	80	
f <sub>CL</sub>	Maximum Clock Frequency	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V	Measured with Respect to Carry Output Line	1.0 2.5 3.0	2 5 6	MHz
t <sub>WL</sub> , t <sub>WH</sub>	Minimum Clock Pulse Width	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		125 45 35	250 90 70	ns
t <sub>rCL</sub> , t <sub>fCL</sub>	Clock Rise and Fall Time	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V			20 15 5	μs
t <sub>SU</sub>	Minimum Clock Inhibit Data Setup Time	V <sub>DD</sub> = 5V V <sub>DD</sub> = 10V V <sub>DD</sub> = 15V		120 40 32	240 80 65	ns
C <sub>IN</sub>	Average Input Capacitance			5	7.5	pF

Note 4: AC Parameters are guaranteed by DC correlated testing.

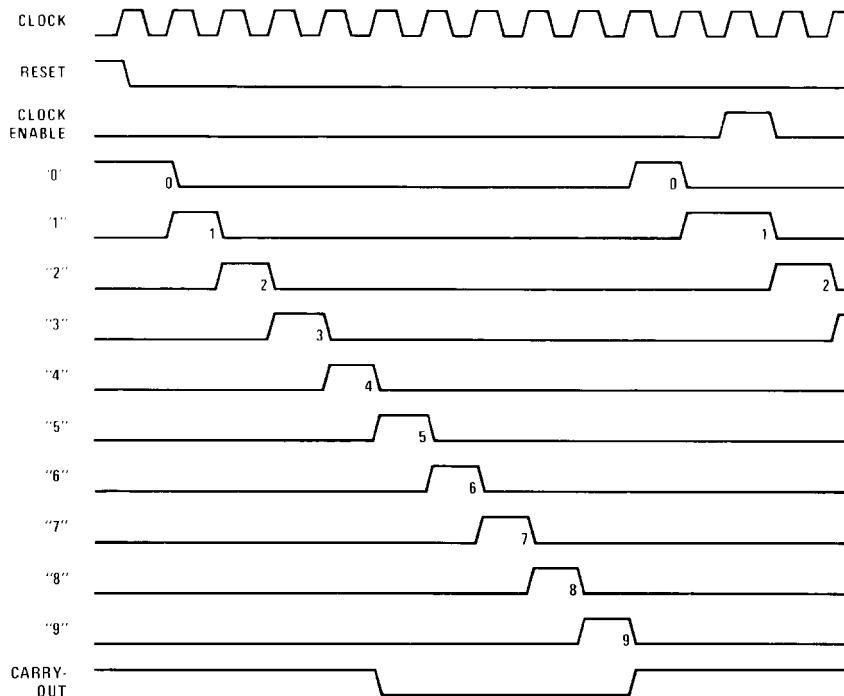
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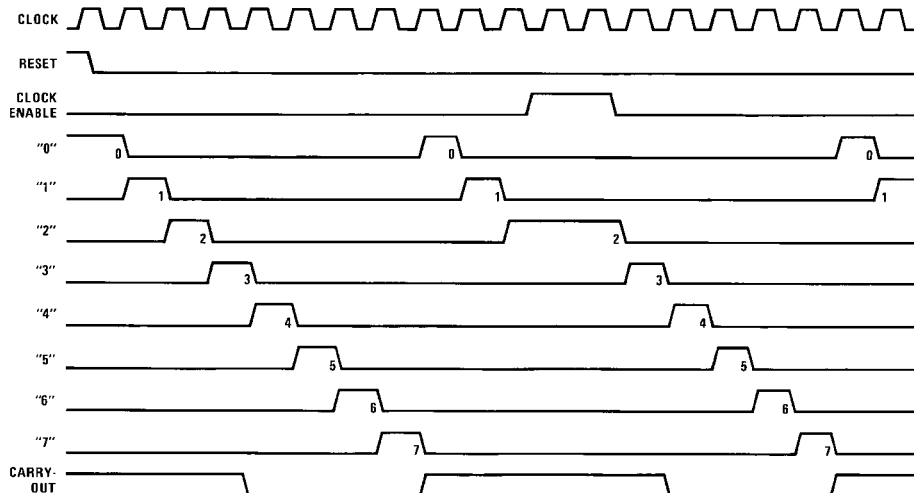
Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>RESET OPERATION</b>						
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Time Carry Out Line	V <sub>DD</sub> = 5V		415	800	ns
		V <sub>DD</sub> = 10V		160	320	
		V <sub>DD</sub> = 15V		130	250	
	Carry Out Line	V <sub>DD</sub> = 5V	C <sub>L</sub> = 15 pF	240	480	ns
		V <sub>DD</sub> = 10V		85	170	
		V <sub>DD</sub> = 15V		70	140	
	Decode Out Lines	V <sub>DD</sub> = 5V		500	1000	ns
		V <sub>DD</sub> = 10V		200	400	
		V <sub>DD</sub> = 15V		160	320	
t <sub>W</sub>	Minimum Reset Pulse Width	V <sub>DD</sub> = 5V		200	400	ns
		V <sub>DD</sub> = 10V		70	140	
		V <sub>DD</sub> = 15V		55	110	
t <sub>REM</sub>	Minimum Reset Removal Time	V <sub>DD</sub> = 5V		75	150	ns
		V <sub>DD</sub> = 10V		30	60	
		V <sub>DD</sub> = 15V		25	50	

### Timing Diagrams

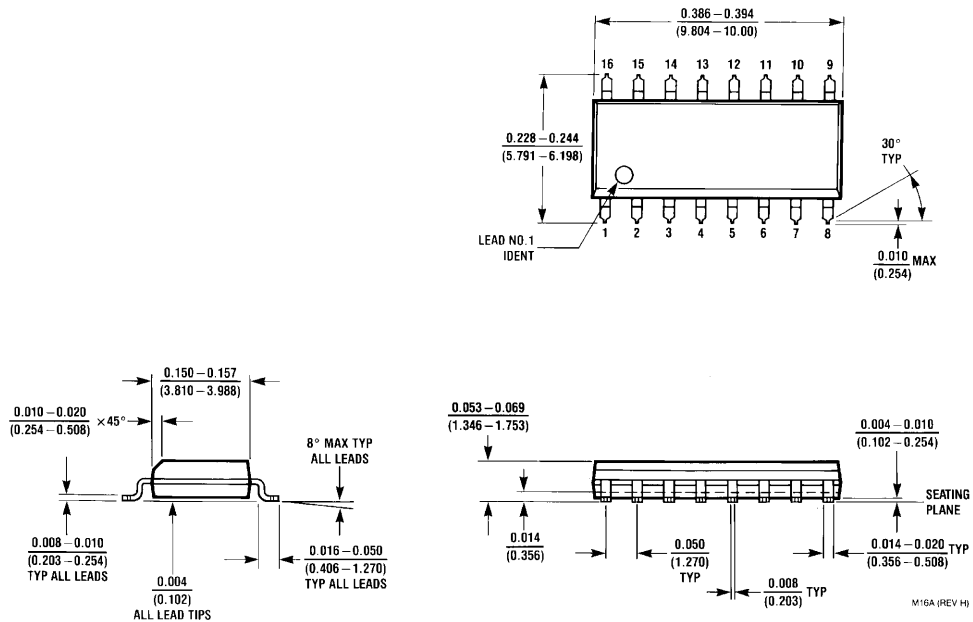
CD4017B



CD4022B

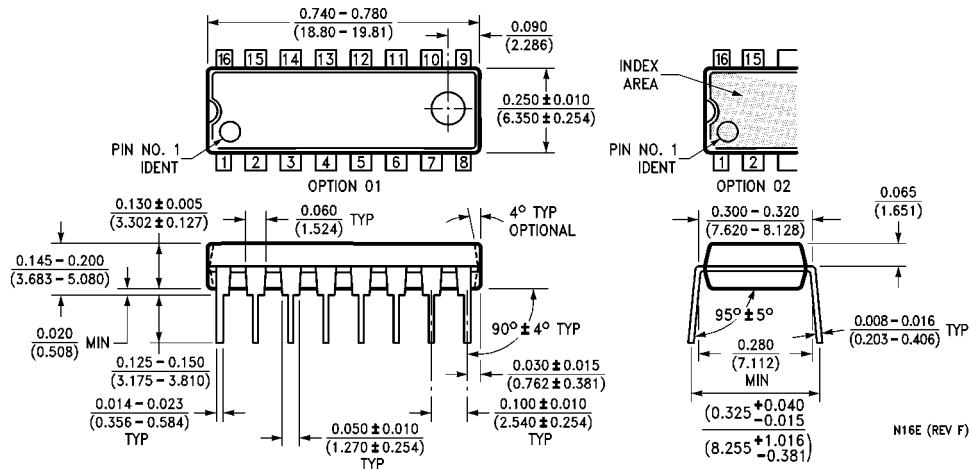


**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E**

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