

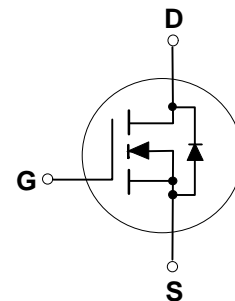
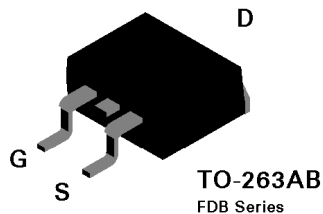
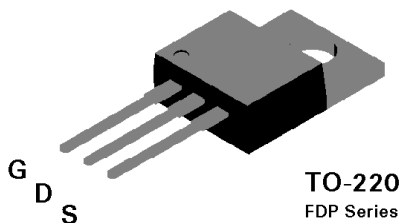
## FDP7030L / FDB7030L N-Channel Logic Level Enhancement Mode Field Effect Transistor

### General Description

These N-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as DC/DC converters and high efficiency switching circuits where fast switching, low in-line power loss, and resistance to transients are needed.

### Features

- 100 A, 30 V.  $R_{DS(ON)} = 0.007 \Omega @ V_{GS}=10 \text{ V}$   
 $R_{DS(ON)} = 0.010 \Omega @ V_{GS}=5 \text{ V}$ .
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- High density cell design for extremely low  $R_{DS(ON)}$ .
- 175°C maximum junction temperature rating.



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDP7030L	FDB7030L	Units
$V_{DSS}$	Drain-Source Voltage	30		V
$V_{GSS}$	Gate-Source Voltage - Continuous	±20		V
$I_D$	Drain Current - Continuous (Note 1)	100		A
	- Pulsed (Note 1)	75		
$P_D$	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	125		W
	Derate above $25^\circ\text{C}$	0.83		
$T_J, T_{STG}$	Operating and Storage Temperature Range	-65 to 175		$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		$^\circ\text{C}$
<b>THERMAL CHARACTERISTICS</b>				
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.2		$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5		$^\circ\text{C}/\text{W}$

**Electrical Characteristics** ( $T_c = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>DRAIN-SOURCE AVALANCHE RATINGS</b> (Note 1)						
$W_{DSS}$	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 15\text{ V}, I_D = 38\text{ A}$			200	mJ
$I_{AR}$	Maximum Drain-Source Avalanche Current				38	A
<b>OFF CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		36		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ $T_J = 125^\circ\text{C}$			10	$\mu\text{A}$
					1	mA
$I_{GSSF}$	Gate - Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
<b>ON CHARACTERISTICS</b> (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	1.5	2	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-5		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 50\text{ A}$ $T_J = 125^\circ\text{C}$		0.006	0.007	$\Omega$
				0.009	0.011	
				$V_{GS} = 5\text{ V}, I_D = 40\text{ A}$		0.009
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 10\text{ V}$	60			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 50\text{ A}$		50		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		2150		pF
$C_{oss}$	Output Capacitance			1290		pF
$C_{rss}$	Reverse Transfer Capacitance			420		pF
<b>SWITCHING CHARACTERISTICS</b> (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = 15\text{ V}, I_D = 75\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega,$ $R_{GS} = 10\ \Omega$		10	20	nS
$t_T$	Turn - On Rise Time			160	225	nS
$t_{D(off)}$	Turn - Off Delay Time			70	95	nS
$t_f$	Turn - Off Fall Time			140	195	nS
$Q_g$	Total Gate Charge		$V_{DS} = 12\text{ V}$ $I_D = 50\text{ A}, V_{GS} = 4.5\text{ V}$		35	50
$Q_{gs}$	Gate-Source Charge			12		nC
$Q_{gd}$	Gate-Drain Charge			18		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current (Note 1)				100	A
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current (Note 2)				300	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 50\text{ A}$ (Note 2) $T_J = 125^\circ\text{C}$		1	1.3	V
				0.85	1.1	

**Notes**

1. Calculated continuous current based on maximum allowable junction temperature. Actual maximum continuous current limited by package constraints to 75A.
2. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

## Typical Electrical Characteristics

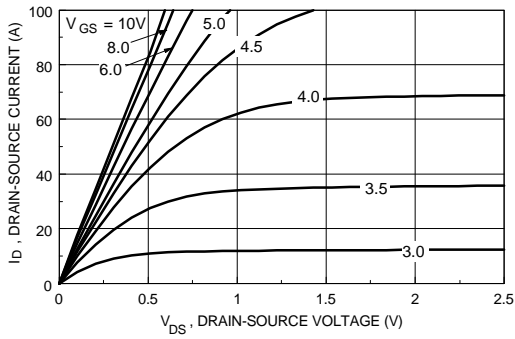


Figure 1. On-Region Characteristics.

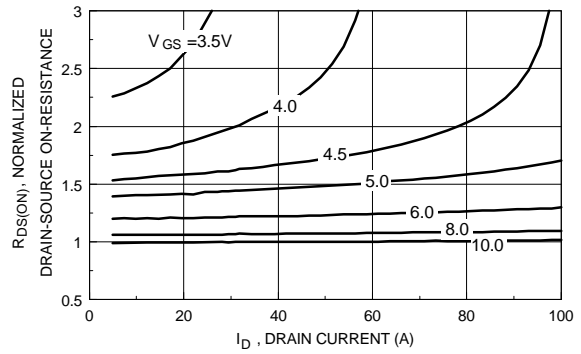


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

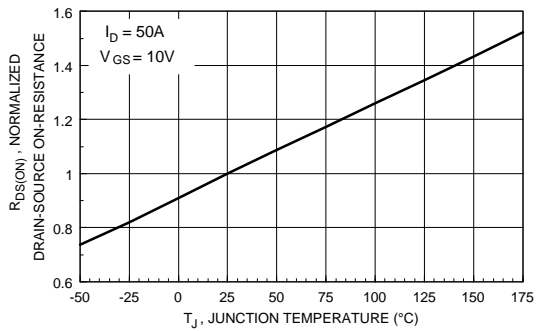


Figure 3. On-Resistance Variation with Temperature.

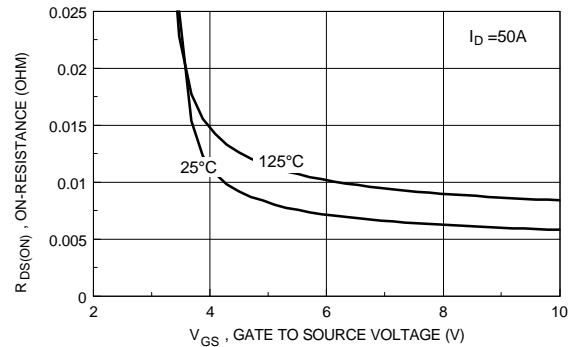


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

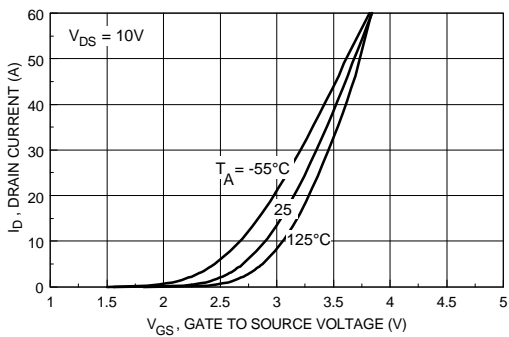


Figure 5. Transfer Characteristics.

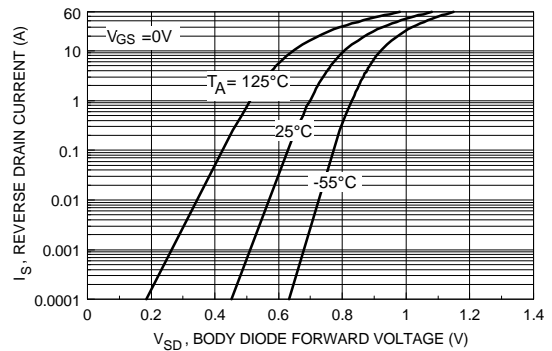


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

### Typical Electrical Characteristics (continued)

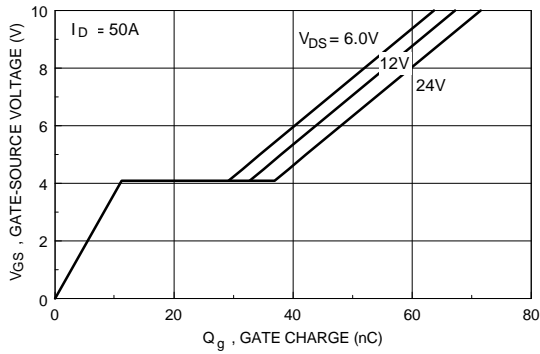


Figure 7. Gate Charge Characteristics.

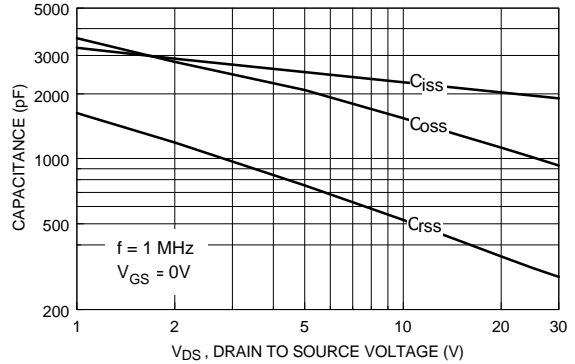


Figure 8. Capacitance Characteristics.

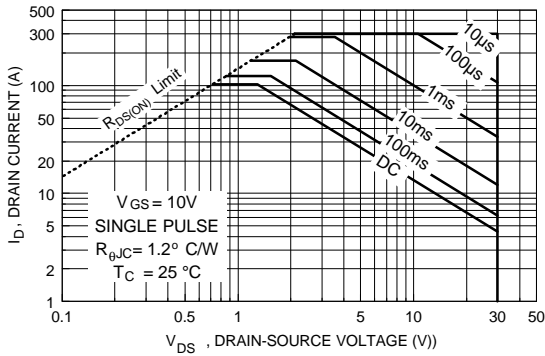


Figure 9. Maximum Safe Operating Area.

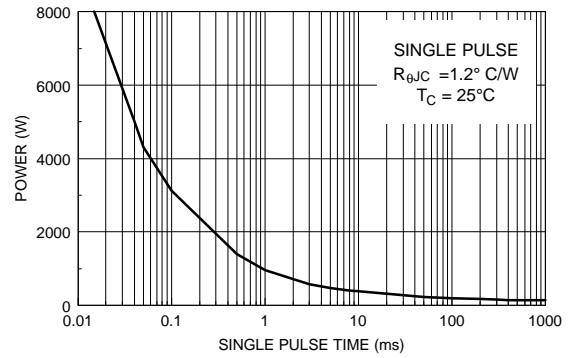


Figure 10. Single Pulse Maximum Power Dissipation.

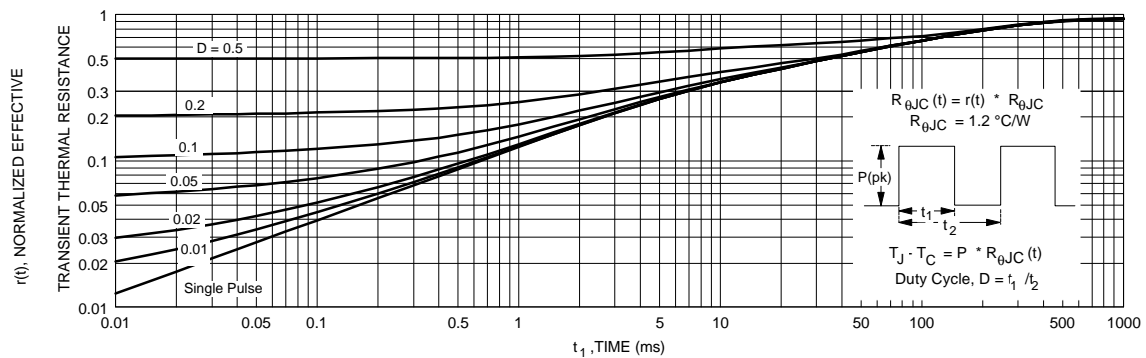


Figure 11. Transient Thermal Response Curve.

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