FAIRCHILD SEMICONDUCTOR®

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# FDM606P

## P-Channel 1.8V Logic Level Power Trench® MOSFET

### General Description

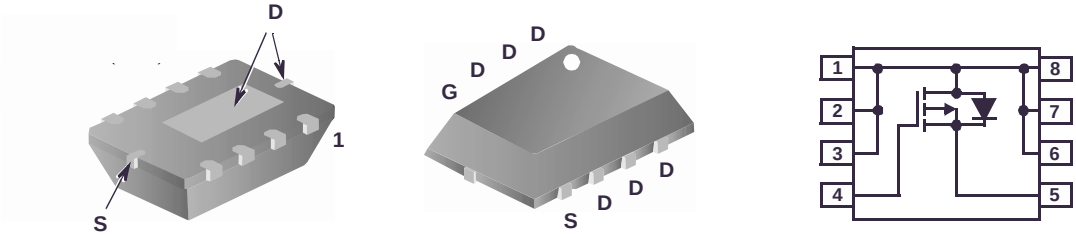
This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance. These devices are well suited for portable electronics applications.

### Features

- Fast switching
- $r_{DS(ON)}$ = 0.026Ω (Typ), $V_{GS}$ = -4.5V
- $r_{DS(ON)}$ = 0.033Ω (Typ), $V_{GS}$ = -2.5V
- $r_{DS(ON)}$ = 0.052Ω (Typ), $V_{GS}$ = -1.8V

### Applications

- Load switch
- Battery charge
- Battery disconnect circuits




MicroFET 3x2-8

## MOSFET Maximum Ratings $T_A$=25°C unless otherwise noted

| Symbol | Parameter | Ratings | Units |
|---|---|---|---|
| $V_{DSS}$ | Drain to Source Voltage | -20 | V |
| $V_{GS}$ | Gate to Source Voltage | ±8 | V |
| $I_D$ | Drain Current<br>Continuous ($T_C$ = 25°C, $V_{GS}$ = - 4.5V) | -6.8 | A |
| | Continuous ($T_C$ = 100°C, $V_{GS}$ = - 2.5V) | -3.8 | A |
| | Continuous ($T_C$ = 100°C, $V_{GS}$ = -1.8V) | -3.0 | A |
| | Pulsed | Figure 4 | |
| $P_D$ | Power dissipation<br>Derate above 25°C | 1.92<br>15.4 | W<br>mW/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature | -55 to 150 | °C |

## Thermal Characteristics

| | | | |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance Junction to Case (Note1) | 6.0 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance Junction to Ambient (Note 2) | 65 | °C/W |

## Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| .06P | FDM606P | MicroFET3x2 | 178 mm | 8 mm | 3000 |

## Electrical Characteristics $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | | |
| $B_{VDSS}$ | Drain to Source Breakdown Voltage | $I_D$ = -250µA, $V_{GS}$ = 0V | | -20 | - | - | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = -16V, $V_{GS}$ = 0V | | - | - | -1 | µA |
| | | | $T_A$=100°C | - | - | -5 | |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±8V | | - | - | ±100 | nA |
| **On Characteristics** | | | | | | | |
| $V_{GS(TH)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = -250µA | | -0.4 | -0.9 | -1.5 | V |
| $r_{DS(ON)}$ | Drain to Source On Resistance | $I_D$ = -6.8A, $V_{GS}$ = -4.5V | | - | 0.026 | 0.030 | Ω |
| | | $I_D$ = -3.8A, $V_{GS}$ = -2.5V | | - | 0.033 | 0.038 | |
| | | $I_D$ = -3.0A, $V_{GS}$ = -1.8V | | - | 0.052 | 0.070 | |
| **Dynamic Characteristics** | | | | | | | |
| $C_{ISS}$ | Input Capacitance | $V_{DS}$ = -10V, $V_{GS}$ = 0V, f = 1MHz | | - | 2200 | - | pF |
| $C_{OSS}$ | Output Capacitance | | | - | 350 | - | pF |
| $C_{RSS}$ | Reverse Transfer Capacitance | | | - | 160 | - | pF |
| $Q_{g(TOT)}$ | Total Gate Charge at -4.5V | $V_{GS}$ = 0V to -4.5V | $V_{DD}$ = -10V, $I_D$ = -3.0A, $I_g$ = 1.0mA | - | 20 | 30 | nC |
| $Q_{g(-2.5)}$ | Total Gate Charge at -2.5V | $V_{GS}$ = 0V to -2.5V | | - | 12 | 18 | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | | | - | 3.0 | - | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | | - | 3.8 | - | nC |
| **Switching Characteristics** ($V_{GS}$ = -4.5V) | | | | | | | |
| $t_{ON}$ | Turn-On Time | $V_{DD}$ = -10V, $I_D$ = -3.0A, $V_{GS}$ = -4.5V, $R_{GS}$ = 6.8Ω | | - | - | 81 | ns |
| $t_{d(ON)}$ | Turn-On Delay Time | | | - | 9 | - | ns |
| $t_r$ | Rise Time | | | - | 46 | - | ns |
| $t_{d(OFF)}$ | Turn-Off Delay Time | | | - | 134 | - | ns |
| $t_f$ | Fall Time | | | - | 71 | - | ns |
| $t_{OFF}$ | Turn-Off Time | | | - | - | 308 | ns |
| **Drain-Source Diode Characteristics** | | | | | | | |
| $V_{SD}$ | Source to Drain Diode Voltage | $I_{SD}$ = -6.8A | | - | -0.9 | -1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_{SD}$ = -3.0A, $dI_{SD}/dt$ = 100A/µs | | - | - | 28 | ns |
| $Q_{RR}$ | Reverse Recovered Charge | $I_{SD}$ = -3.0A, $dI_{SD}/dt$ = 100A/µs | | - | - | 20 | nC |

**Notes:**

**1.** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the center drain pad. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by user’s board design.

**2.** $R_{\theta JA}$ is 65 °C/W (steady state) when mounted on a 1 inch$^2$ copper pad on FR-4.

## Typical Characteristic $T_A$ = 25°C unless otherwise noted

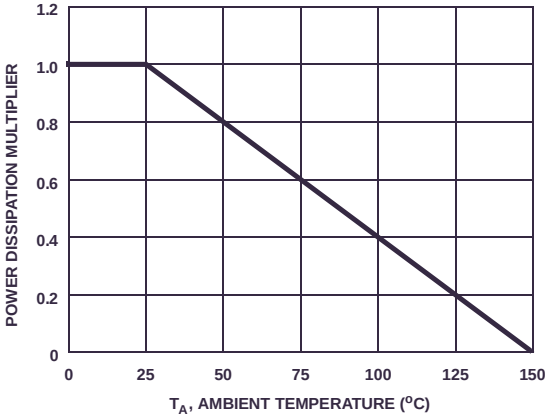



**Figure 1. Normalized Power Dissipation vs Ambient Temperature**

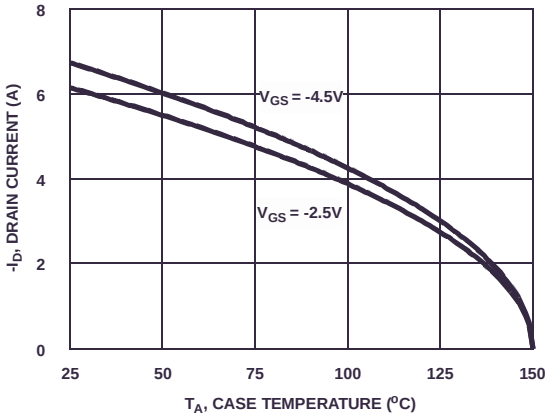



**Figure 2. Maximum Continuous Drain Current vs Case Temperature**

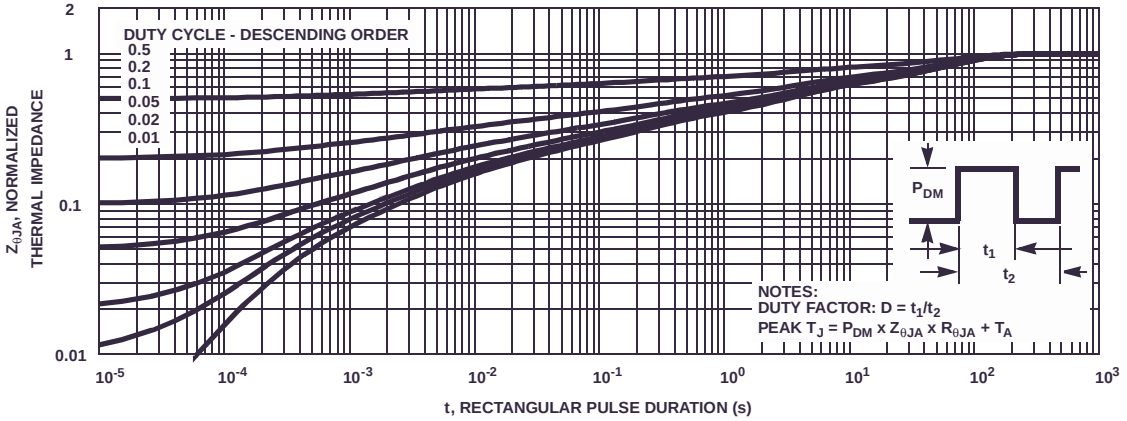



**Figure 3. Normalized Maximum Transient Thermal Impedance**

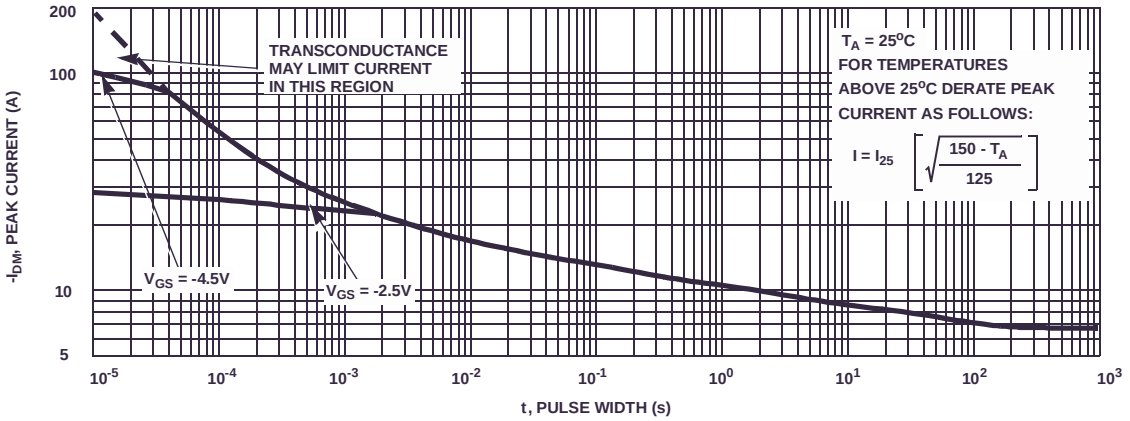



**Figure 4. Peak Current Capability**

## Typical Characteristic (Continued) $T_A$ = 25°C unless otherwise noted

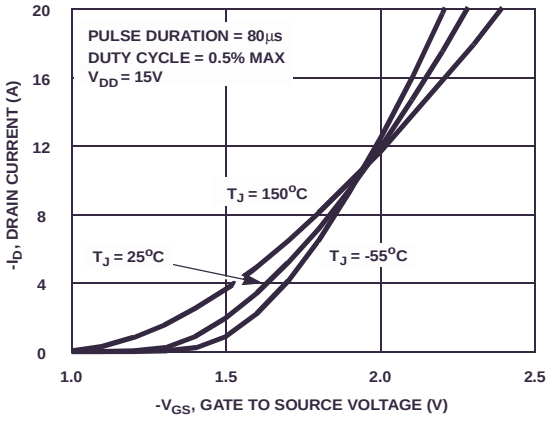



**Figure 5. Transfer Characteristics**

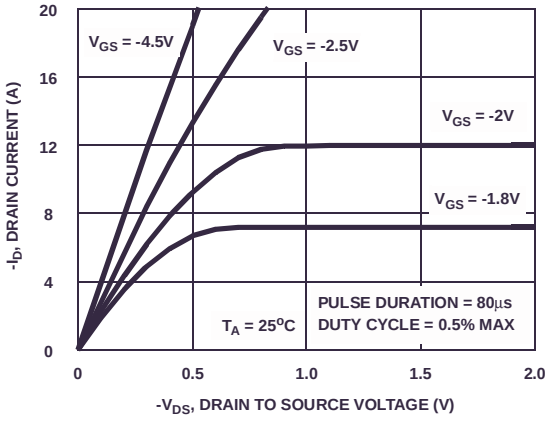



**Figure 6. Saturation Characteristics**

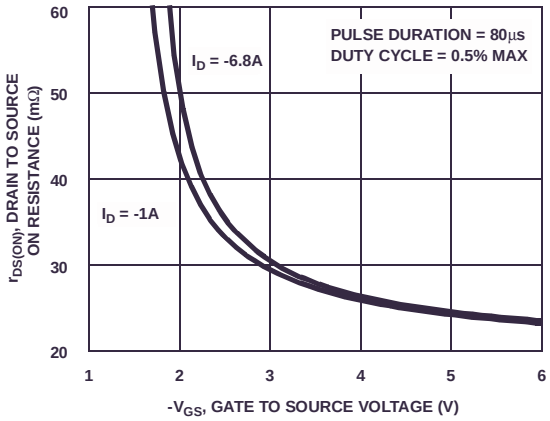



**Figure 7. Drain to Source On Resistance vs Gate Voltage and Drain Current**

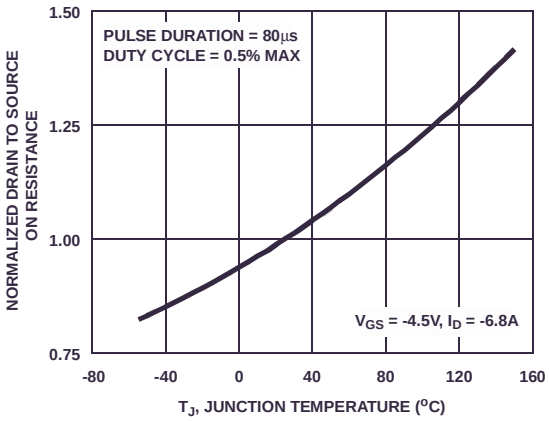



**Figure 8. Normalized Drain to Source On Resistance vs Junction Temperature**

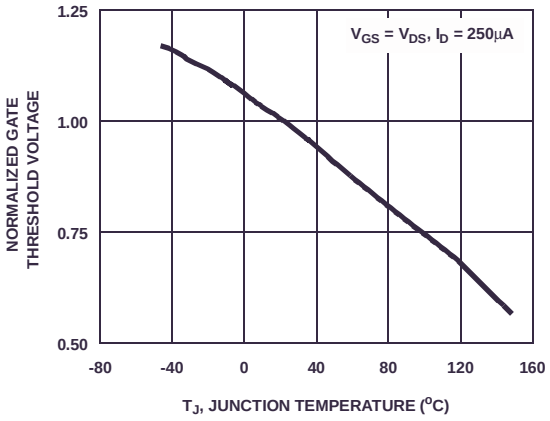



**Figure 9. Normalized Gate Threshold Voltage vs Junction Temperature**

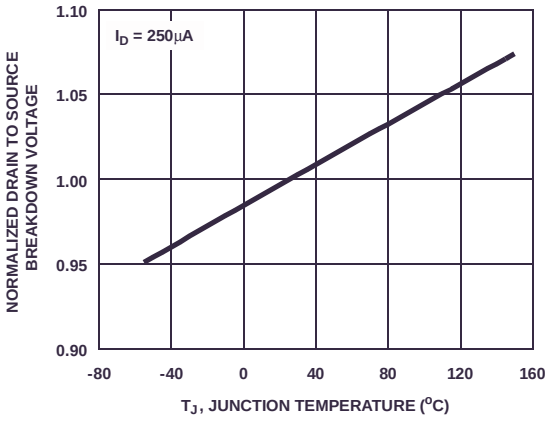



**Figure 10. Normalized Drain to Source Breakdown Voltage vs Junction Temperature**

## Typical Characteristic (Continued) $T_A$ = 25°C unless otherwise noted

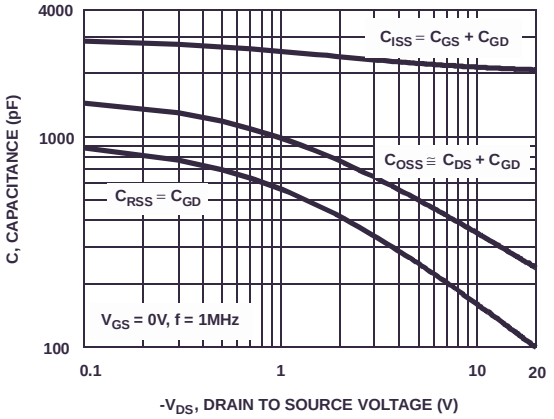



**Figure 11. Capacitance vs Drain to Source Voltage**

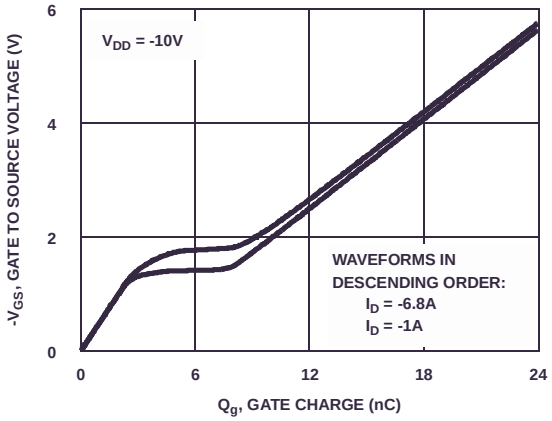



**Figure 12. Gate Charge Waveforms for Constant Gate Currents**

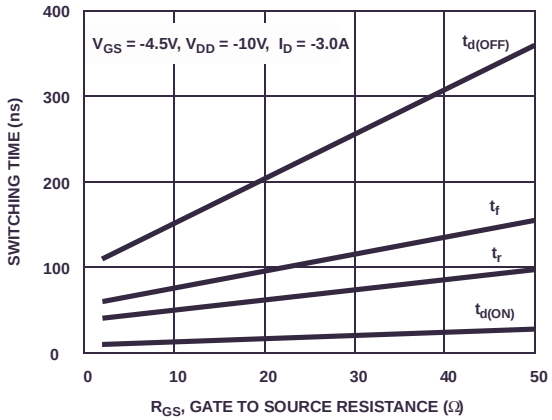



**Figure 13. Switching Time vs Gate Resistance**

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