

# FDN342P

## P-Channel 2.5V Specified PowerTrench™ MOSFET

### General Description

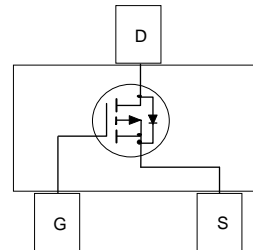
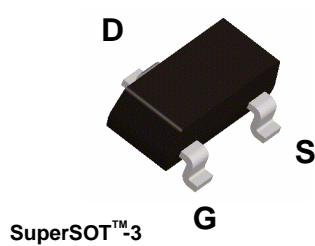
This P-Channel 2.5V specified MOSFET is produced in a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications for a wide range of gate drive voltages (2.5V - 12V).

### Applications

- Load switch
- Battery protection
- Power management

### Features

- -2 A, -20 V.  $R_{DS(ON)} = 0.08 \Omega @ V_{GS} = -4.5 V$   
 $R_{DS(ON)} = 0.13 \Omega @ V_{GS} = -2.5 V.$
- Rugged gate rating ( $\pm 12V$ ).
- High performance trench technology for extremely low  $R_{DS(ON)}$ .
- Enhanced power SuperSOT™-3 (SOT-23).



### Absolute Maximum Ratings T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage	-20	V
V <sub>GSS</sub>	Gate-Source Voltage	±12	V
I <sub>D</sub>	Drain Current - Continuous (Note 1a) - Pulsed	-2	A
		-10	
P <sub>D</sub>	Power Dissipation for Single Operation (Note 1a) (Note 1b)	0.5	W
		0.46	
T <sub>J</sub> , T <sub>stg</sub>	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case (Note 1)	75	°C/W

### Package Outlines and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
FDN342P	FDN342P	7"	8mm	3000 units

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-16		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 12\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -12\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

**On Characteristics** (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.6	-1.05	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -4.5\text{ V}, I_D = -2\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -2\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = -2.5\text{ V}, I_D = -1.5\text{ A}$		0.062 0.086 0.099	0.08 0.14 0.13	$\Omega$
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	-5			A
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -5\text{ A}$		7		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}$ $f = 1.0\text{ MHz}$		635		pF
$C_{oss}$	Output Capacitance			175		pF
$C_{riss}$	Reverse Transfer Capacitance			75		pF

**Switching Characteristics** (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -10\text{ V}, I_D = -1\text{ A}$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$		20	35	ns
$t_r$	Turn-On Rise Time			8	16	ns
$t_{d(off)}$	Turn-Off Delay Time			9	18	ns
$t_f$	Turn-Off Fall Time			19	32	ns
$Q_g$	Total Gate Charge	$V_{DS} = -10\text{ V}, I_D = -2\text{ A}$ $V_{GS} = -4.5\text{ V}$		6.3	9	nC
$Q_{gs}$	Gate-Source Charge			1.5		nC
$Q_{gd}$	Gate-Drain Charge			1.7		nC

**Drain-Source Diode Characteristics and Maximum Ratings**

$I_S$	Maximum Continuous Drain-Source Diode Forward Current				-0.42	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -0.42\text{ A}$ (Note 2)		-0.7	-1.2	V

**Notes:**

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $250^\circ\text{C/W}$  when mounted on a  $0.02\text{ in}^2$  pad of 2 oz. Cu.



b)  $270^\circ\text{C/W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$

## Typical Characteristics

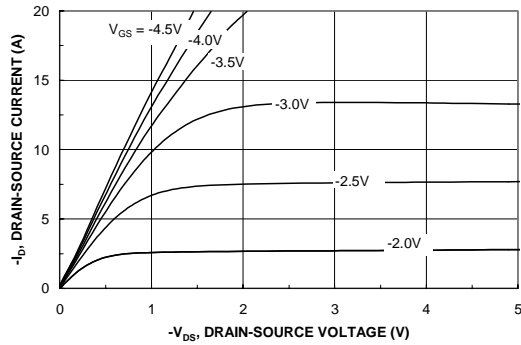


Figure 1. On-Region Characteristics.

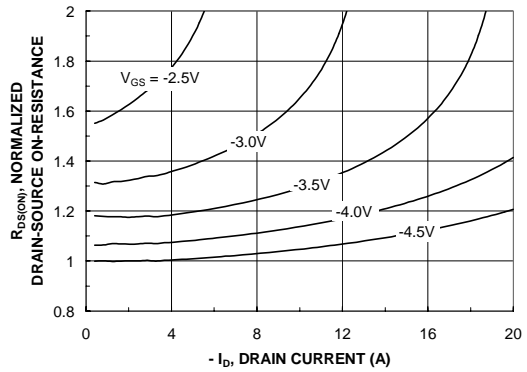


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

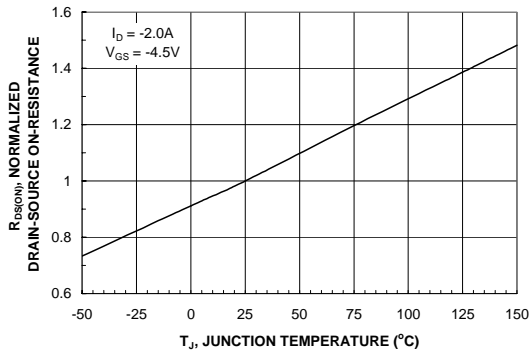


Figure 3. On-Resistance Variation with Temperature.

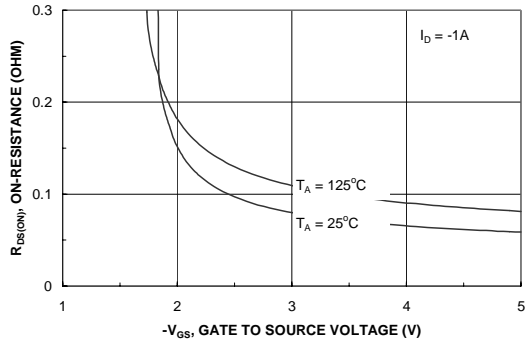


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

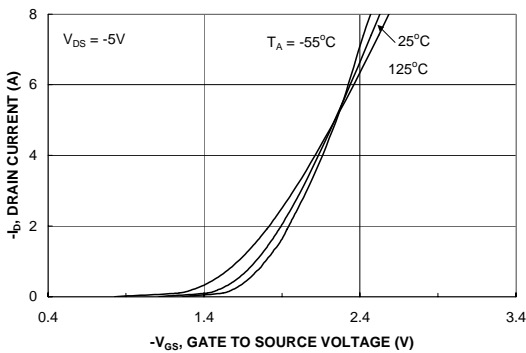


Figure 5. Transfer Characteristics.

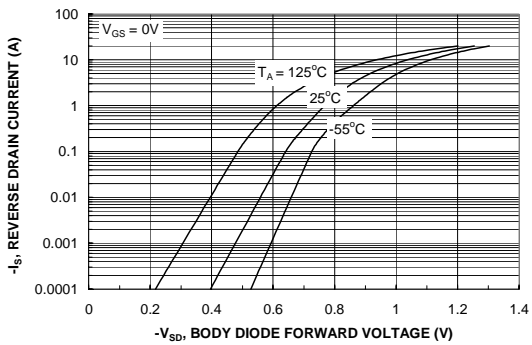
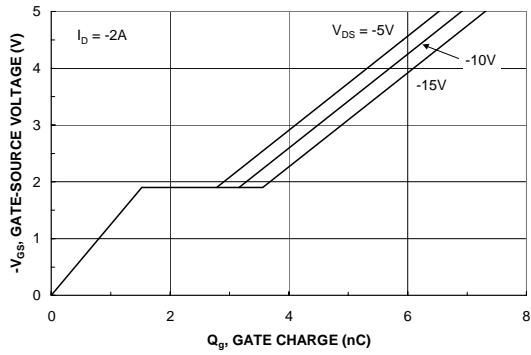
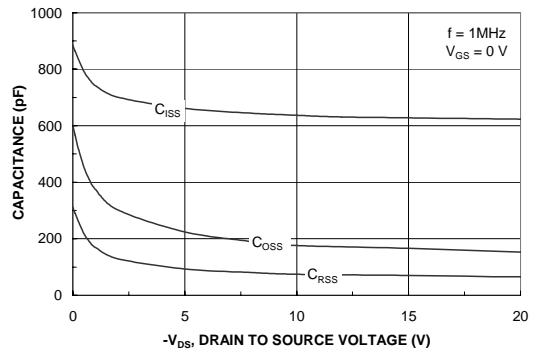


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

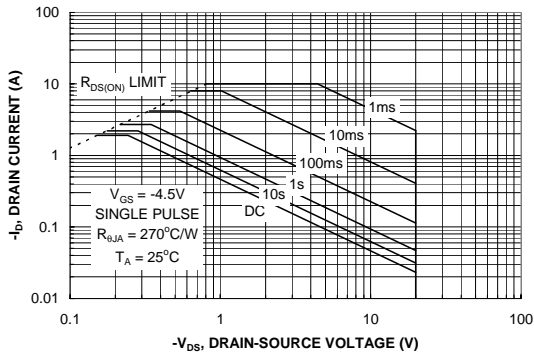
**Typical Characteristics** (continued)



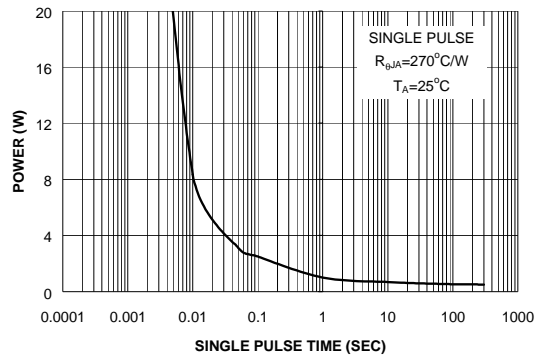
**Figure 7. Gate Charge Characteristics.**



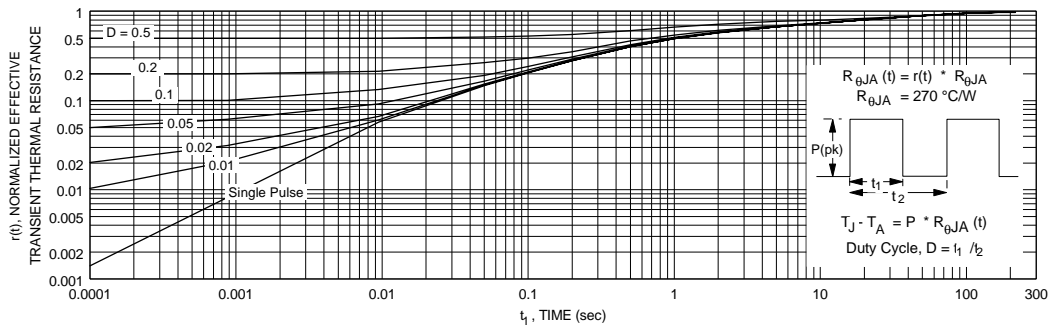
**Figure 8. Capacitance Characteristics.**



**Figure 9. Maximum Safe Operating Area.**



**Figure 10. Single Pulse Maximum Power Dissipation.**



**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

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