

FDD6692/FDU6692

30V N-Channel PowerTrench® MOSFET

General Description

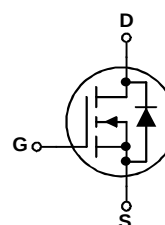
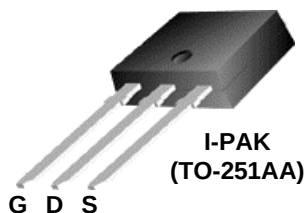
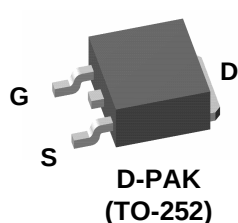
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

Applications

- DC/DC converter
- Motor drives

Features

- 54 A, 30 V. $R_{DS(ON)} = 12 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$
 $R_{DS(ON)} = 14.5 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$
- Low gate charge (18 nC typical)
- Fast switching
- High performance trench technology for extremely low $R_{DS(ON)}$



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	±16	V
I_D	Drain Current – Continuous (Note 3)	54	A
	– Pulsed (Note 1a)	162	
P_D	Power Dissipation for Single Operation (Note 1)	57	W
	(Note 1a)	3.8	
	(Note 1b)	1.6	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	2.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	40	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	96	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape width	Quantity
FDD6692	FDD6692	D-PAK (TO-252)	13"	12mm	2500 units
FDU6692	FDU6692	I-PAK (TO-251)	Tube	N/A	75

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Ratings (Note 2)						
W_{DSS}	Drain-Source Avalanche Energy	Single Pulse, $V_{DD} = 15\text{ V}$, $I_D=14\text{ A}$			165	mJ
I_{AR}	Drain-Source Avalanche Current				14	A
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		26		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSSF}	Gate–Body Leakage, Forward	$V_{GS} = 16\text{ V}$, $V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	$V_{GS} = -16\text{ V}$, $V_{DS} = 0\text{ V}$			–100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1	1.6	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		–5		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10\text{ V}$, $I_D = 14\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 13\text{ A}$ $V_{GS} = 10\text{ V}$, $I_D = 14\text{ A}$, $T_J = 125^\circ\text{C}$		9.5 11.5 16.5	12 14.5 18	m Ω
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 10\text{ V}$, $V_{DS} = 5\text{ V}$	50			A
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}$, $I_D = 14\text{ A}$		54		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$		2164		pF
C_{oss}	Output Capacitance			357		pF
C_{rss}	Reverse Transfer Capacitance			138		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 1\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		9	18	ns
t_r	Turn–On Rise Time			5	10	ns
$t_{d(off)}$	Turn–Off Delay Time			35	56	ns
t_f	Turn–Off Fall Time			10	20	ns
Q_g	Total Gate Charge	$V_{DS} = 15\text{ V}$, $I_D = 14\text{ A}$, $V_{GS} = 5\text{ V}$		18	25	nC
Q_{gs}	Gate–Source Charge			5		nC
Q_{gd}	Gate–Drain Charge			5		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				3.2	A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 3.2\text{ A}$ (Note 2)		0.72	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $R_{\theta JA} = 40^{\circ}\text{C/W}$ when mounted on a
1 in² pad of 2 oz copper



b) $R_{\theta JA} = 96^{\circ}\text{C/W}$ when mounted
on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

3. Maximum current is calculated as:
$$\sqrt{\frac{P_D}{R_{DS(on)}}}$$

where P_D is maximum power dissipation at $T_C = 25^{\circ}\text{C}$ and $R_{DS(on)}$ is at $T_{J(max)}$ and $V_{GS} = 10\text{V}$. Package current limitation is 21A

Typical Characteristics

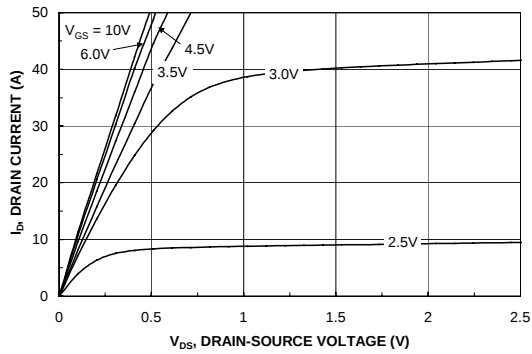


Figure 1. On-Region Characteristics.

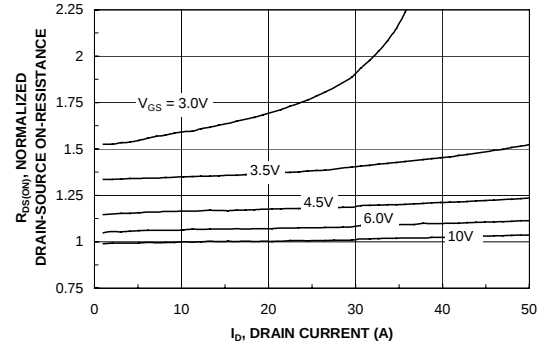


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

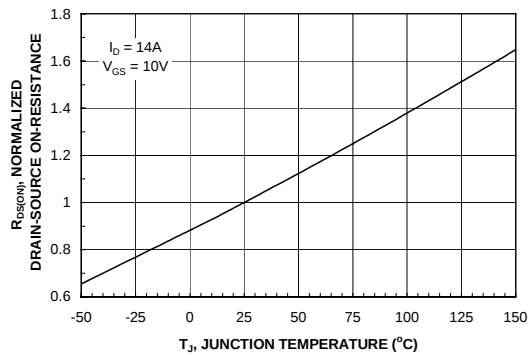


Figure 3. On-Resistance Variation with Temperature.

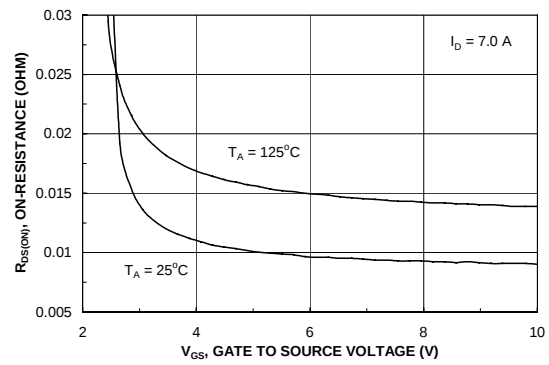


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

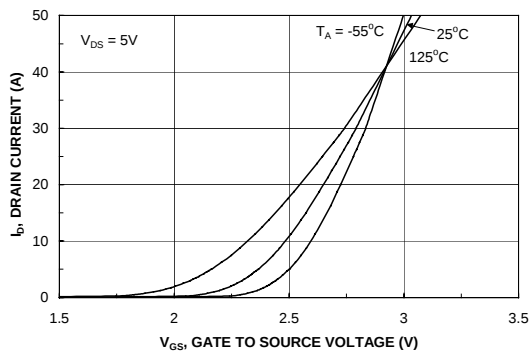


Figure 5. Transfer Characteristics.

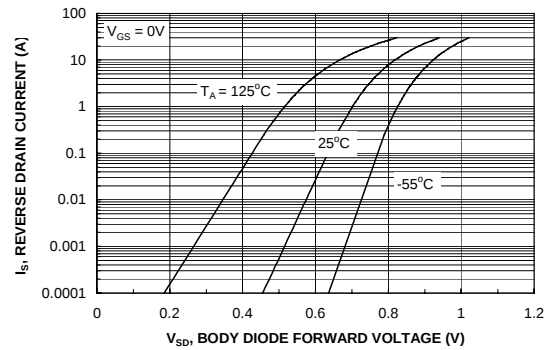


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

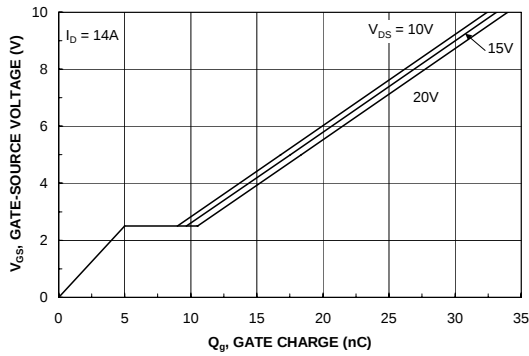


Figure 7. Gate Charge Characteristics.

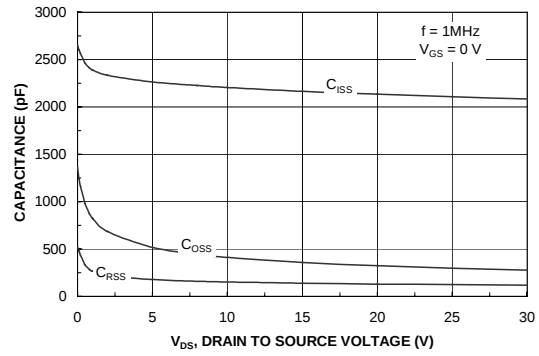


Figure 8. Capacitance Characteristics.

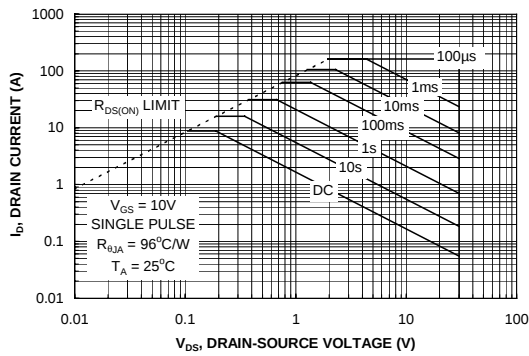


Figure 9. Maximum Safe Operating Area.

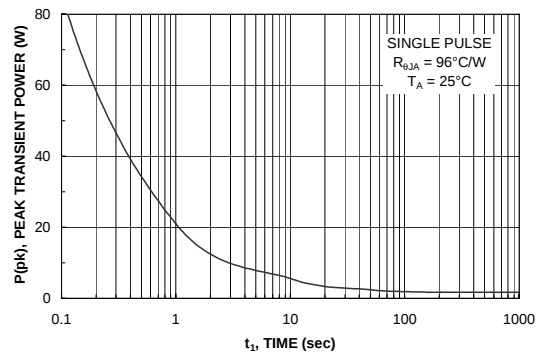


Figure 10. Single Pulse Maximum Power Dissipation.

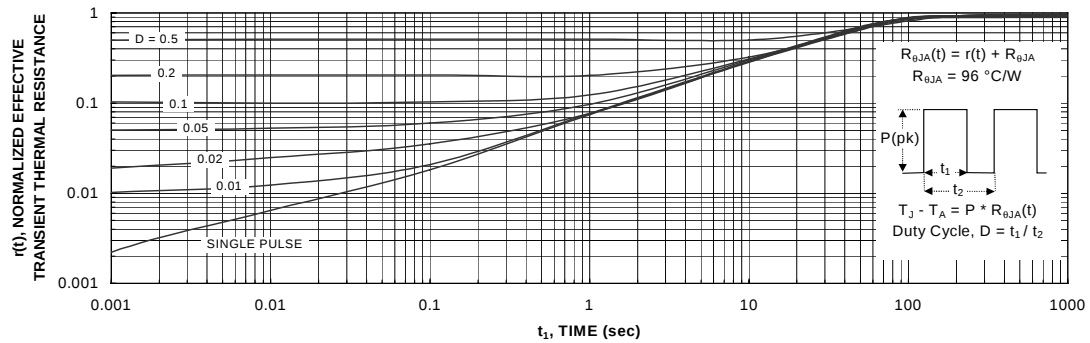


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

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