



August 2000

QFET™

FQB24N08 / FQI24N08

80V N-Channel MOSFET

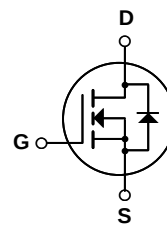
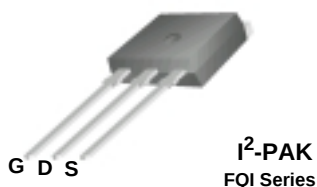
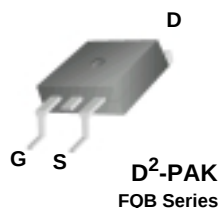
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as automotive, high efficiency switching for DC/DC converters, and DC motor control.

Features

- 24A, 80V, $R_{DS(on)} = 0.06\Omega$ @ $V_{GS} = 10V$
- Low gate charge (typical 19 nC)
- Low C_{rss} (typical 50 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- 175°C maximum junction temperature rating



Absolute Maximum Ratings

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQB24N08 / FQI24N08	Units
V_{DSS}	Drain-Source Voltage	80	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	24	A
	- Continuous ($T_C = 100^\circ\text{C}$)	17	A
I_{DM}	Drain Current - Pulsed (Note 1)	96	A
V_{GSS}	Gate-Source Voltage	± 25	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	230	mJ
I_{AR}	Avalanche Current (Note 1)	24	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	7.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	6.5	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) *	3.75	W
	Power Dissipation ($T_C = 25^\circ\text{C}$)	75	W
	- Derate above 25°C	0.5	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	2.0	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	40	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	$^\circ\text{C/W}$

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	80	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	--	0.08	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 64\text{ V}, T_C = 150^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 12\text{ A}$	--	0.048	0.06	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 30\text{ V}, I_D = 12\text{ A}$ (Note 4)	--	12	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	580	750	pF
C_{oss}	Output Capacitance		--	210	270	pF
C_{rss}	Reverse Transfer Capacitance		--	50	65	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 40\text{ V}, I_D = 24\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 4, 5)	--	10	30	ns
t_r	Turn-On Rise Time		--	105	220	ns
$t_{d(off)}$	Turn-Off Delay Time		--	30	70	ns
t_f	Turn-Off Fall Time		--	35	80	ns
Q_g	Total Gate Charge	$V_{DS} = 64\text{ V}, I_D = 24\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 4, 5)	--	19	25	nC
Q_{gs}	Gate-Source Charge		--	4.2	--	nC
Q_{gd}	Gate-Drain Charge		--	9.6	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	24	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	96	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 24 A	--	--	1.5	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 24 A,	--	63	--	ns
Q _{rr}	Reverse Recovery Charge	dI _F / dt = 100 A/μs (Note 4)	--	130	--	nC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 0.55\text{ mH}$, $I_{AS} = 24\text{ A}$, $V_{DD} = 25\text{ V}$, $R_G = 25\text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 24\text{ A}$, $di/dt \leq 300\text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

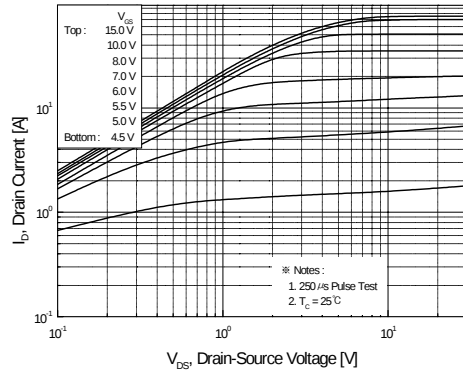


Figure 1. On-Region Characteristics

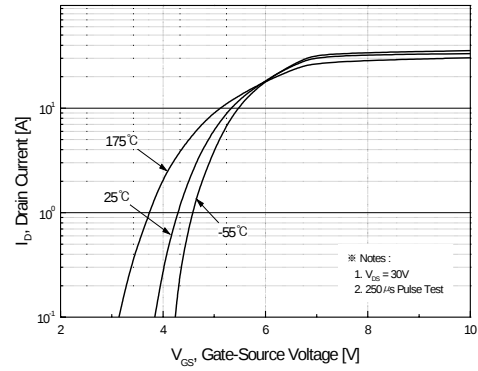


Figure 2. Transfer Characteristics

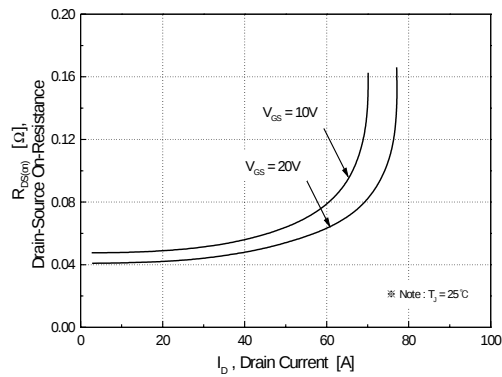


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

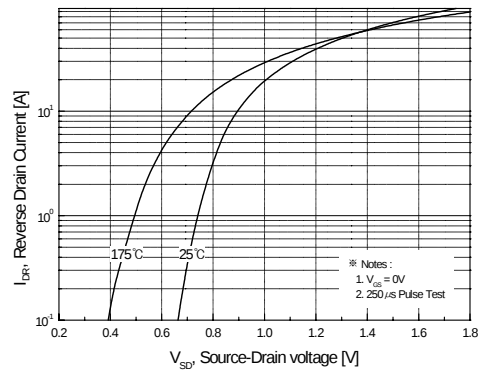


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

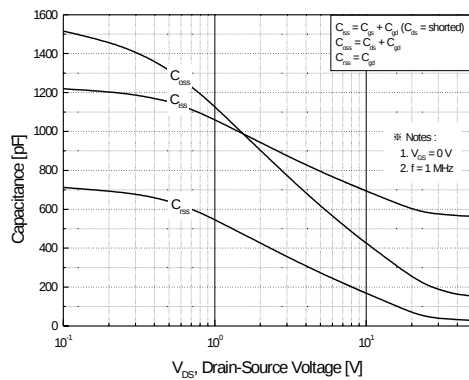


Figure 5. Capacitance Characteristics

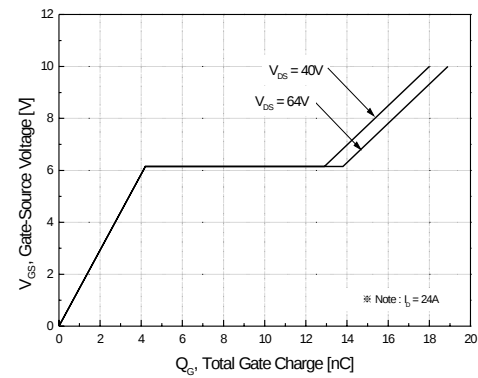


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

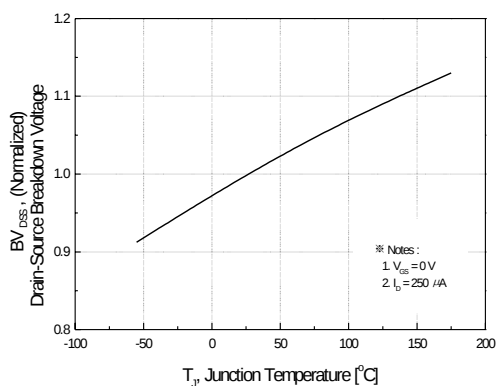


Figure 7. Breakdown Voltage Variation vs. Temperature

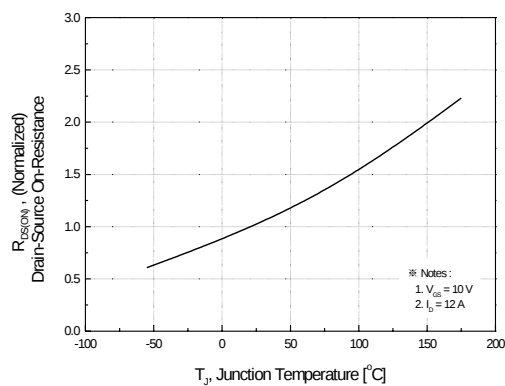


Figure 8. On-Resistance Variation vs. Temperature

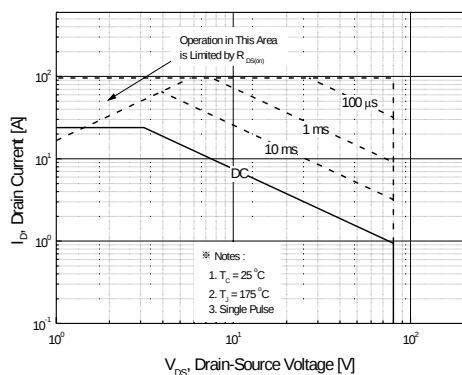


Figure 9. Maximum Safe Operating Area

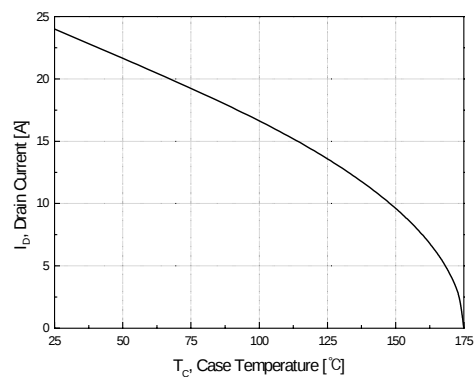


Figure 10. Maximum Drain Current vs. Case Temperature

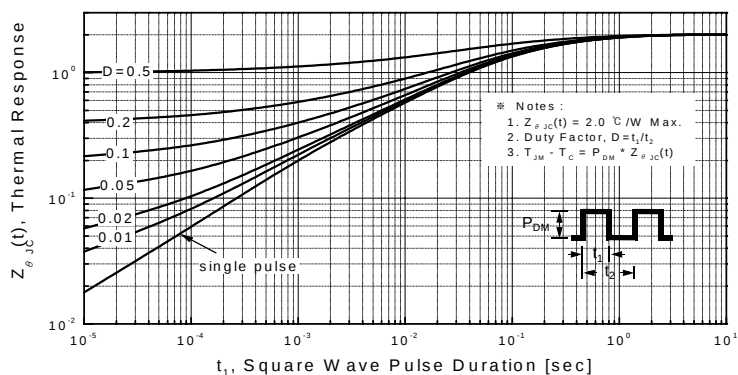
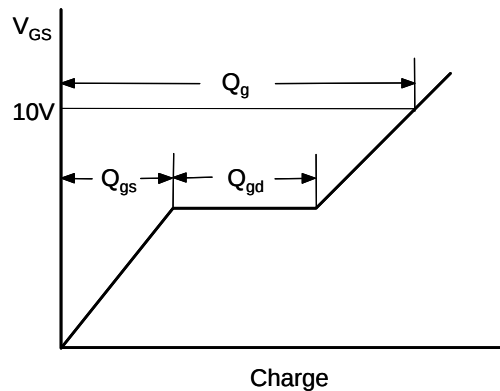
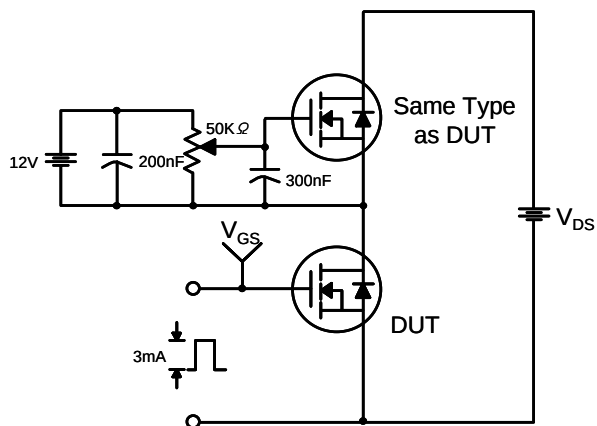
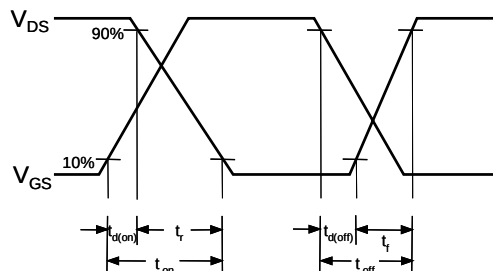
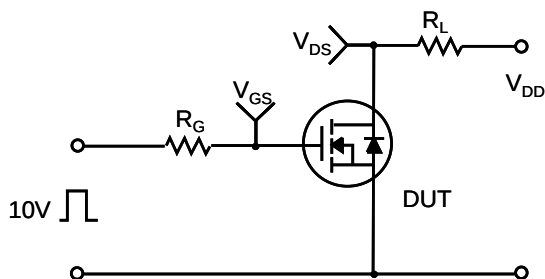


Figure 11. Transient Thermal Response Curve

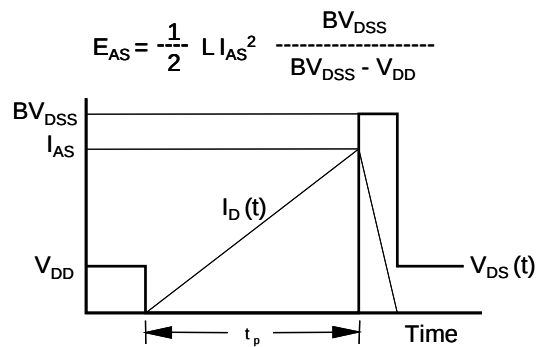
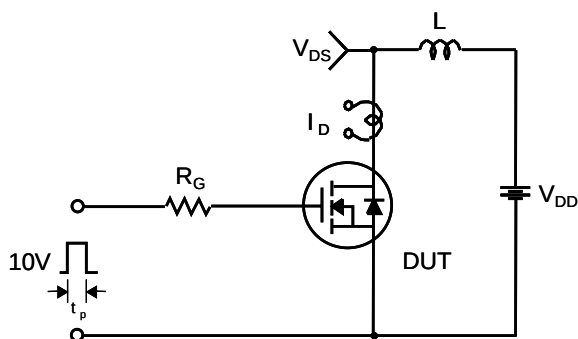
Gate Charge Test Circuit & Waveform



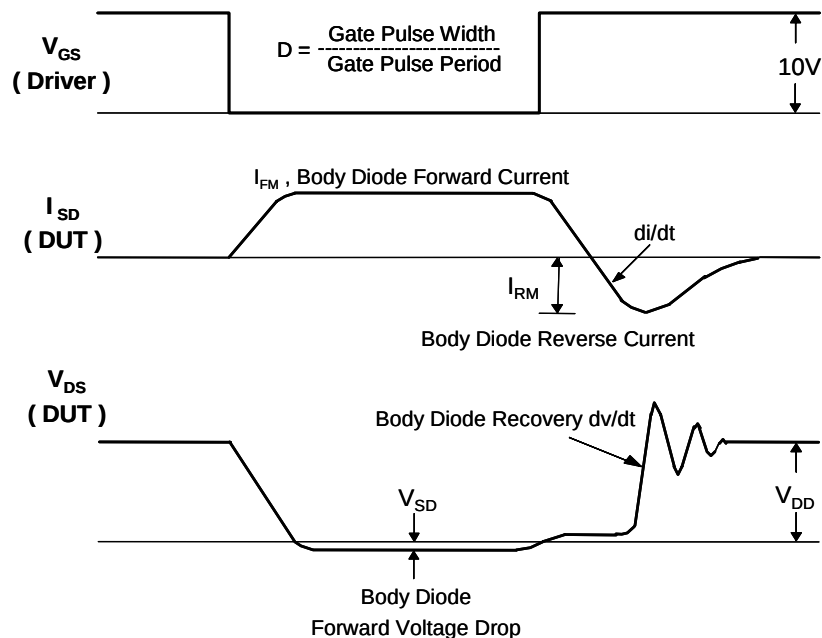
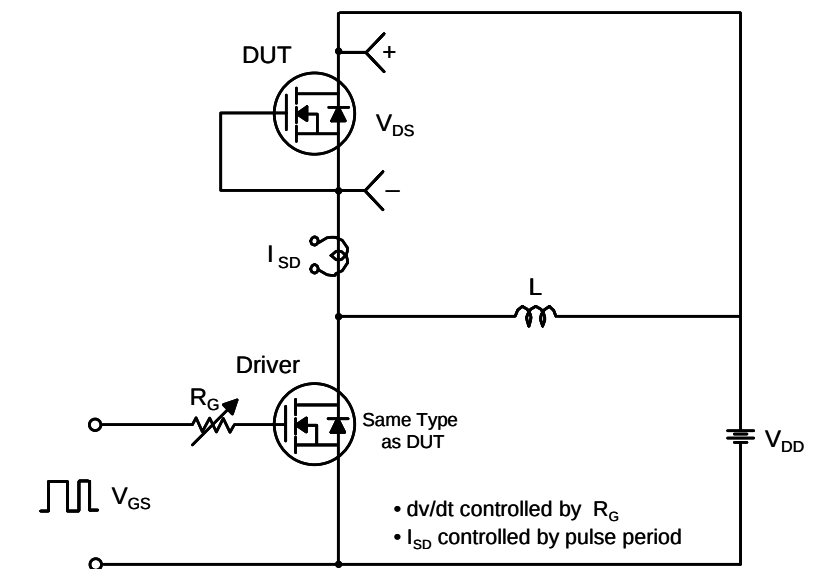
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

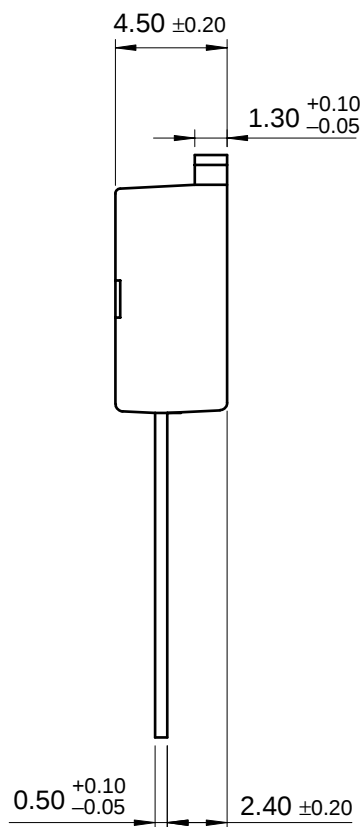
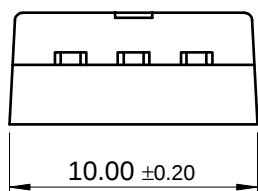


Peak Diode Recovery dv/dt Test Circuit & Waveforms



[illegible]

Technical drawing of a 3-pin connector. The drawing shows a top view and a side view. The top view dimensions are: overall width 9.90 ±0.20 mm (0.40 inches), overall height 13.08 ±0.20 mm (0.515 inches), and pin spacing 2.54 TYP mm. The side view dimensions are: overall height 13.08 ±0.20 mm (0.515 inches), pin height 1.27 ±0.10 mm (0.05 inches), pin diameter 0.80 ±0.10 mm (0.031 inches), and pin length 10.08 ±0.20 mm (0.397 inches). The connector has a central pin and two side pins. The top view also shows a central hole with a diameter of 1.20 ±0.20 mm (0.047 inches) and a distance of 1.20 ±0.20 mm (0.047 inches) from the center to the side pins. The side view shows a 45° chamfer on the pins.



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