

# FQPF2NA90

## 900V N-Channel MOSFET

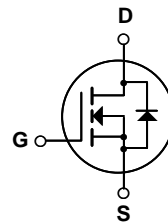
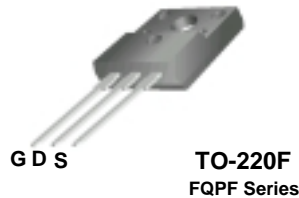
### General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply.

### Features

- 1.7A, 900V,  $R_{DS(on)} = 5.8 \Omega @ V_{GS} = 10 V$
- Low gate charge ( typical 15 nC)
- Low Crss ( typical 6.5 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



### Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted

| Symbol                            | Parameter   | FQPF2NA90   | Units |
|-----------------------------------|---|-------------|-------|
| V <sub>DSS</sub>                  | Drain-Source Voltage  | 900         | V     |
| I <sub>D</sub>                    | Drain Current - Continuous (T <sub>C</sub> = 25°C)<br>- Continuous (T <sub>C</sub> = 100°C) | 1.7         | A     |
|                                   |   | 1.07        | A     |
| I <sub>DM</sub>                   | Drain Current - Pulsed (Note 1)   | 6.8         | A     |
| V <sub>GSS</sub>                  | Gate-Source Voltage   | ± 30        | V     |
| E <sub>AS</sub>                   | Single Pulsed Avalanche Energy (Note 2)   | 310         | mJ    |
| I <sub>AR</sub>                   | Avalanche Current (Note 1)  | 1.7         | A     |
| E <sub>AR</sub>                   | Repetitive Avalanche Energy (Note 1)  | 3.9         | mJ    |
| dv/dt                             | Peak Diode Recovery dv/dt (Note 3)  | 4.0         | V/ns  |
| P <sub>D</sub>                    | Power Dissipation (T <sub>C</sub> = 25°C)<br>- Derate above 25°C                            | 39          | W     |
|                                   |   | 0.31        | W/°C  |
| T <sub>J</sub> , T <sub>STG</sub> | Operating and Storage Temperature Range   | -55 to +150 | °C    |
| T <sub>L</sub>                    | Maximum lead temperature for soldering purposes,<br>1/8" from case for 5 seconds            | 300         | °C    |

### Thermal Characteristics

| Symbol           | Parameter                               | Typ | Max  | Units |
|------------------|---|-----|------|-------|
| R <sub>θJC</sub> | Thermal Resistance, Junction-to-Case    | --  | 3.2  | °C/W  |
| R <sub>θJA</sub> | Thermal Resistance, Junction-to-Ambient | --  | 62.5 | °C/W  |

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted

| Symbol                         | Parameter                                 | Test Conditions   | Min | Typ | Max  | Units               |
|--------------------------------|---|---|-----|-----|------|---------------------|
| <b>Off Characteristics</b>     |   |   |     |     |      |                     |
| $BV_{DSS}$                     | Drain-Source Breakdown Voltage            | $V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$               | 900 | --  | --   | V                   |
| $\Delta BV_{DSS} / \Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$ | --  | 1.0 | --   | V/ $^\circ\text{C}$ |
| $I_{DSS}$                      | Zero Gate Voltage Drain Current           | $V_{DS} = 900\text{ V}, V_{GS} = 0\text{ V}$                | --  | --  | 10   | $\mu\text{A}$       |
|                                |   | $V_{DS} = 720\text{ V}, T_C = 125^\circ\text{C}$            | --  | --  | 100  | $\mu\text{A}$       |
| $I_{GSSF}$                     | Gate-Body Leakage Current, Forward        | $V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$                 | --  | --  | 100  | nA                  |
| $I_{GSSR}$                     | Gate-Body Leakage Current, Reverse        | $V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$                | --  | --  | -100 | nA                  |

### On Characteristics

|              |                                   |  |     |     |     |          |
|--------------|-----------------------------------|--|-----|-----|-----|----------|
| $V_{GS(th)}$ | Gate Threshold Voltage            | $V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$            | 3.0 | --  | 5.0 | V        |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS} = 10\text{ V}, I_D = 0.85\text{ A}$          | --  | 4.5 | 5.8 | $\Omega$ |
| $g_{FS}$     | Forward Transconductance          | $V_{DS} = 50\text{ V}, I_D = 0.85\text{ A}$ (Note 4) | --  | 2.3 | --  | S        |

### Dynamic Characteristics

|           |                              |  |    |     |     |    |
|-----------|------------------------------|--|----|-----|-----|----|
| $C_{iss}$ | Input Capacitance            | $V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$<br>$f = 1.0\text{ MHz}$ | -- | 525 | 680 | pF |
| $C_{oss}$ | Output Capacitance           |  | -- | 52  | 68  | pF |
| $C_{rss}$ | Reverse Transfer Capacitance |  | -- | 6.5 | 8.5 | pF |

### Switching Characteristics

|              |                     |  |             |    |     |    |    |
|--------------|---------------------|--|-------------|----|-----|----|----|
| $t_{d(on)}$  | Turn-On Delay Time  | $V_{DD} = 450\text{ V}, I_D = 2.8\text{ A},$<br>$R_G = 25\ \Omega$     | --          | 17 | 45  | ns |    |
| $t_r$        | Turn-On Rise Time   |  | --          | 40 | 90  | ns |    |
| $t_{d(off)}$ | Turn-Off Delay Time |  | (Note 4, 5) | -- | 30  | 70 | ns |
| $t_f$        | Turn-Off Fall Time  |  | (Note 4, 5) | -- | 30  | 70 | ns |
| $Q_g$        | Total Gate Charge   | $V_{DS} = 720\text{ V}, I_D = 2.8\text{ A},$<br>$V_{GS} = 10\text{ V}$ | --          | 15 | 20  | nC |    |
| $Q_{gs}$     | Gate-Source Charge  |  | (Note 4, 5) | -- | 3.7 | -- | nC |
| $Q_{gd}$     | Gate-Drain Charge   |  | (Note 4, 5) | -- | 7.5 | -- | nC |

### Drain-Source Diode Characteristics and Maximum Ratings

|          |   |   |    |     |     |               |
|----------|---|---|----|-----|-----|---------------|
| $I_S$    | Maximum Continuous Drain-Source Diode Forward Current | --  | -- | 1.7 | A   |               |
| $I_{SM}$ | Maximum Pulsed Drain-Source Diode Forward Current     | --  | -- | 6.8 | A   |               |
| $V_{SD}$ | Drain-Source Diode Forward Voltage                    | $V_{GS} = 0\text{ V}, I_S = 1.7\text{ A}$   | -- | --  | 1.4 | V             |
| $t_{rr}$ | Reverse Recovery Time                                 | $V_{GS} = 0\text{ V}, I_S = 2.8\text{ A},$<br>$di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4) | -- | 500 | --  | ns            |
| $Q_{rr}$ | Reverse Recovery Charge                               |   | -- | 2.6 | --  | $\mu\text{C}$ |

#### Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 203\text{ mH}, I_{AS} = 1.7\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 2.8\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width  $\leq 300\ \mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

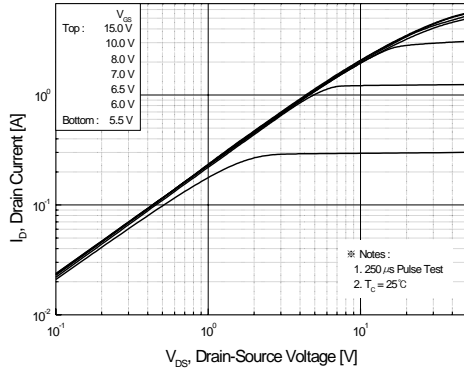


Figure 1. On-Region Characteristics

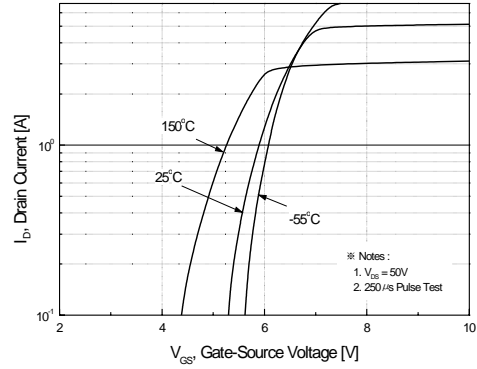


Figure 2. Transfer Characteristics

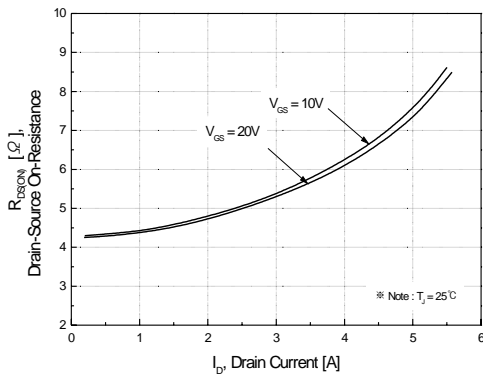


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

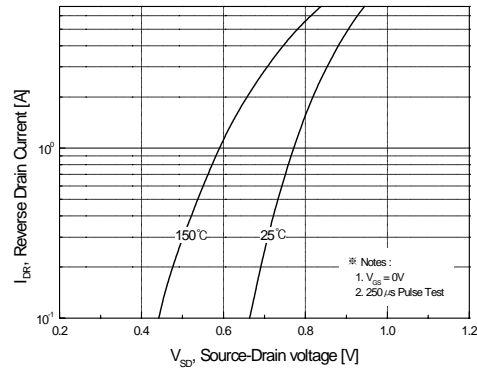


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

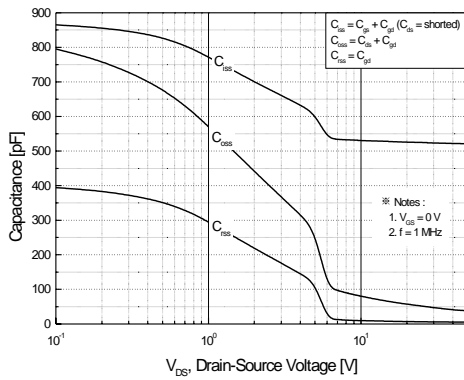


Figure 5. Capacitance Characteristics

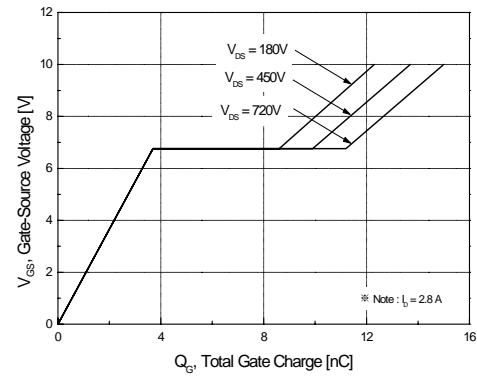
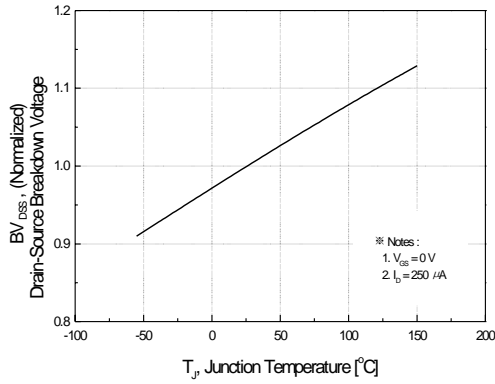
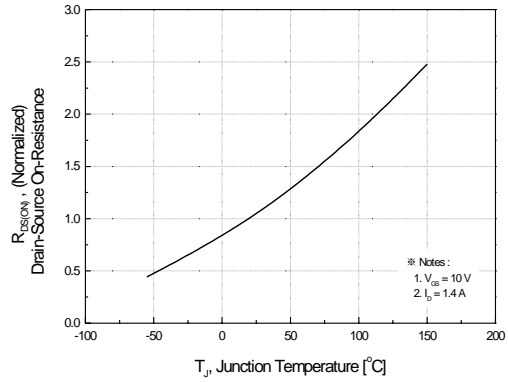


Figure 6. Gate Charge Characteristics

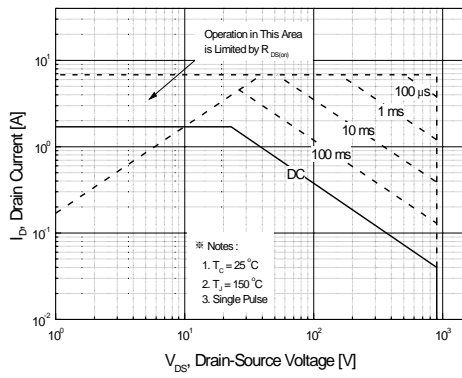
**Typical Characteristics** (Continued)



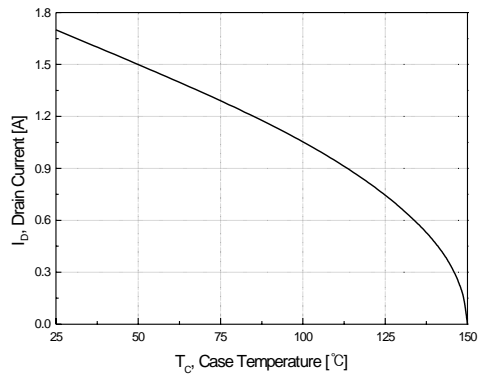
**Figure 7. Breakdown Voltage Variation vs. Temperature**



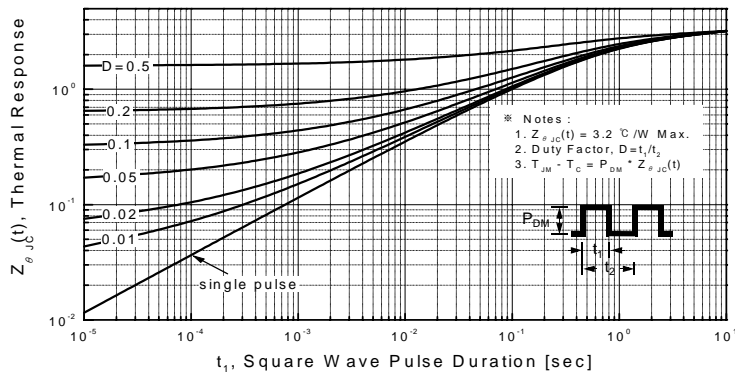
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**

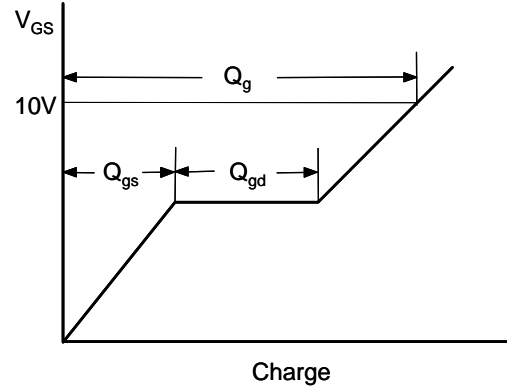
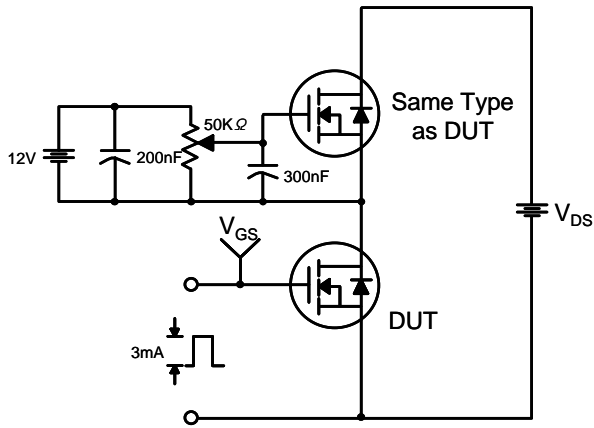


**Figure 10. Maximum Drain Current vs. Case Temperature**

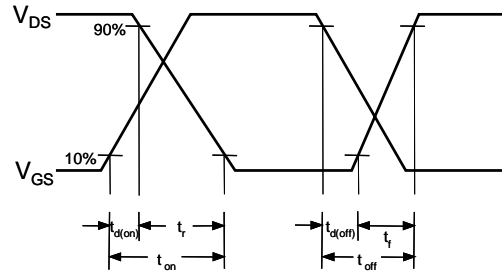
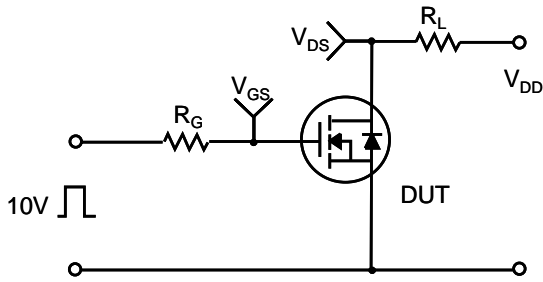


**Figure 11. Transient Thermal Response Curve**

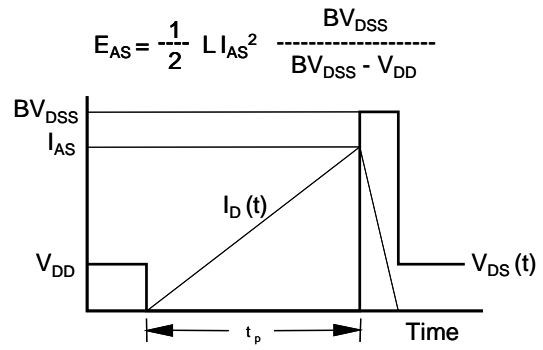
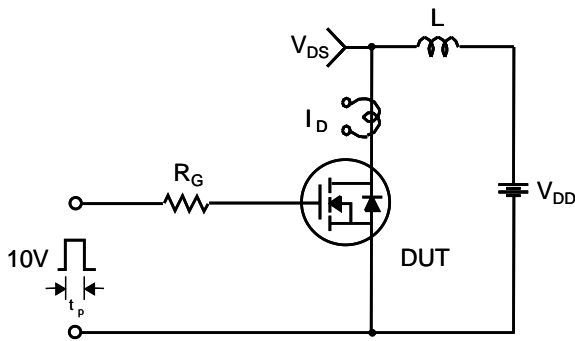
Gate Charge Test Circuit & Waveform



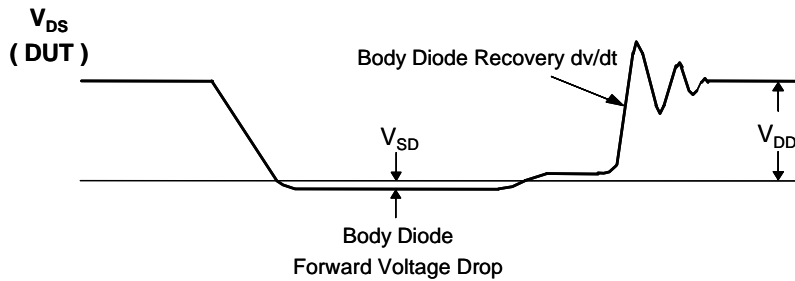
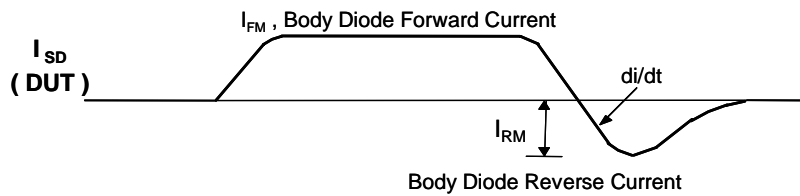
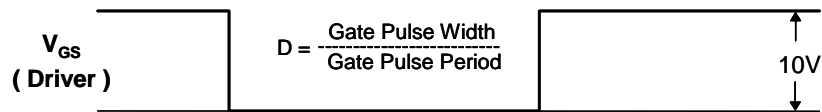
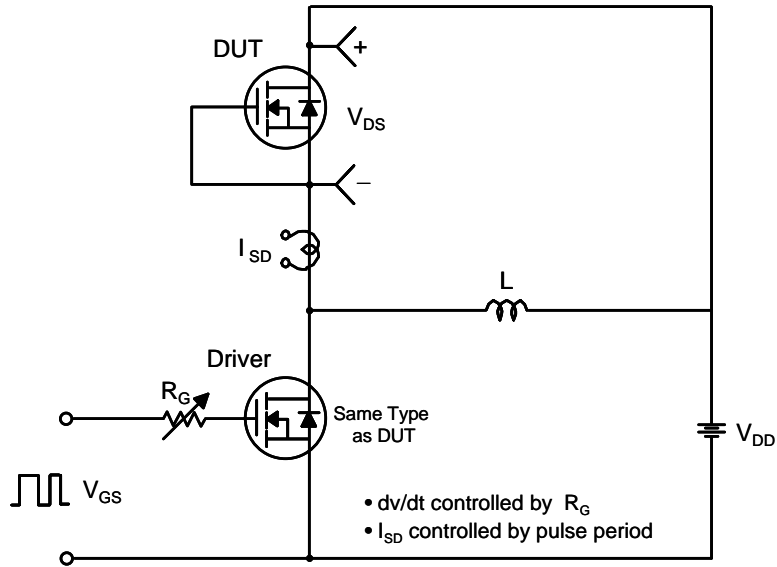
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

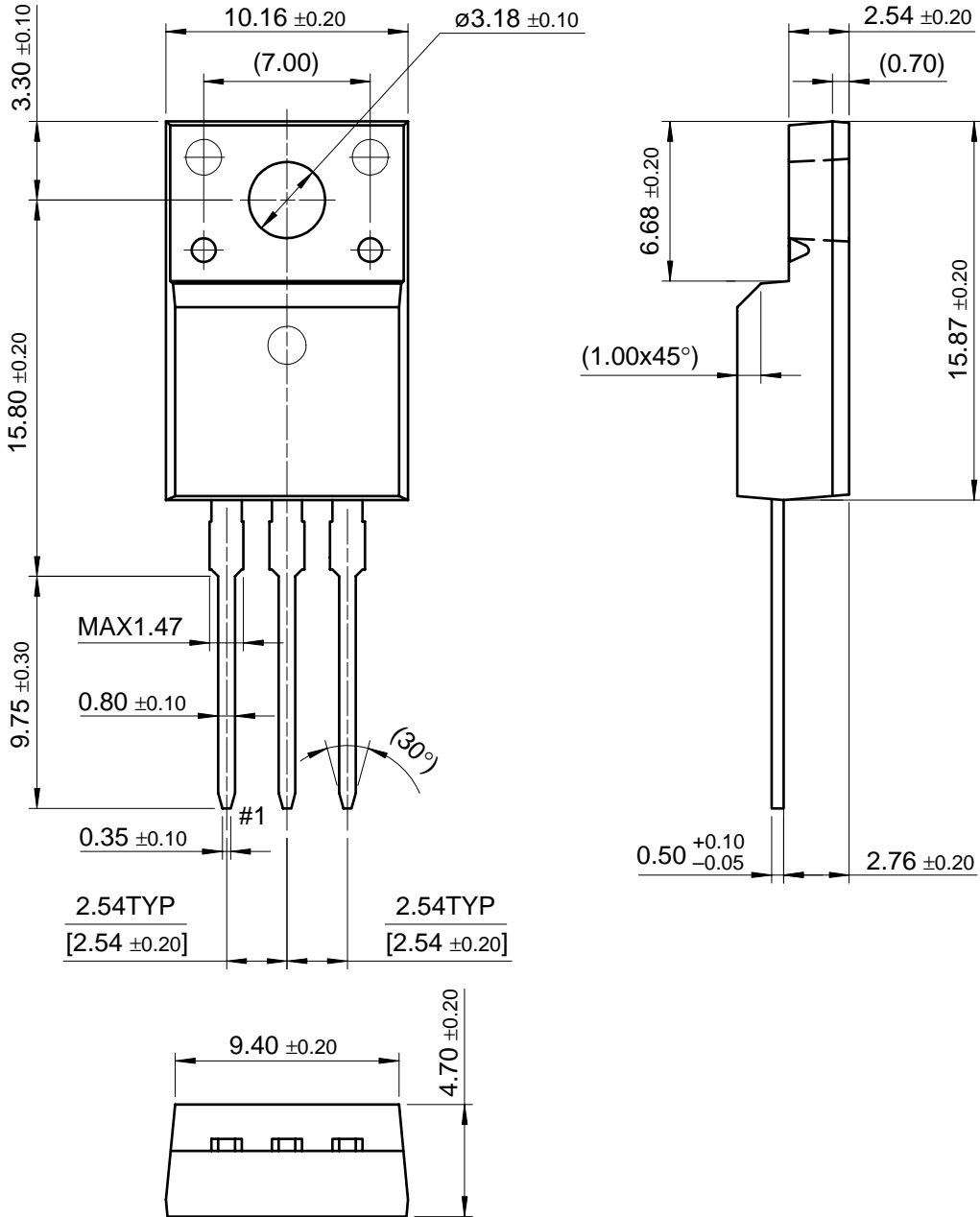


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimensions

TO-220F



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