

FQT13N06L

60V LOGIC N-Channel MOSFET

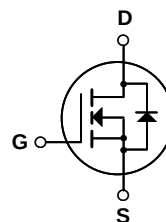
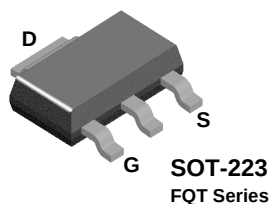
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as automotive, DC/DC converters, and high efficiency switching for power management in portable and battery operated products.

Features

- 2.8A, 60V, $R_{DS(on)} = 0.11\Omega$ @ $V_{GS} = 10V$
- Low gate charge (typical 4.8 nC)
- Low C_{rss} (typical 17 pF)
- Fast switching
- Improved dv/dt capability



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQT13N06L	Units
V_{DSS}	Drain-Source Voltage	60	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	2.8	A
	- Continuous ($T_C = 70^\circ\text{C}$)	2.24	A
I_{DM}	Drain Current - Pulsed (Note 1)	11.2	A
V_{GSS}	Gate-Source Voltage	± 20	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	85	mJ
I_{AR}	Avalanche Current (Note 1)	2.8	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	0.21	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	7.0	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	2.1	W
	- Derate above 25°C	0.017	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	60	$^\circ\text{C/W}$

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	--	0.05	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 48\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0	--	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 1.4\text{ A}$	--	0.088	0.11	Ω
		$V_{GS} = 5\text{ V}, I_D = 1.4\text{ A}$	--	0.110	0.14	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 25\text{ V}, I_D = 1.4\text{ A}$ (Note 4)	--	4.1	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	270	350	pF
C_{oss}	Output Capacitance		--	95	125	pF
C_{rss}	Reverse Transfer Capacitance		--	17	23	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{ V}, I_D = 6.8\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 4, 5)	--	8	25	ns
t_r	Turn-On Rise Time		--	90	190	ns
$t_{d(off)}$	Turn-Off Delay Time		--	20	50	ns
t_f	Turn-Off Fall Time		--	40	90	ns
Q_g	Total Gate Charge	$V_{DS} = 48\text{ V}, I_D = 13.6\text{ A},$ $V_{GS} = 5\text{ V}$ (Note 4, 5)	--	4.8	6.4	nC
Q_{gs}	Gate-Source Charge		--	1.6	--	nC
Q_{gd}	Gate-Drain Charge		--	2.7	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	2.8	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	11.2	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 2.8 A	--	--	1.5	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 13.6 A, dI _F / dt = 100 A/μs (Note 4)	--	45	--	ns
Q _{rr}	Reverse Recovery Charge		--	45	--	nC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 12.6\text{ mH}, I_{AS} = 2.8\text{ A}, V_{DD} = 25\text{ V}, R_G = 25\text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 13.6\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

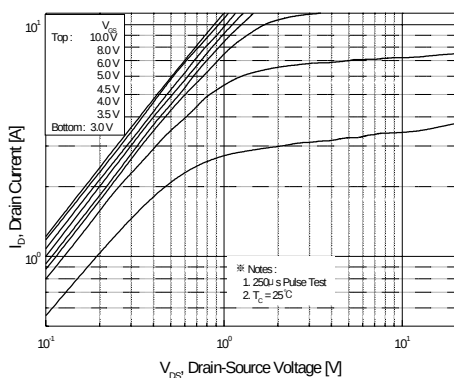


Figure 1. On-Region Characteristics

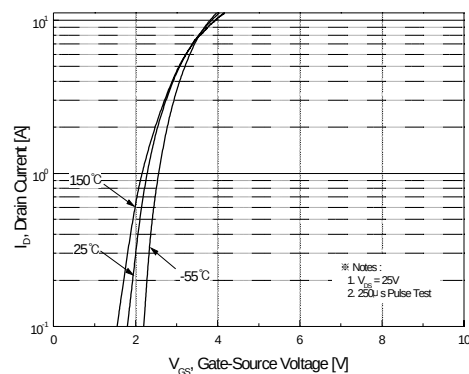


Figure 2. Transfer Characteristics

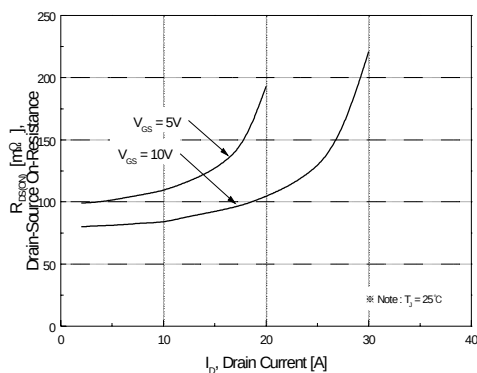


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

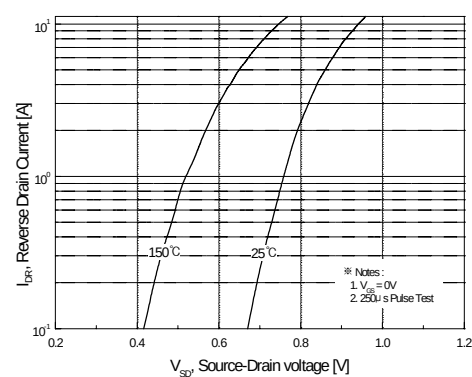


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

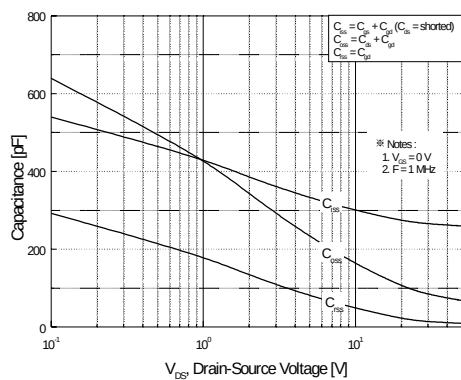


Figure 5. Capacitance Characteristics

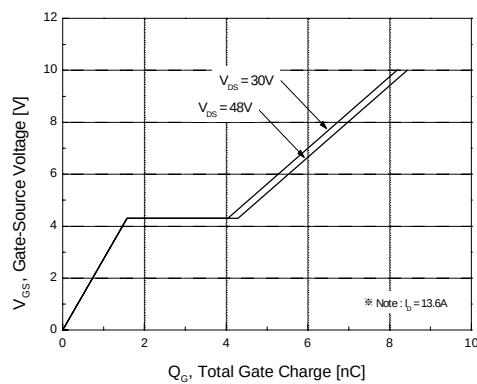


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

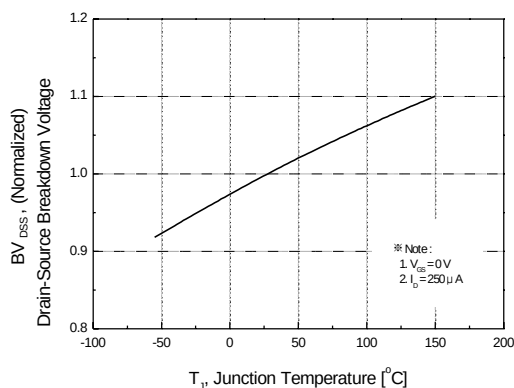


Figure 7. Breakdown Voltage Variation vs Temperature

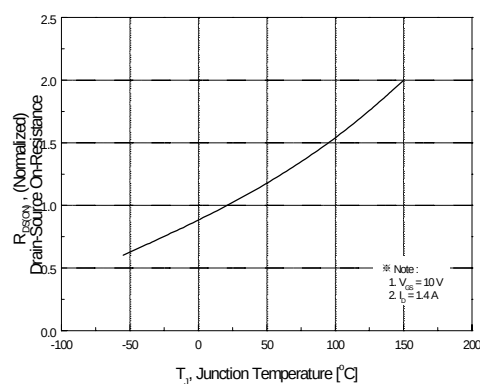


Figure 8. On-Resistance Variation vs Temperature

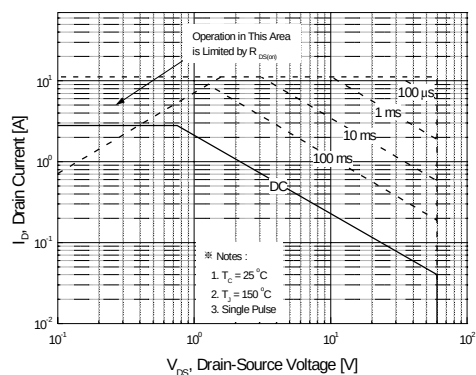


Figure 9. Maximum Safe Operating Area

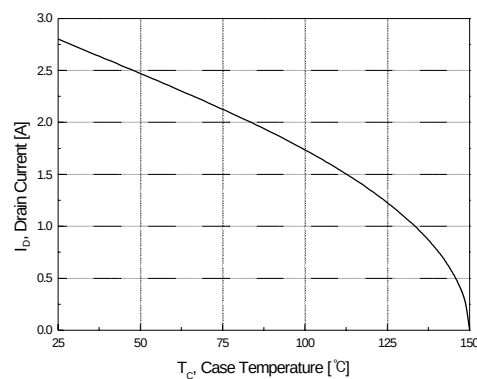


Figure 10. Maximum Drain Current vs Case Temperature

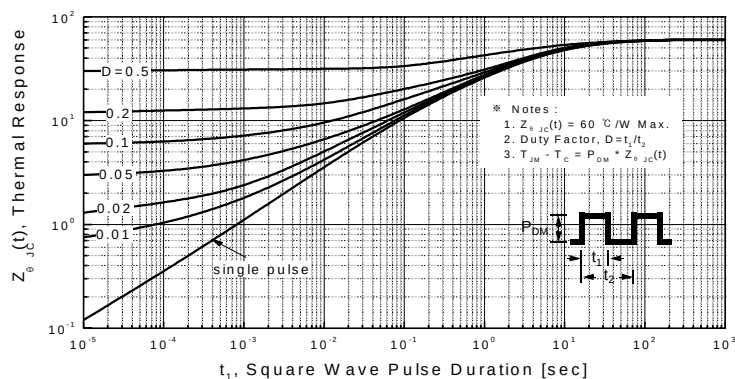
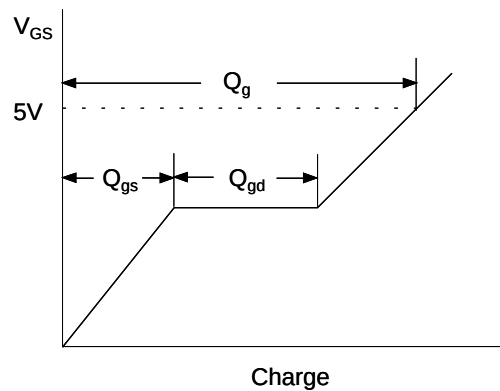
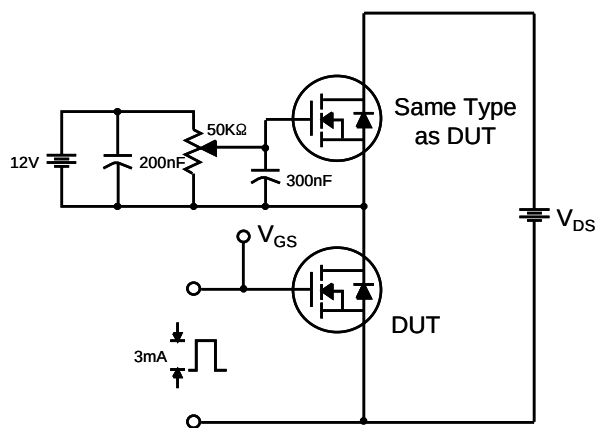
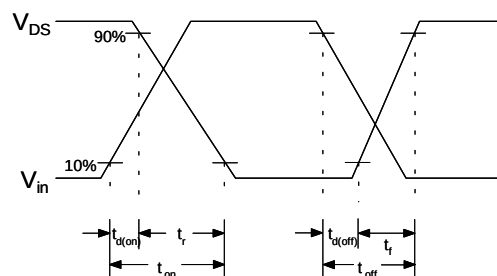
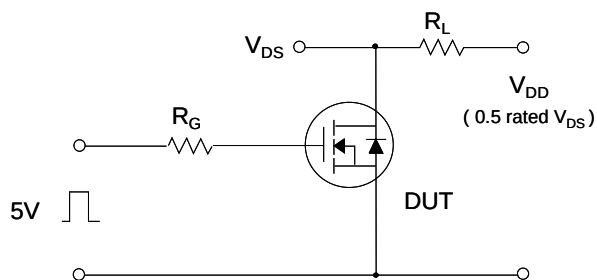


Figure 11. Transient Thermal Response Curve

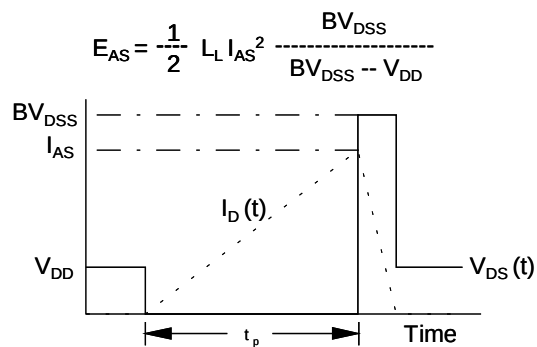
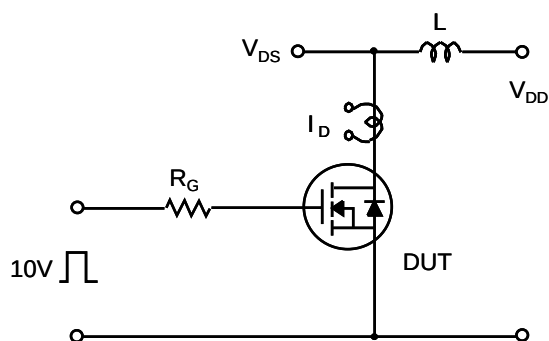
Gate Charge Test Circuit & Waveform

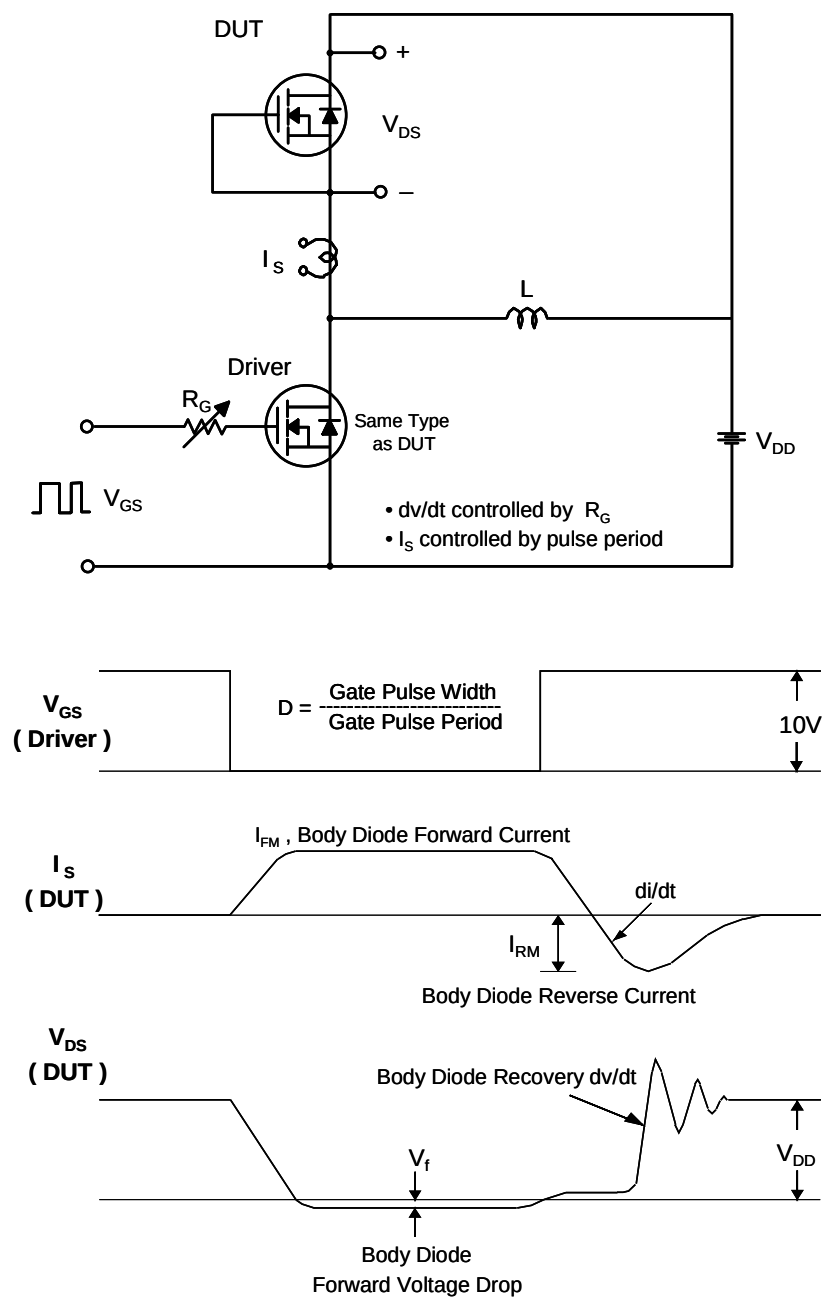


Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveform



Peak Diode Recovery dv/dt Test Circuit & Waveform

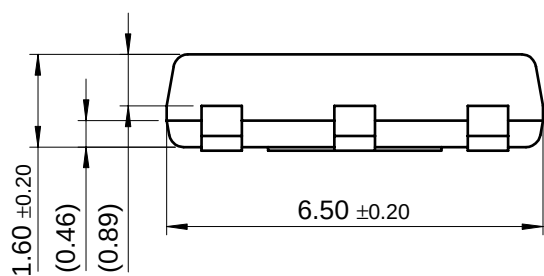
Technical drawing of a component, showing top and side views with dimensions.

Top View Dimensions:

- Overall width: 7.00 ± 0.30
- Base width: 4.60 ± 0.25
- Pin spacing: 2.30 TYP
- Central feature width: 3.00 ± 0.10
- Base offset: 0.70 ± 0.10
- Base thickness: $0.25^{+0.10}_{-0.05}$
- Base angle: $0^{\circ} \sim 10^{\circ}$

Side View Dimensions:

- Top flange thickness: 0.08 MAX
- Top flange width: 0.65 ± 0.20
- Central section height: 3.50 ± 0.20
- Central section width: $0.06^{+0.04}_{-0.02}$
- Central section offset: 0.60
- Central section width (inner): 0.60
- Central section width (outer): 0.60
- Central section offset (inner): 1.75 ± 0.20
- Central section offset (outer): 1.80 MAX



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