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FS8S0965RCB

Fairchild Power Switch(FPS)

Features

- Burst Mode Operation to Reduce the Power Consumption in the Standby Mode
- External pin for Synchronization and Soft Start
- Wide Operating Frequency Range up to 150kHz
- Low Start-up Current (Max:80uA)
- Low Operating Current (Max:15mA)
- Pulse by Pulse Current Limiting
- Over Voltage Protection (Auto Restart Mode)
- Over Load Protection (Auto Restart Mode)
- Abnormal Over Current Protection (Auto Restart Mode)
- Internal Thermal Shutdown (Auto Restart Mode)
- Under Voltage Lockout
- Internal High Voltage SenseFET

Application

- Monitor SMPS

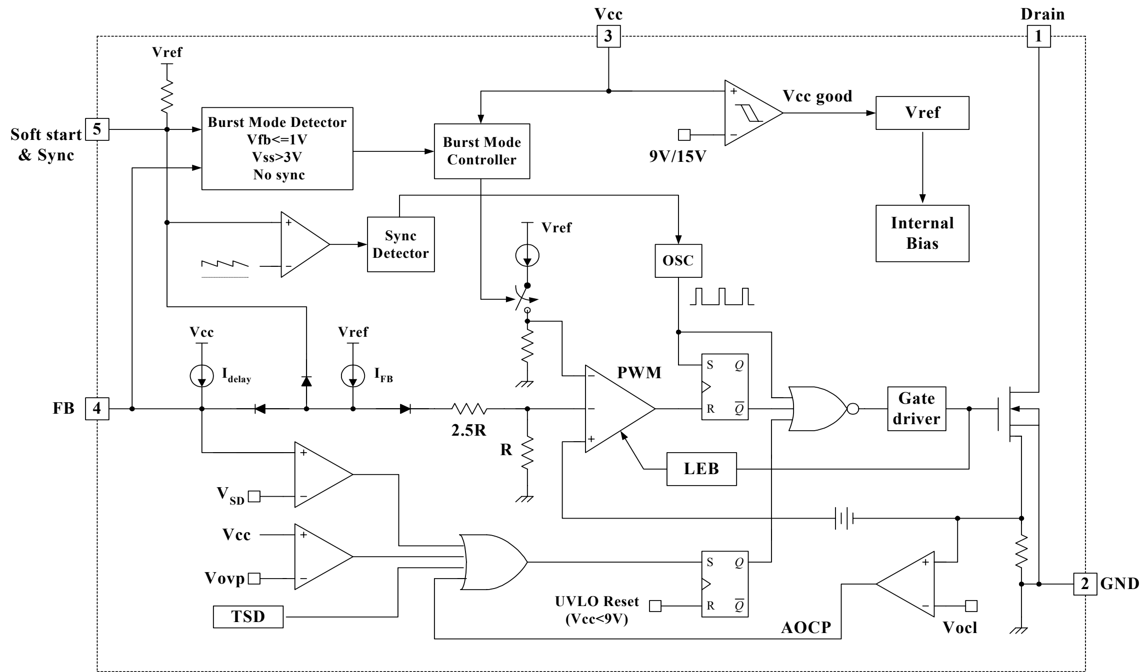
Description

FS8S0965RCB is a Fairchild Power Switch (FPS) that is specially designed for off-line SMPS of CRT monitor with minimal external components. This device is a current mode PWM controller combined with a high voltage power SenseFET in a single package. The PWM controller features integrated oscillator to be synchronized with the external sync signal, under voltage lockout, optimized gate driver and temperature compensated precise current sources for the loop compensation. This device also includes various fault protection circuits such as over voltage protection, over load protection, abnormal over current protection and over temperature protection. Compared with discrete MOSFET and PWM controller solution, FPS can reduce total cost, component count, size and weight simultaneously increasing efficiency, productivity and system reliability. This device is well suited for the cost effective monitor power supply.

TO-220-5L

1. Drain 2. GND 3. V_{CC} 4. Feedback 5. Sync

Internal Block Diagram



Rev.1.0.1

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	Drain	High voltage power SenseFET drain connection. This pin is designed to drive the transformer directly.
2	GND	This pin is the control ground and the SenseFET source.
3	Vcc	This pin is the positive supply input. This pin provides internal operating current for both start-up and steady-state operation.
4	Feedback	This pin is internally connected to the inverting input of the PWM comparator. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 7.5V, the over load protection is activated resulting in shutdown of FPS.
5	Soft Start & Sync	This pin is for soft start and synchronization to the external sync signal.

Absolute Maximum Ratings

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-Gate Voltage (R_{GS}=1MΩ)	V_{DGR}	650	V
Gate-Source (GND) Voltage	V_{GS}	±30	V
Drain Current Pulsed (1)	I_{DM}	32.4	A_{DC}
Single Pulsed Avalanche Energy (2)	E_{AS}	515	mJ
Single Pulsed Avalanche Current (3)	I_{AS}	25	A
Continuous Drain Current (Tc = 25°C)	I_D	8.1	A_{DC}
Continuous Drain Current (T_C=100°C)	I_D	5.1	A_{DC}
Supply Voltage	V_{CC}	40	V
Input Voltage Range	V_{FB}	-0.3 to Vcc	V
	V_{S_S}	-0.3 to 10	V
Total Power Dissipation	P_D(Watt H/S)	155	W
	Derating	1.243	W/°C
Operating Junction Temperature	T_j	+150	°C
Operating Ambient Temperature	T_A	-25 to +85	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C

Notes:
1. Repetitive rating: Pulse width limited by maximum junction temperature
2. L=14mH, starting Tj=25°C
3. L=13uH, starting Tj=25°C

Electrical Characteristics (SenseFET part)

(Ta=25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	650	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V	-	-	200	μA
		V_{DS}=520V V_{GS}=0V, T_C=125°C	-	-	300	μA
Static Drain Source On Resistance (1)	$R_{DS(ON)}$	V_{GS}=10V, I_D=1.8A	-	1.0	1.2	Ω
Forward Transconductance	gfs	V_{DS}=50V, I_D=1.8A	-	8	-	mho
Input Capacitance	Ciss	V_{GS}=0V, V_{DS}=25V, f = 1MHz	-	1300	-	pF
Output Capacitance	Coss		-	135	-	
Reverse Transfer Capacitance	Crss		-	25	-	
Turn On Delay Time	td(on)	V_{DD}=325V, I_D=6.5A (MOSFET switching time is essentially independent of operating temperature)	-	25	-	nS
Rise Time	tr		-	75	-	
Turn Off Delay Time	td(off)		-	130	-	
Fall Time	tf		-	70	-	
Total Gate Charge (Gate-Source+Gate-Drain)	Qg	V_{GS}=10V, I_D=6.5A, V_{DS}=520V (MOSFET switching time is essentially independent of operating temperature)	-	45	60	nC
Gate-Source Charge	Qgs		-	8	-	
Gate-Drain (Miller) Charge	Qgd		-	21	-	

Note:
(1) Pulse test : Pulse width ≤ 300μS, duty 2%

Electrical Characteristics (Continued)

(Ta=25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
UVLO SECTION						
Start Threshold Voltage	V_{START}	V_{FB}=GND	14	15	16	V
Stop Threshold Voltage	V_{STOP}	V_{FB}=GND	8	9	10	V
OSCILLATOR SECTION						
Initial Frequency	F_{OSC}	-	18	20	22	kHz
Voltage Stability	F_{STABLE}	12V ≤ Vcc ≤ 23V	0	1	3	%
Temperature Stability (1)	ΔF_{OSC}	-25°C ≤ Ta ≤ 85°C	0	±5	±10	%
Maximum Duty Cycle	D_{MAX}	-	92	95	98	%
Minimum Duty Cycle	D_{MIN}	-	-	-	0	%
FEEDBACK SECTION						
Feedback Source Current	I_{FBSO}	V_{FB}=GND	0.7	0.9	1.1	mA
Feedback Sink Current	I_{FBSI}	V_{FB}=4V,V_{CC}=19V	2.4	3.0	3.6	mA
Shutdown Feedback Voltage	V_{SD}	Vfb ≥ 6.9V	6.9	7.5	8.1	V
Shutdown Delay Current	Idelay	V_{FB}=5V	1.6	2.0	2.4	μA
PROTECTION SECTION						
Over Voltage Protection	V_{OVP}	Vcc ≥ 27V	34	37	-	V
Over Current Latch Voltage (2)	V_{OCL}	-	0.95	1.0	1.05	V
Thermal Shutdown Temp.(1)	T_{SD}	-	140	160	-	°C
SYNC & SOFTSTART SECTION						
Softstart Vortage	V_{SS}	Vfb=2	4.7	5.0	5.3	V
Softstart Current	I_{SS}	Vss=0V	0.8	1.0	1.2	mA
Sync High Threshold Voltage	V_{SH}	Vcc=16V,Vfb=5V	6.7	7.2	7.9	V
Sync Low Threshold Voltage	V_{SL}	Vcc=16V,Vfb=5V	5.4	5.8	6.2	V

Note:
1. These parameters, although guaranteed at the design, are not tested in mass production.
2. These parameters, although guaranteed, are tested in EDS(wafer test) process.

Electrical Characteristics(Continued)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
BURST MODESECTION(DPMS MODE)						
Burst Mode High Threshold Voltage	V_{BUH}	Vfb=0V	11.6	12	12.6	V
Burst Mode Low Threshold Voltage	V_{BUL}	Vfb=0V	10.6	11	11.6	V
Burst Mode Enable FB Voltage	V_{BUFB}	Vcc=10.5V	0.9	1.0	1.1	V
Burst Mode Enable S_S Voltage	V_{BUSS}	Vcc=10.5V,Vfb=0V	2.5	3.0	3.5	V
Burst Mode Enable Delay Time	T_{BUDT}	Vcc=10.5V,Vfb=0V	-	0.5	-	ms
Burst Mode Frequency	F_{BU}	Vcc=10.5V,Vfb=0V	32	40	48	kHz
CURRENT LIMIT(SELF-PROTECTION)SECTION						
Peak Current Limit(1)	I_{OVER}	-	5.28	6.0	6.72	A
Burst Mode Peak Current Limit	I_{BU_PK}	-	0.45	0.6	0.75	A
TOTAL DEVICE SECTION						
Start Up Current	I_{START}	V_{CC}=Vstart-0.1V	-	40	80	uA
Operating Supply Current (2)	I_{OP}	Vfb=GND, V_{CC}=16V	-	9	15	mA
	$I_{OP(MIN)}$	Vfb=GND, V_{CC}=12V				
	$I_{OP(MAX)}$	Vfb=GND, V_{CC}=27V				

Note:
1. These parameters indicate inductor current.
2. These parameters are the current flowing in the control IC.

Typical Performance Characteristics

(These characteristic graphs are normalized at Ta= 25°C)

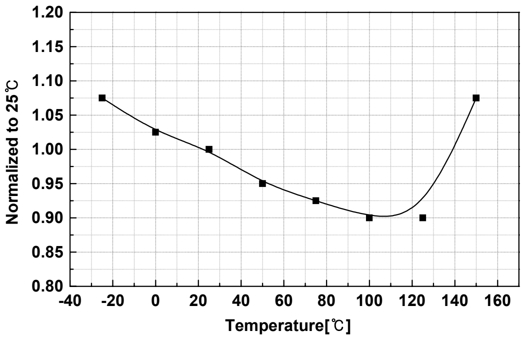


Figure 1. Start Up Current vs. Temp.

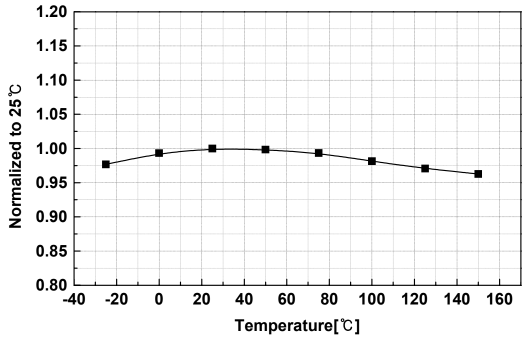


Figure 2. Operating Supply Current vs. Temp.

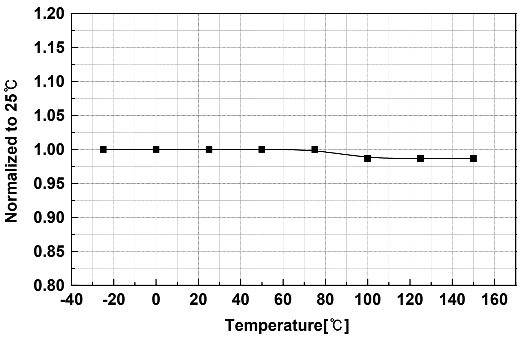


Figure 3. Start Threshold Voltage vs. Temp.

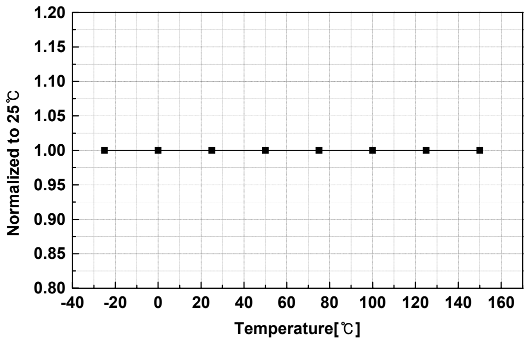


Figure 4. Stop Threshold Voltage vs. Temp.

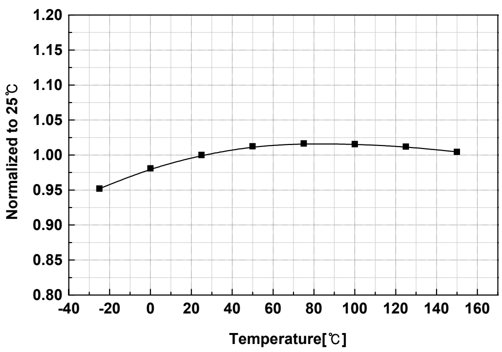


Figure 5. Initial Freqency vs. Temp.

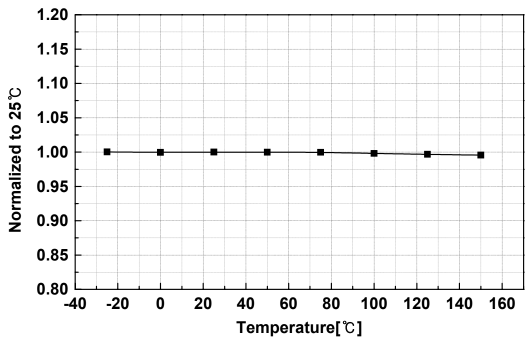


Figure 6. Maximum Duty Cycle vs. Temp.

Typical Performance Characteristics(Continued)

(These characteristic graphs are normalized at Ta= 25°C)

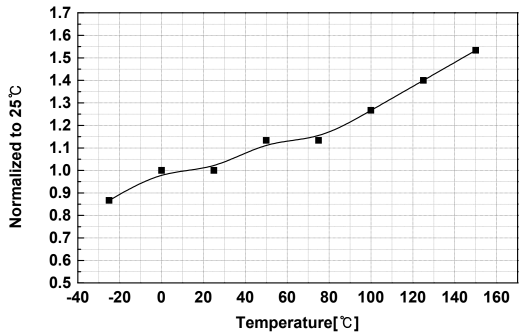


Figure 7. Feedback Offset Voltage vs. Temp.

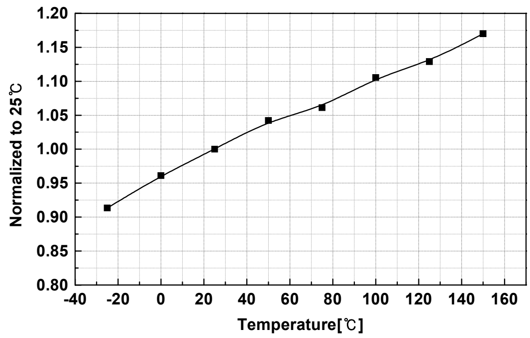


Figure 8. Feedback Sink Current vs. Temp.

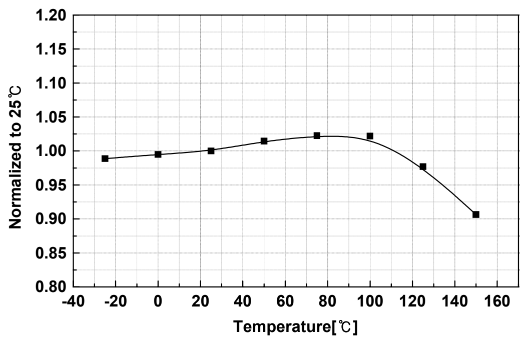


Figure 9. Shutdown Delay Current vs. Temp.

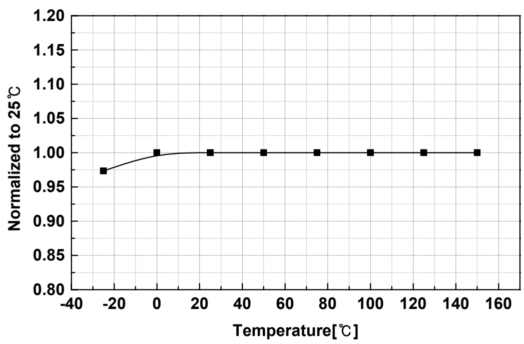


Figure 10. Shutdown Feedback Voltage vs. Temp.

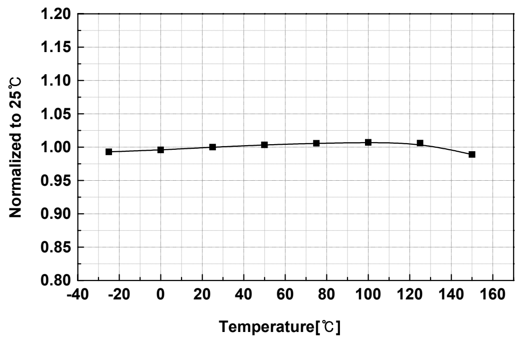


Figure 11. Soft Start Voltage vs. Temp.

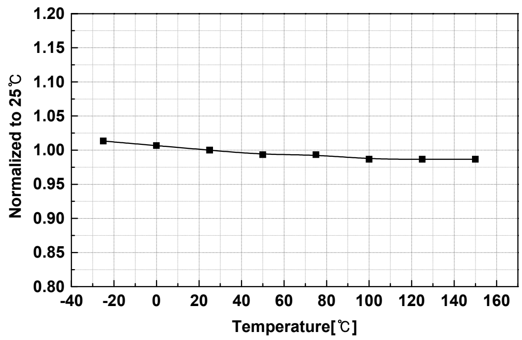


Figure 12. Over Voltage Protection vs. Temp.

Typical Performance Characteristics(Continued)

(These characteristic graphs are normalized at Ta= 25°C)

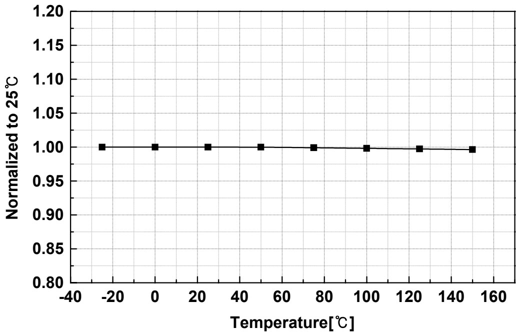


Figure 13. Normal Mode Regulation Voltage vs. Temp.

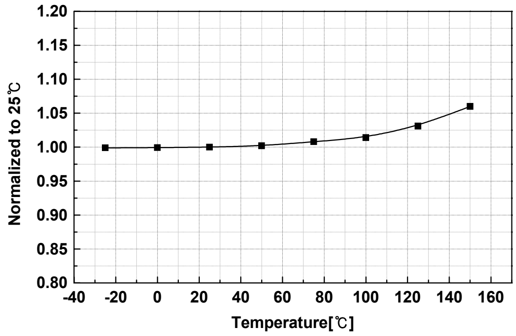


Figure 14. Peak Current vs. Temp.

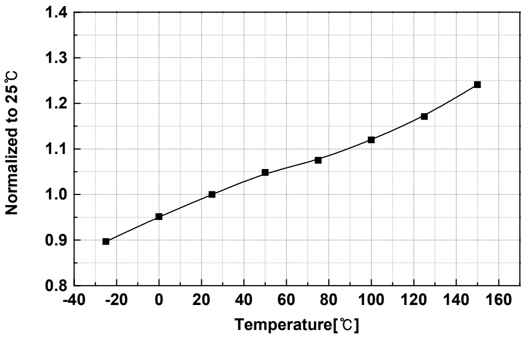


Figure 15. Feedback Sink Current vs. Temp.

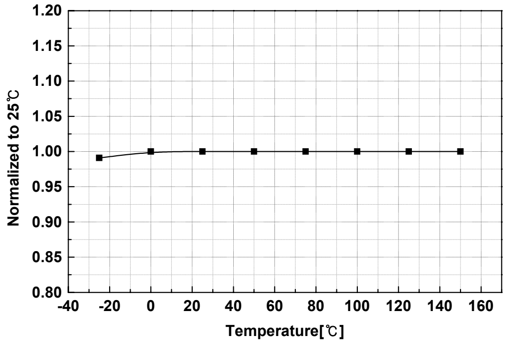


Figure 16. Burst Mode Low Threshold Voltage vs. Temp.

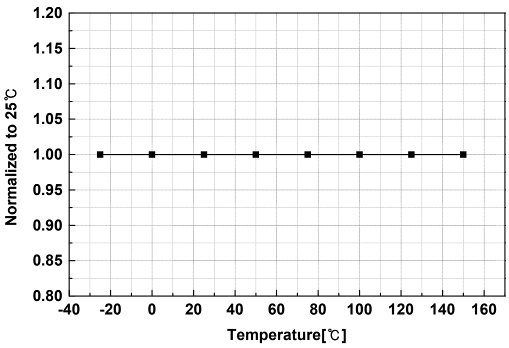


Figure 17. Burst Mode High Threshold Voltage vs. Temp.

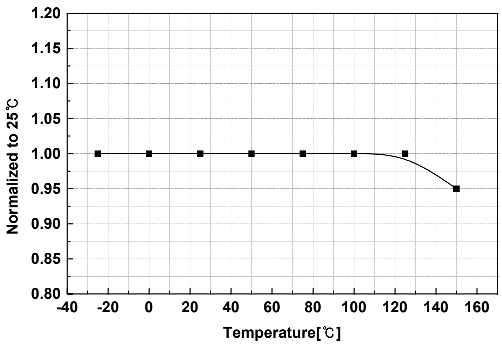


Figure 18. Burst Mode Enable Voltage vs. Temp.

Typical Performance Characteristics(Continued)

(These characteristic graphs are normalized at Ta= 25°C)

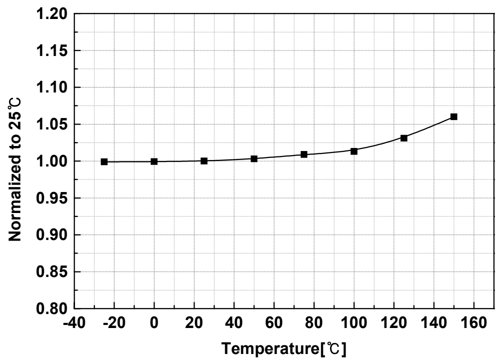


Figure 19. Burst Mode Peak Current vs. Temp.

Functional Description

1. **Start up** : To guarantee stable operation of the control IC, FS8S0965RCB has UVLO circuit with 6V hysteresis band. Figure 1 shows the relation between the supply current (Icc) and the supply voltage (Vcc). Before Vcc reaches 15V, the FPS consumes only startup current of 80μA, which is usually provided by the DC link through start-up resistor. When Vcc reaches 15V, the FPS begins operation and the operating current increases to 15mA as shown. Once the control IC starts operation, it continues its normal operation until Vcc goes below the stop voltage of 9V

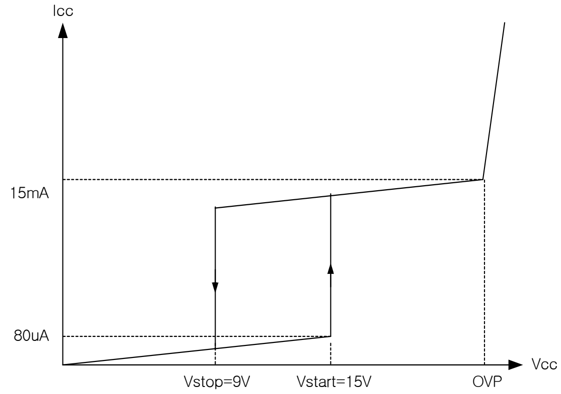


Figure 1. Strat up with hysteresis

2. Feedback Control : FS8S0965RCB employs primary side regulation, which permits elimination of feedback circuit components in the secondary side such as opto coupler and TL431. Figure 2 shows the primary side control circuit. The primary side regulation voltage (Vpsr) is controlled to the breakdown voltage of zener diode (Dz). Because current mode control is employed, the drain current of the power MOSFET is limited by the inverting input of PWM comparator (Vfb*). When MOSFET turns on, usually there exists high current spike in the MOSFET current caused by primary-side capacitance and secondary-side rectifier reverse recovery. In order to prevent premature termination of the switching pulse due to the current spike, the FPS employs leading edge blanking (LEB). The leading edge blanking circuit inhibits the PWM comparator for a short time after the MOSFET is turned on.

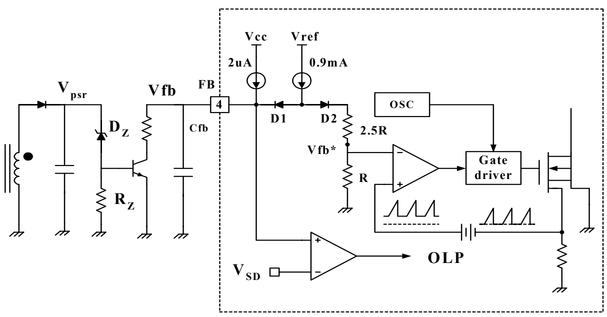


Figure 2. Primary side control circuit

3. Protection function : FS8S0965RCB has 4 self protective functions such as abnormal over current protection (AOCP), over load protection (OLP), over voltage protection (OVP) and thermal shutdown (TSD). Because these protection circuits are fully integrated into the IC without external components, the reliability can be improved without cost increase. In the event of these fault conditions, the FPS enters into auto-restart operation. Once the fault condition occurs, switching operation is terminated and MOSFET remains off, which forces Vcc to be reduced. When Vcc reaches 9V, the protection is reset and the supply current reduces to 80 uA. Then, Vcc begin to increase with the current provided through the start-up resistor. When Vcc reaches 15V, the FPS resumes its normal operation if the fault condition is removed. In this manner, the auto-restart alternately enables and disables the switching of the power MOSFET until the fault condition is eliminated as illustrated in figure 3.

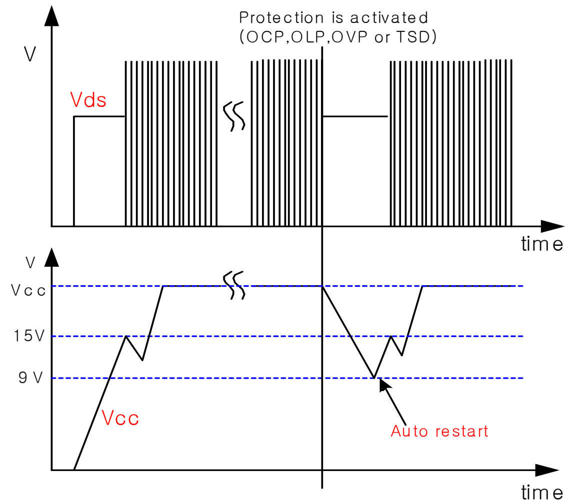


Figure 3. Auto restart operation after protection

3.1 Abnormal Over Current Protection (AOCP) : When the secondary rectifying diodes or the transformer pins are shorted, a steep current with extremely high di/dt can flow during the LEB time. Therefore, the abnormal over current protection (AOCP) block is added to ensure the reliability as shown in figure 4. It turns off the SenseFET within 300ns after the abnormal over current condition is sensed.

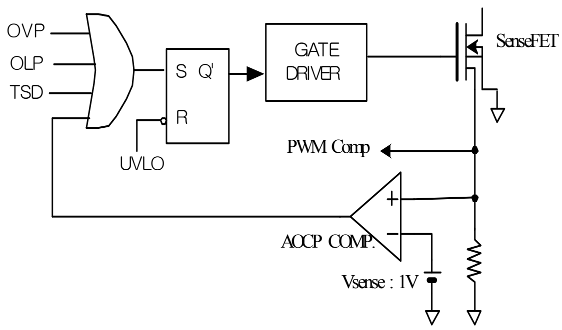


Figure 4. AOCP block

3.2 Over Load Protection (OLP) : When the load current exceeds a pre-set level for longer than pre-determined time, protection circuit should be activated in order to protect the SMPS. Because of the pulse-by-pulse current limit capability, the maximum peak current through the SMPS is limited, and therefore the maximum input power is restricted with a given input voltage. If the output consumes beyond this maximum power, the output voltage together with primary side regulation voltage decrease below the set voltage. This reduces the current through primary side regulation transistor, which increases feedback voltage (Vfb). If Vfb exceeds 2.7V, D1 is blocked and the 2uA current source starts to charge Cfb slowly compared to when the 0.9mA current source charges Cfb. In this condition, Vfb continues increasing until it reaches 7.5V, and the switching operation is terminated at that time as shown in figure 6. The delay time for shutdown is the time required to charge Cfb from 2.7V to 7.5V with 2uA.

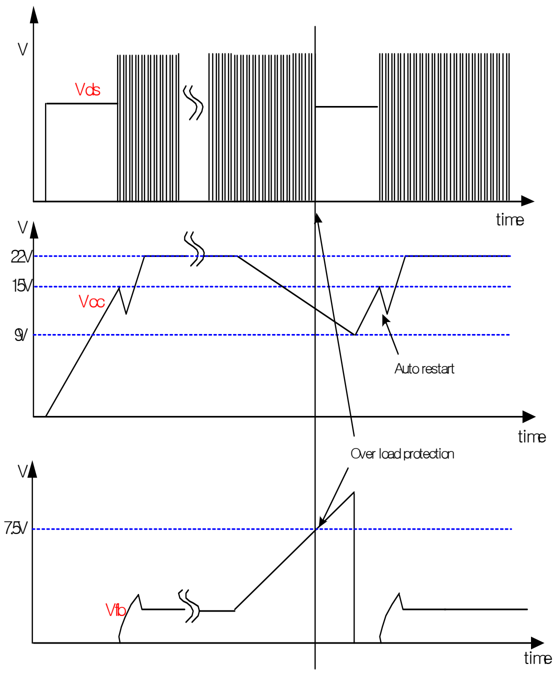


Figure 5. The waveforms at the OLP and auto restart

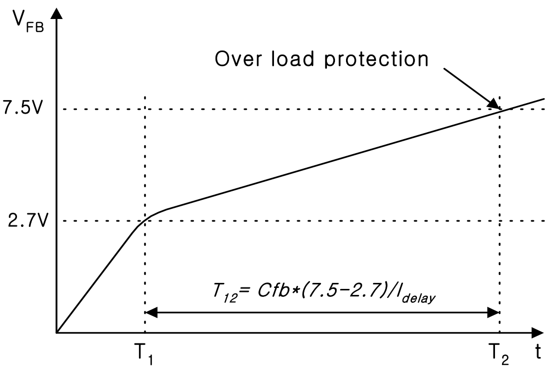


Figure 6. Over load protection

3.3 Over Voltage Protection (OVP) : In case of malfunction in the primary side feedback circuit, or feedback loop open caused by a defect of solder, the current through primary side control transistor becomes almost zero. Then, Vfb climbs up in a similar manner to the over load situation, forcing the preset maximum current to be supplied to the secondary side until the over load protection is activated. Because energy more than required is provided to the output, the output voltage may exceed the rated voltage before the over load protection is activated, resulting in the breakdown of the devices in the secondary side. In order to prevent this situation, an over voltage protection (OVP) circuit is employed. When the Vcc voltage touches 37V, the OVP block is activated.

3.4 Thermal Shutdown (TSD) : The SenseFET and the control IC are built in one package. This makes it easy for the control IC to detect the heat generation from the SenseFET. When the temperature exceeds approximately 160°C, the thermal shutdown is activated.

4. Soft Start : Figure 7 shows the soft start circuit. During the initial start up, the 0.9 mA current source leaks out through Css and Rss. As Css is charged, the leakage current decreases. Therefore, by choosing much bigger Css than Cfb, it is possible to increase the feedback voltage slowly forcing the SenseFET current to increase slowly. After Css reaches its steady state value, D3 is blocked and the soft switching circuit is decoupled from the feedback circuit. If the value of Css is too large, there is possibility that Vfb increases to 7.5V activating the over load protection during soft start time. In order to avoid this situation, it is recommended that the value of Css should not exceed 100 times of Cfb.

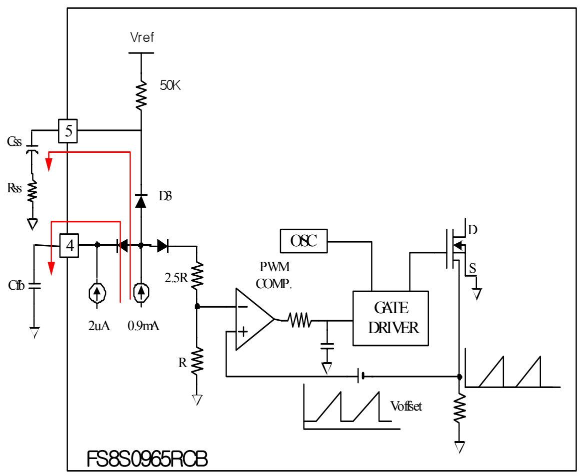


Figure 7. The circuit for the soft start

5. Synchronization : In order to reduce the effect of switching noise on the screen, the SMPS for monitor synchronizes its switching frequency to an external signal, typically the horizontal sync flyback signal. The switching frequency of the FPS can vary from 20 kHz to 150 kHz according to the external sync signal. The internal sync comparator detects the sync signal and determines the SenseFET turn-on time. The SenseFET is turned on at the negative edge of the sync comparator output. The reference voltage of the sync comparator is an inverted saw tooth with a base frequency of 20kHz and a varying range between 5.8V and 7.2V, as shown in the figure 8. The inverted saw tooth reference gets rid of the excessive switching noise at the first synchronized turn-on. The external sync signal is recommended to have an amplitude higher than 4.2V.

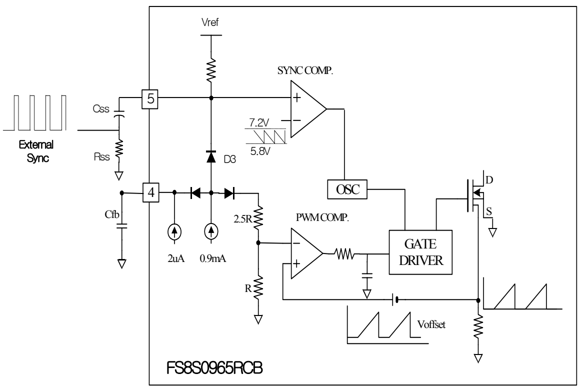


Figure 8. The circuit for the synchronization with external sync

6. Burst mode operation : In order to minimize the power dissipation at standby mode, FS8S0965RCB has a burst mode operation. In burst mode, the FPS reduces the effective switching frequency and output voltage. The FPS enters into burst mode when the voltage of the soft start pin is higher than 3V, no sync signal is applied and the feedback voltage is lower than 1V. During the burst mode operation, Vcc is hysteresis controlled between 11V and 12V. Once the FPS enters into burst mode, it stops switching operation until Vcc drops to 11V. When Vcc reaches 11V, the FPS starts switching with switching frequency of 40kHz and peak MOSFET current of 0.6 A until Vcc reaches 12V. When Vcc reaches 12V, the switching operation is terminated again until Vcc reduces to 11V. Figure 9 shows operating waveforms. The soft start during the initial start-up is shown in the section 1. During this period, there is no external sync signal and the switching frequency is 20kHz. The section 2 represents the normal mode operation. The switching frequency is synchronized with the external sync signal. In the section 3, the external sync signal is removed. However, the load still exists and thus the feedback voltage (Vfb) is higher than 1V. In this period, the FPS does the normal switching operation with switching frequency of 20kHz. The section 4 and 5 show the burst mode operation. At the end of the section 3, the load is eliminated and the feedback voltage (Vfb) drops below 1V forcing the FPS to stop switching operation. During the section 4, Vcc goes down to 11V. During section 5, Vcc is hysteresis controlled between 11V and 12V. When the external sync signal is applied on the pin 5, the FPS resumes its normal operation. In order to minimize the power consumption in standby mode, it is recommended to set the value of Vcc during normal operation as high as possible (about 29V).

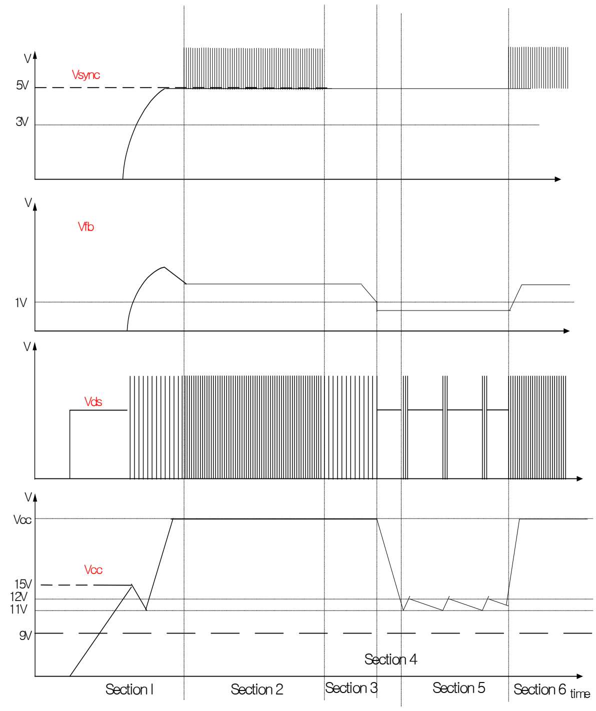
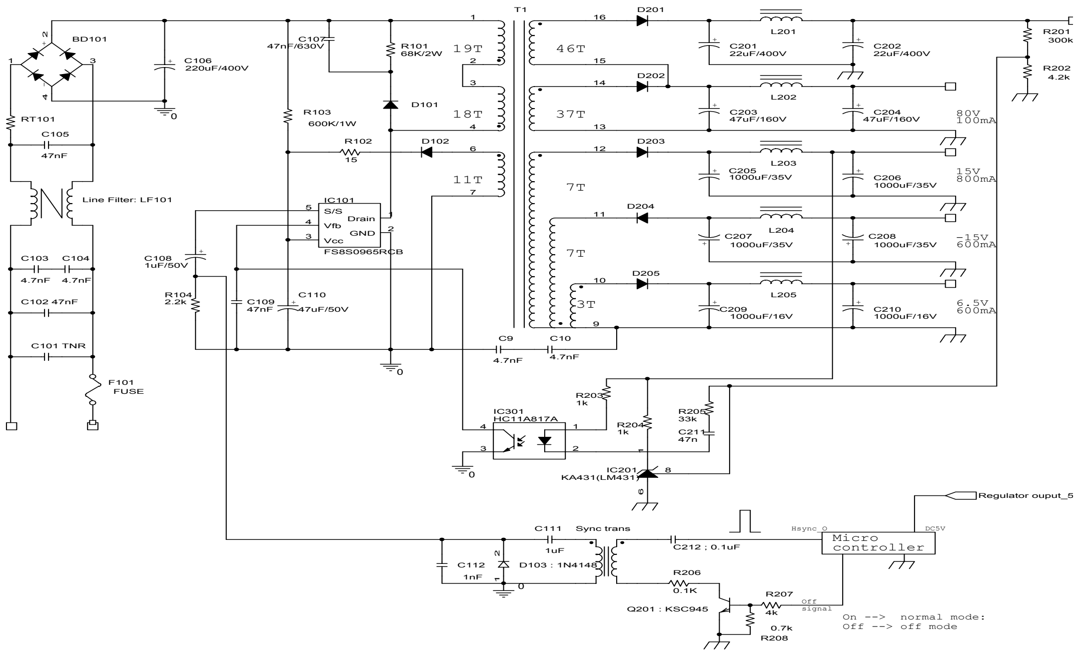


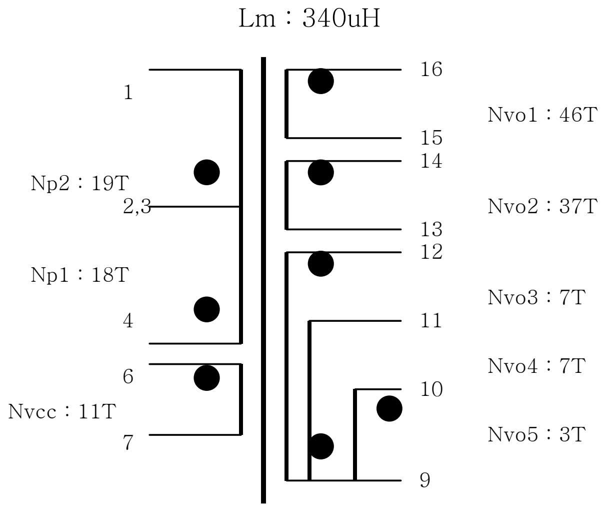
Figure 9. The operation of the FS8S0965RCB at the normal mode and the off mode

Typical application circuit

1. 100W Universal Input Power Supply For CRT Monitor



2. Transformer Schematic Diagram



3.Winding Specification

No	Pin (s→f)	Wire	Turns	Winding Method
Np1	4 → 3	$0.3^{\phi} \times 3$	18	Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Nvo1	16 → 15	$0.3^{\phi} \times 2$	46	Center Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Nvo5	10 → 9	0.45^{ϕ}	3	Center Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Np4	9→ 11	$0.3^{\phi} \times 3$	7	Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Nvo3	12 → 9	$0.3^{\phi} \times 3$	7	Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Nvo2	14 → 13	$0.3^{\phi} \times 2$	37	Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Nvcc	6 → 7	0.2^{ϕ}	11	Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Np2	2 → 1	$0.3^{\phi} \times 3$	19	Solenoid Winding
Outer Insulation: Polyester Tape t = 0.050mm, 2Layers				

4.Electrical Charateristics

	Pin	Specification	Remarks
Inductance	1 - 4	340uH ± 10%	300kHz, 1V
Leakage Inductance	1 - 4	5uH Max	2^{nd} all short

5. Core & Bobbin

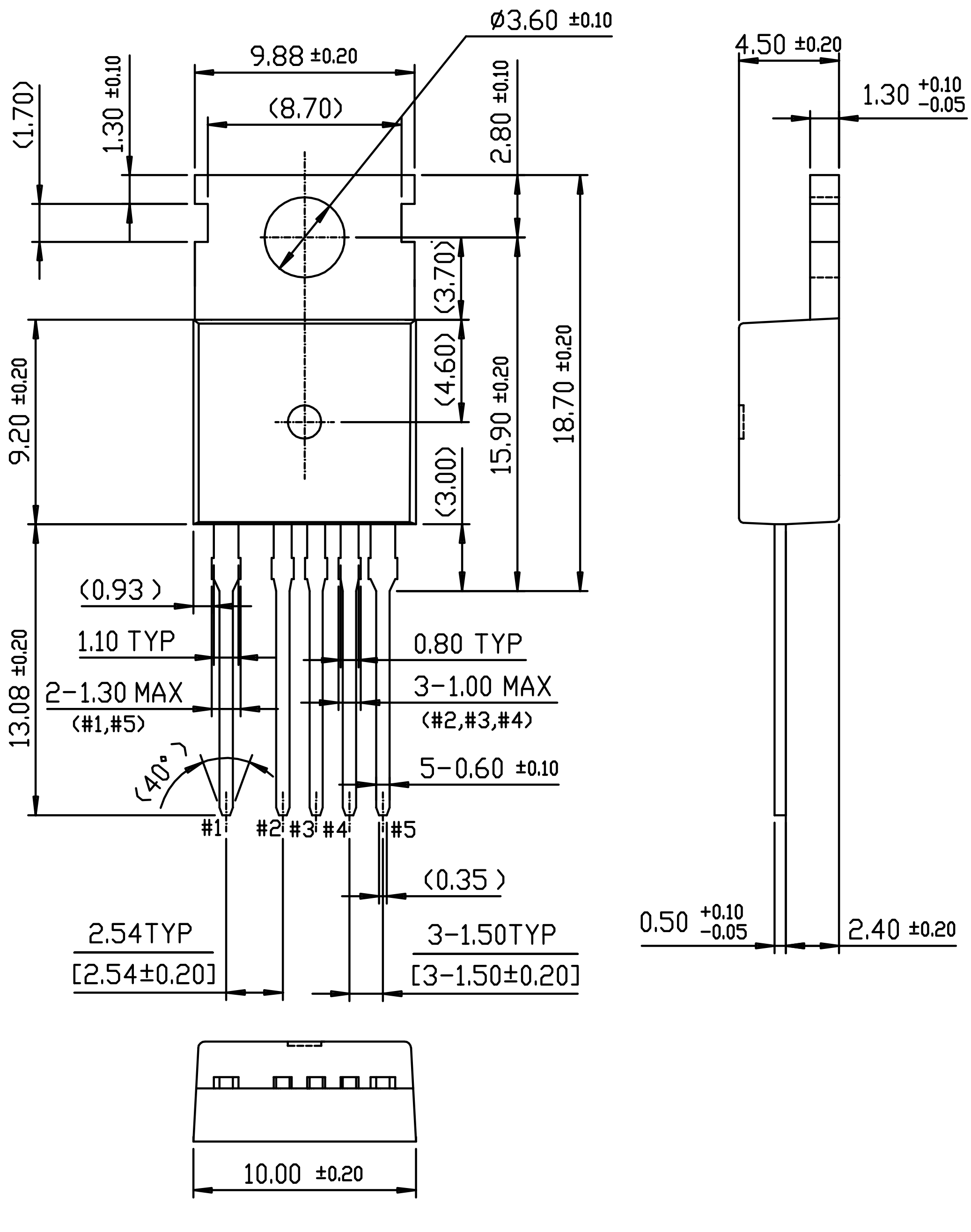
Core : EER 4044
Bobbin : EER 4044
Ae(mm2) : 154

6.Demo Circuit Part List

Part	Value	Note	Part	Value	Note
Fuse			C201	22uF/400V	Electorlytic Capacitor
F101	3A/250V	-	C202	22uF/400V	Electorlytic Capacitor
NTC			C203	47uF/160V	Electorlytic Capacitor
RT101	10D-9	-	C204	47uF/160V	Electorlytic Capacitor
Resistor			C205	1000uF/35V	Electorlytic Capacitor
R101	68K	2W	C206	1000uF/35V	Electorlytic Capacitor
R102	15	1/4W	C207	1000uF/35V	Electorlytic Capacitor
R103	600K	1W	C208	1000uF/35V	Electorlytic Capacitor
R104	2.2K	1/4W	C209	1000uF/16V	Electorlytic Capacitor
R201	300K	1/4W	C210	1000uF/16V	Electorlytic Capacitor
R202	4.2K	1/4W	C211	47nF/50V	Ceramic Capacitor
R203	1K	1/4W	C212	0.1uF/16V	Electorlytic Capacitor
R204	1K	1/4W	C301	4.7nF	AC Filter Capacitor
R205	33K	1/4W	C302	4.7nF	AC Filter Capacitor
R206	0.1K	1/4W			
R207	4K	1/4W			
R208	0..7K	1/4W			
			Sync trans	22mH	
Inductor					
L201 ~ L205	13uH				
			Diode		
			D101	UF4007	
Capacitor			D102	TVR10G	
C101	471D10	TNR	D103	1N4148	
C102	47nF	Box Capacitor	D201	RG4C	
C103	4.7nF	AC Filter Capacitor	D202	SUF15J	
C104	4.7nF	AC Filter Capacitor	D203	UG4D	
C105	47nF	Box Capacitor	D204	UG4D	
			D205	UG4D	
C106	220uF/400V	Electorlytic Capacitor	D206	UF4004	
C107	47nF/630V	Caramic Capacitor			
C108	1uF/50V	Electorlytic Capacitor	BD101	KBU6G	Bridge Diode
C109	47nF/50V	Caramic Capacitor	**Line Filter**		
C110	47uF/50V	Electorlytic Capacitor	LF101	24mH	
C111	1uF/50V	Electorlytic Capacitor	**IC**		
C112	1nF/50V	Caramic Capacitor	IC101	FS8S0965RCB	(9A, 650V)
			IC201	KA431	
			IC301	H11A817A	Photo coupler/QT
			Q201	KSC945	NPN Transistor

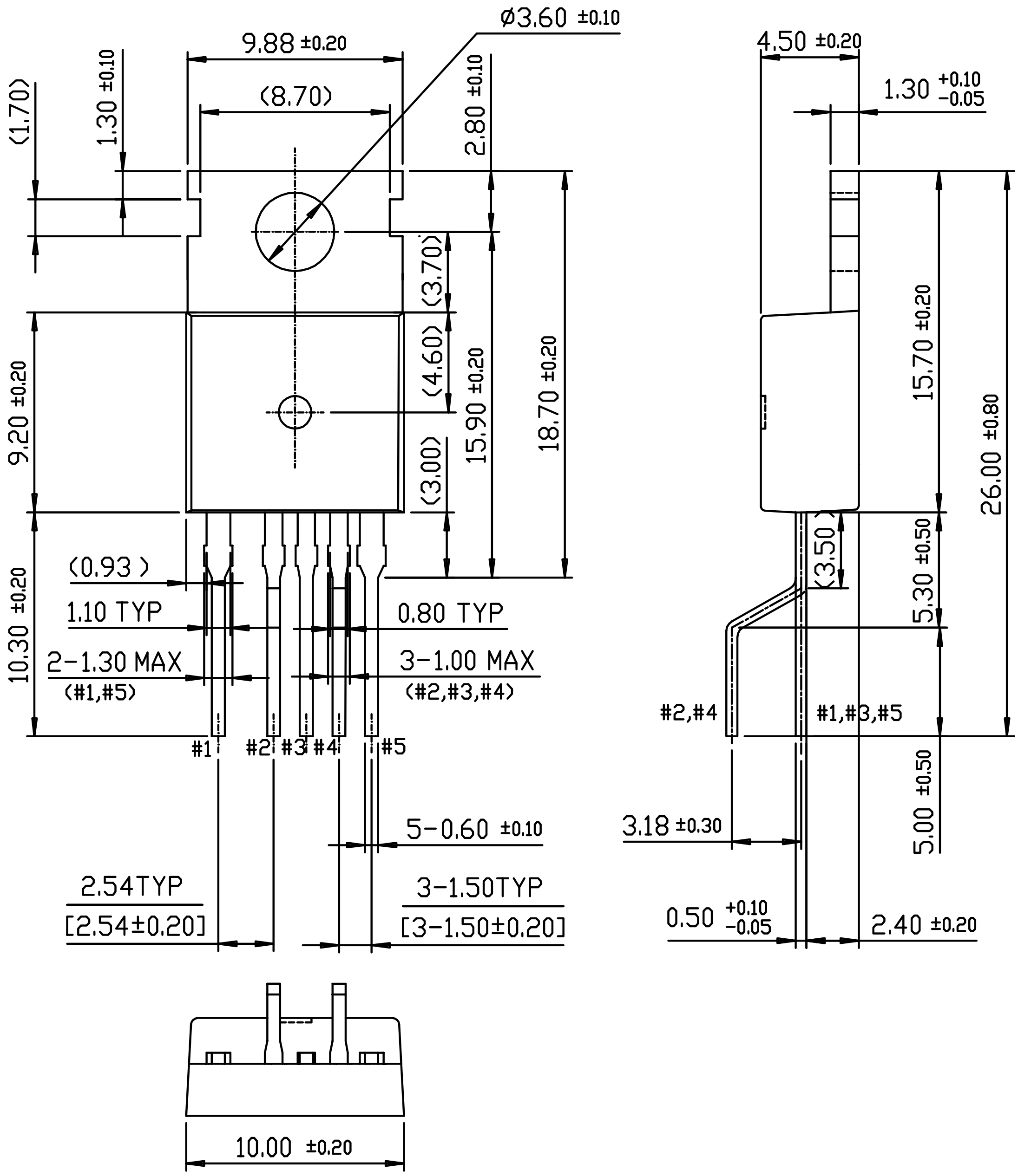
Package Dimensions

TO-220-5L



Package Dimensions (Continued)

TO-220-5L(Forming)



Ordering Information

Product Number	Package	Marking Code	BVdss	Rds(on)Max.
FS8S0965RCBTU	TO-220-5L	8S0965RCB	650V	1.2
FS8S0965RCBYDTU	TO-220-5L(Forming)			

TU : Non Forming Type
YDTU : Forming Type

DISCLAIMER

LIFE SUPPORT POLICY

12/26/03 0.0m 001
Stock#DSxxxxxxxx